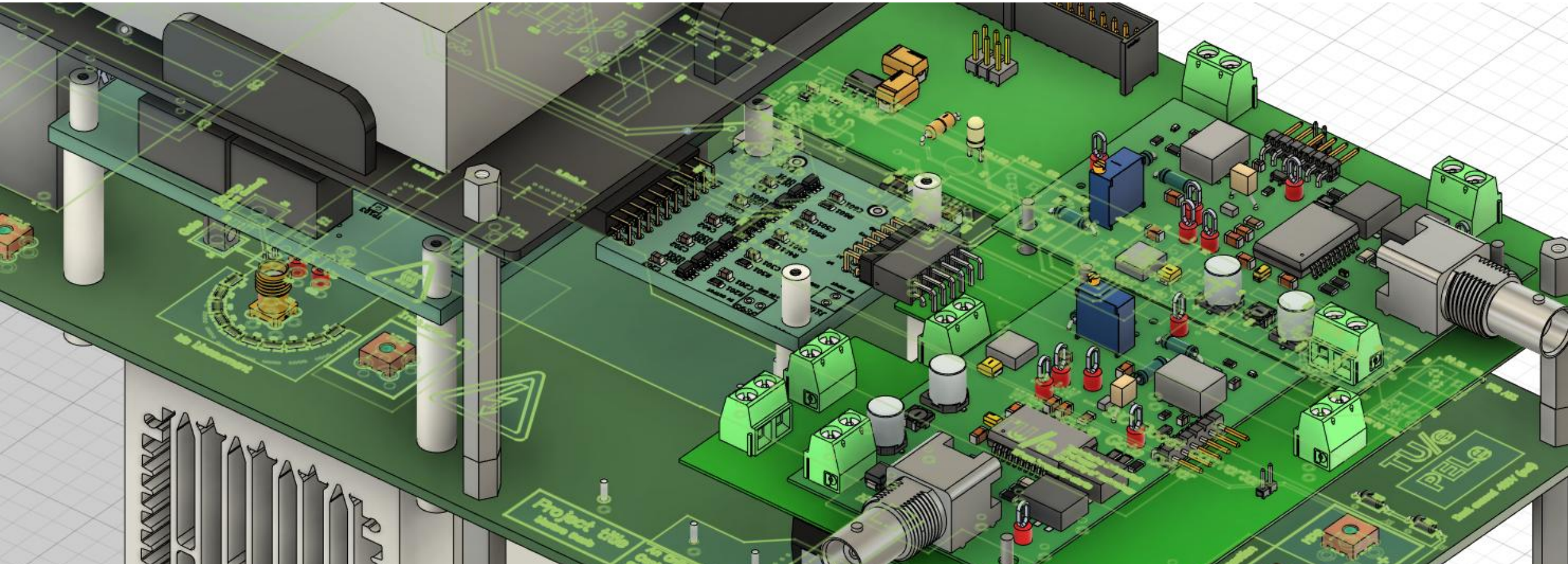
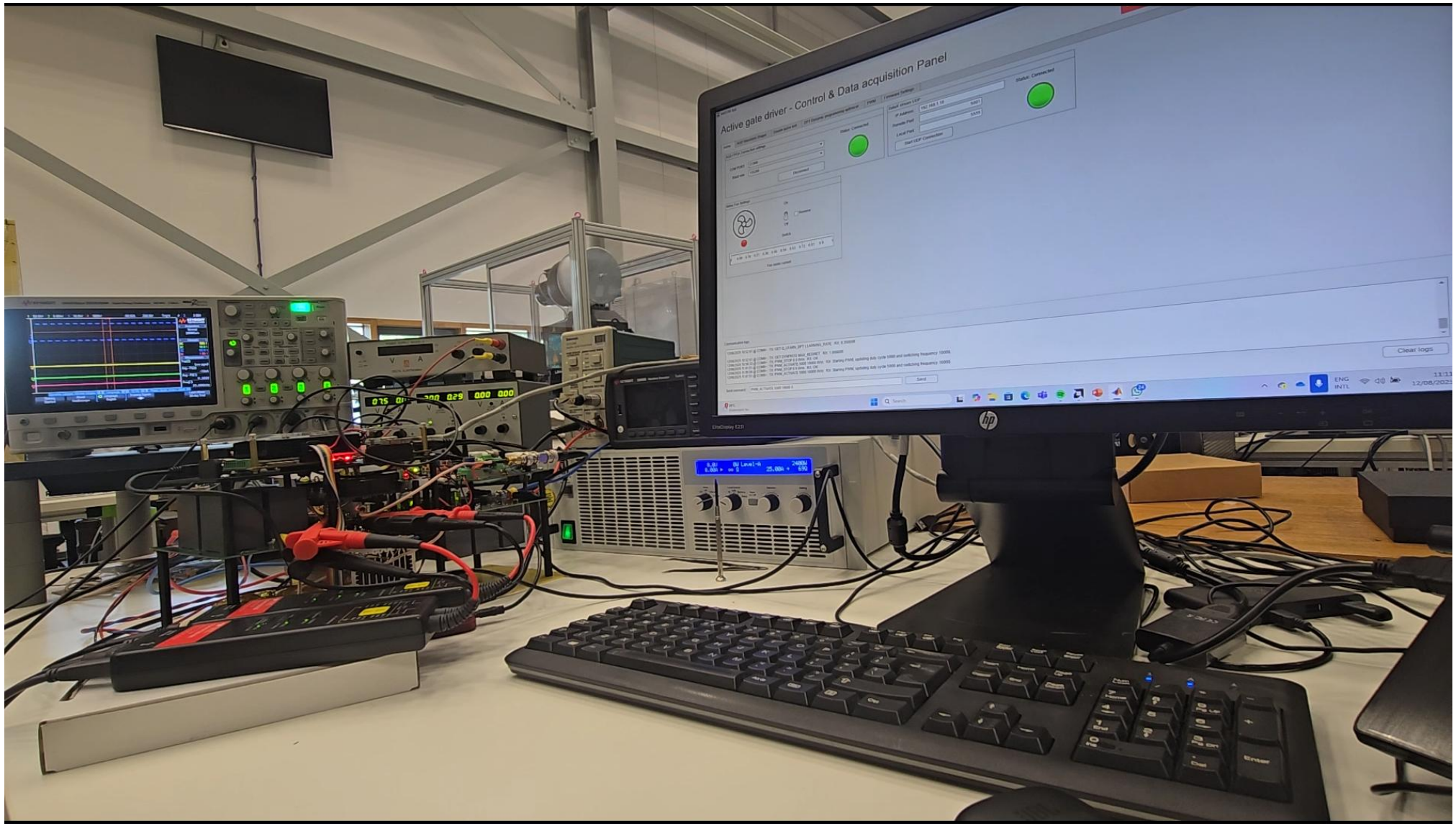
Computational model-free active gate driver control For SiC MOSFETs

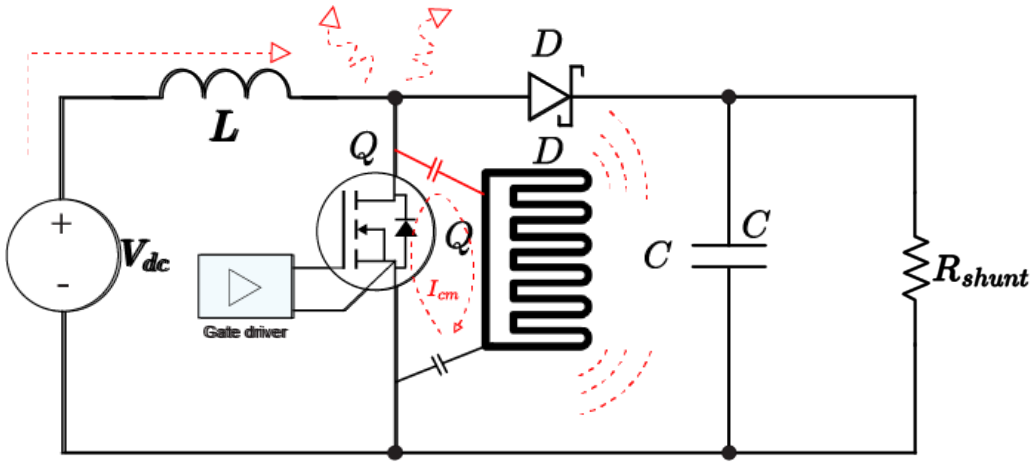
Nart Gashi

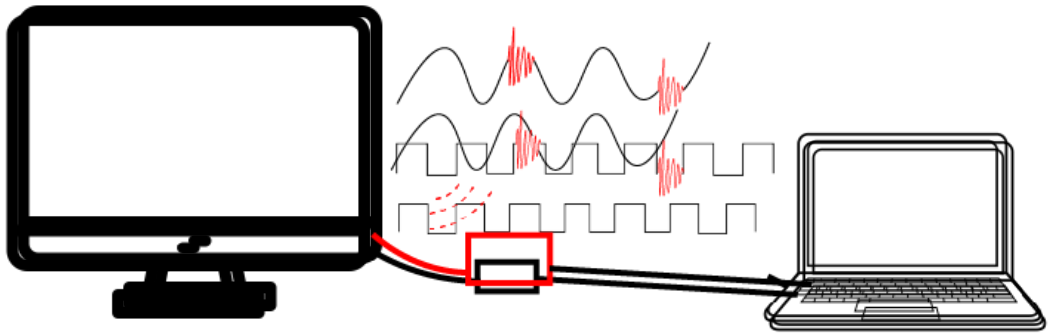



Active gate driver - Control & Data acquisition Panel
Clear logs

So why is the monitor shutting down?

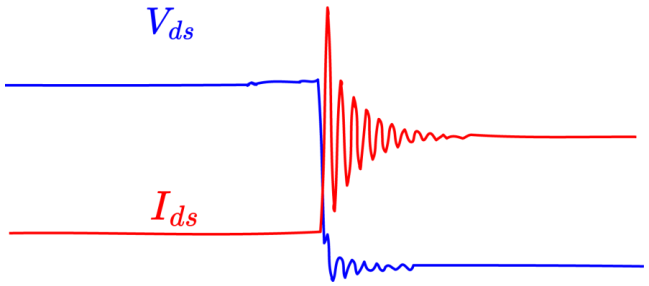
Answer: Bad EMC design! (Both of my 2 kW boost converter and the monitor HDMI adapter)





Switching cycles:

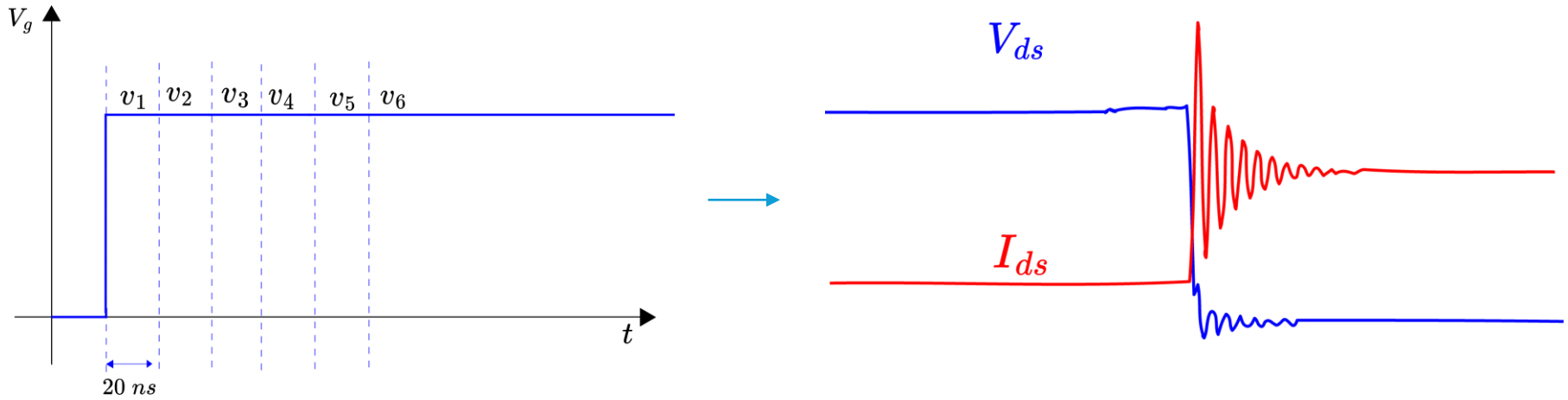
Switching transients:



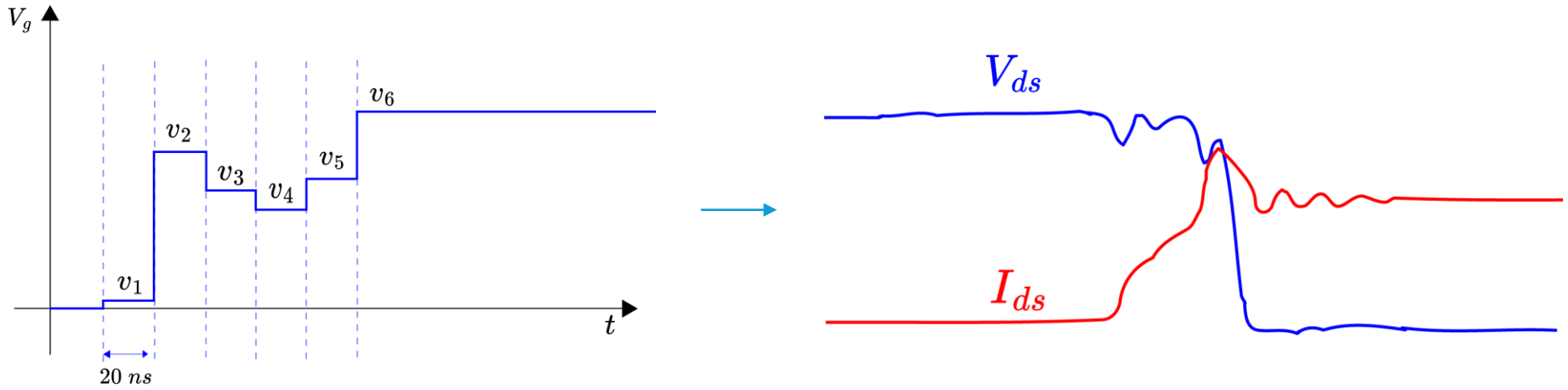
At the core of EMC-related challenges in power converters lies the power switching device

SiC MOSFET dv/dt: 200 V/ns

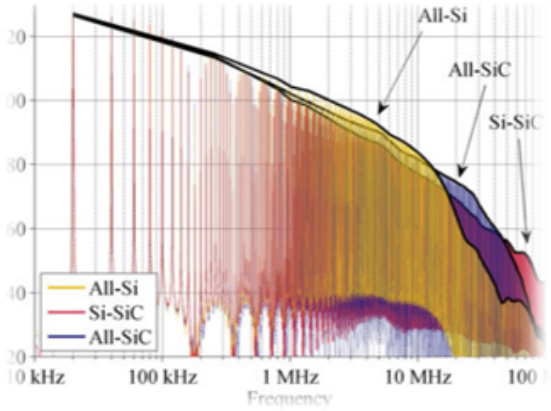
Conventional gate drivers:



Active gate drivers:

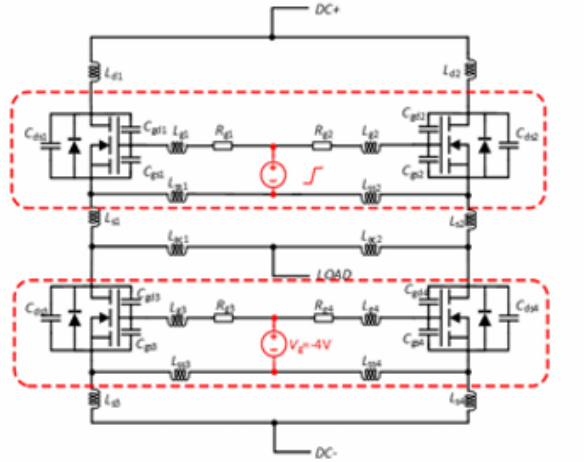


Intelligent gate-drives (closed-loop control)



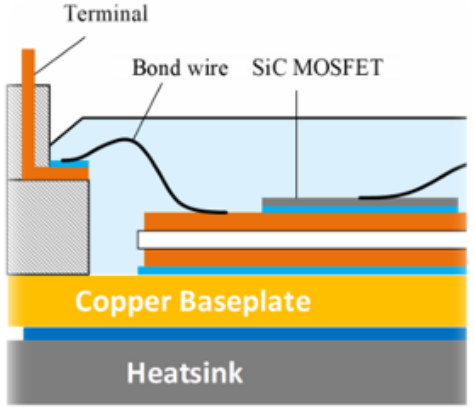
Electromagnetic Interference improvement

Fast switching in WBG devices can increase EMI, which can be suppressed through adaptive gate-voltage control.



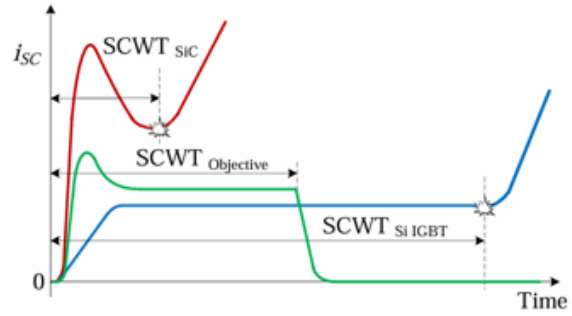
Improving Current imbalance in multi-die packaging

Uneven current sharing and turn-on gate-drive oscillations in SiC modules can be mitigated with intelligent gate drivers.



Device lifetime enhancement

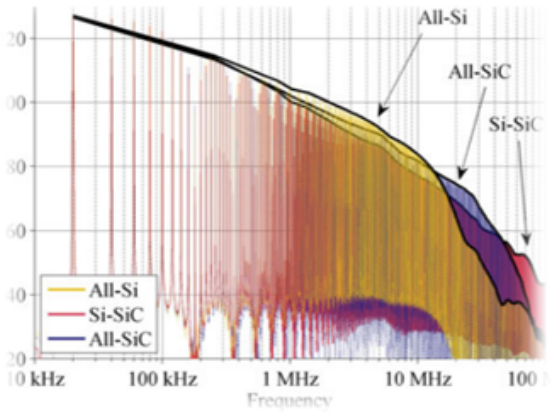
Through smart control of switching and conduction losses, by minimizing thermal cycling.



Device Protection

Intelligent gate drivers can detect faults and degradation early, protecting devices through real-time gate-voltage adjustment.

Intelligent gate-drives (closed-loop control)



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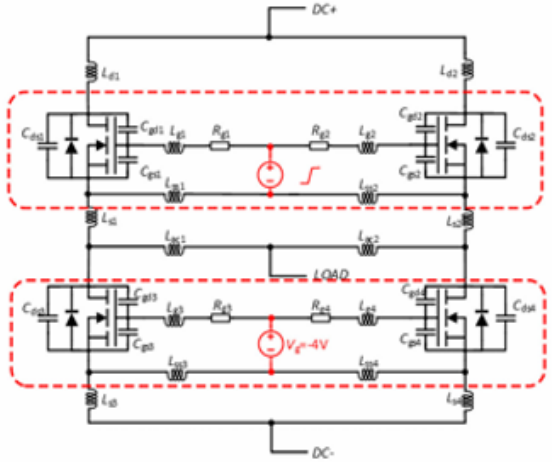

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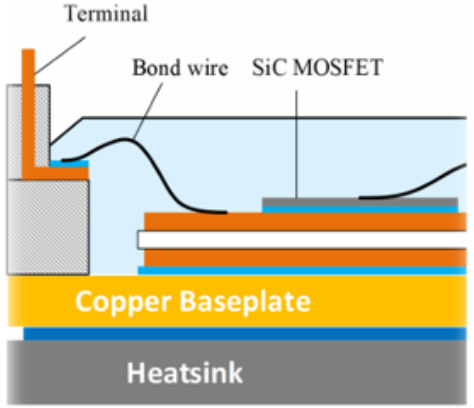

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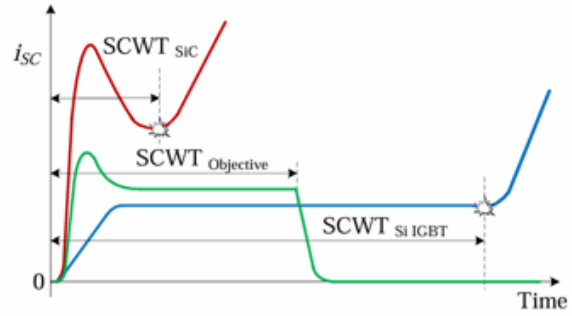


Device Protection

Intelligent gate drivers can detect faults and degradation early, protecting devices through real-time gate-voltage adjustment.

Challenges in intelligent gate drivers

- Switching events last only a few tens to hundreds of nanoseconds

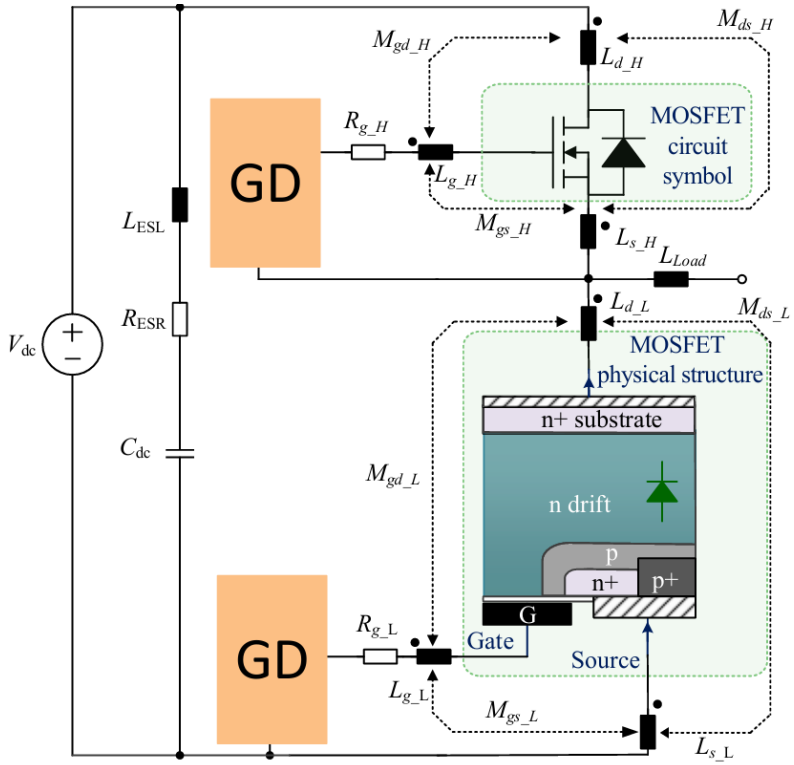
→ Difficulties in sensing

- Device models are highly inaccurate and nonlinear
- Device behaviour changes through temperature change and aging
- Device behaviour is also based on the layout and converter topology

→ Difficulties in modelling for control

- Limited computational capabilities

→ Difficulties in computational control

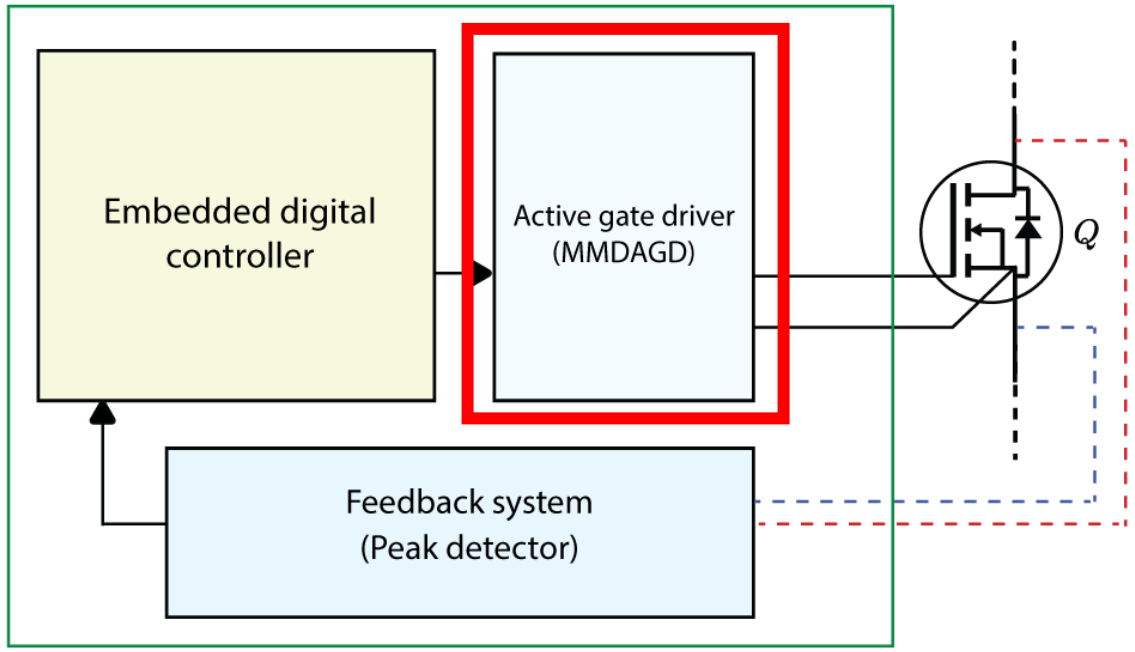


Highly non-linear!

Computational model-free active gate driver control

Computational Intelligence

Capable hardware



Awareness

Online adaptive gate driver architecture

Topology of active gate driver (MMDAGD)

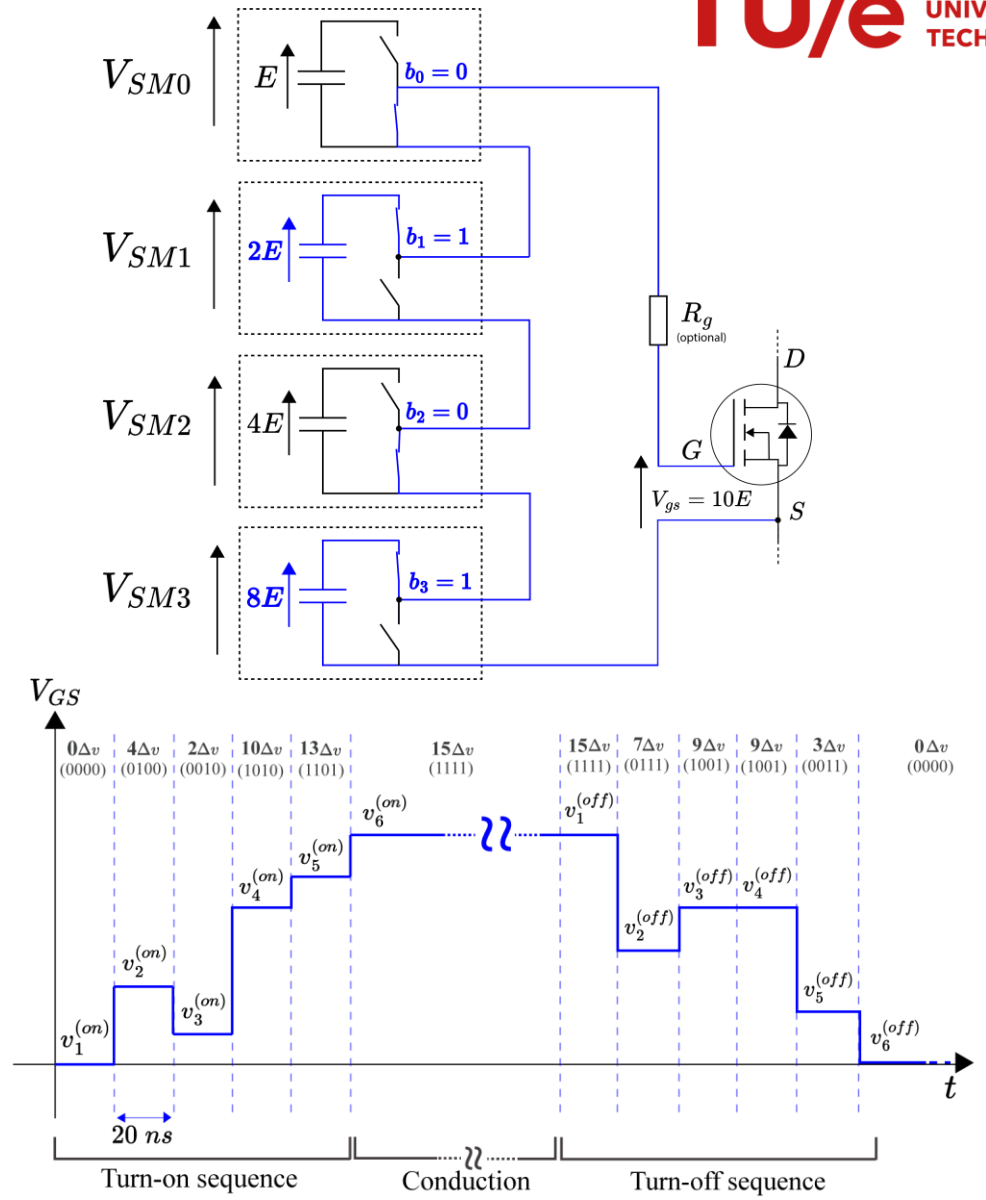
- Voltage-source based gate driver composed of series connecting l floating sub-modules V_{SM}

- A turn-on/turn-off profile (or sequence) is defined as k steps:

$$\mathbf{v} = [v_1, v_2, \ldots, v_k]$$

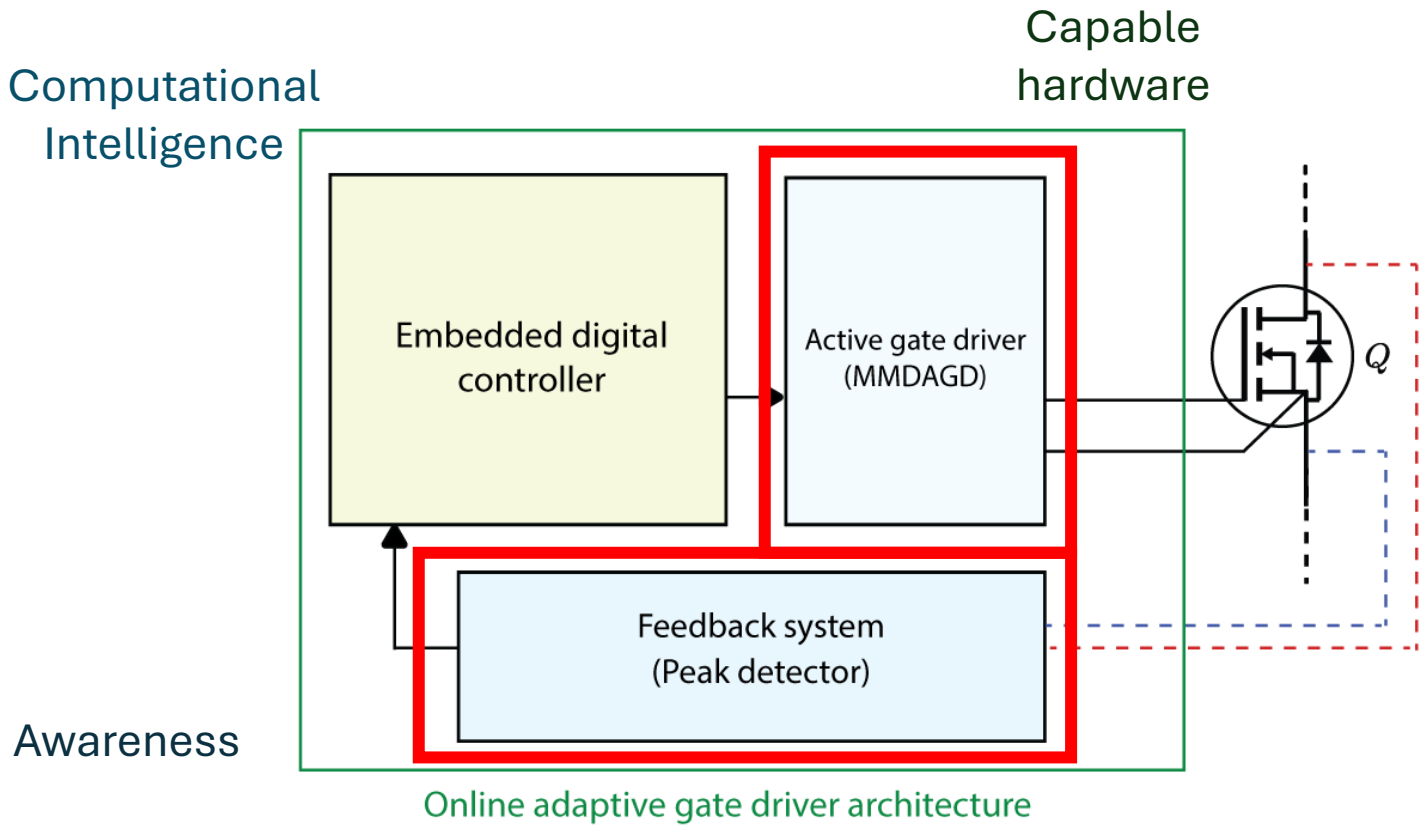
- Where the feasible voltage construction set is defined as:

$$\mathcal{V} = \{0, \Delta v, 2\Delta v, \ldots, (2^l - 1)\Delta v\}$$



[1]: Takayama, H., Fukunaga, S. and Hikihara, T., 2023, September. Binary-weighted modular multi-level digital active gate driver. In 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe) (pp. 1-8). IEEE.

Computational model-free active gate driver control



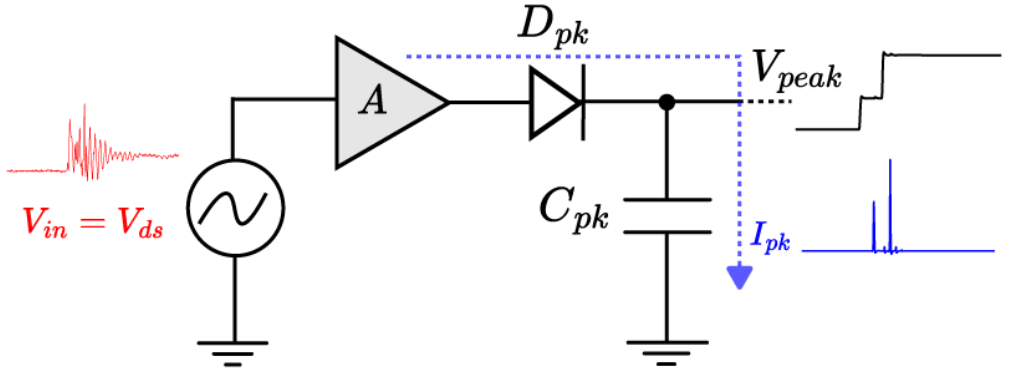
Feedback: Peak detector

- To assess the switching performance, we utilize peak detectors to measure overshoot on
- Measuring I_{Ds} (during turn-on), and/or V_{DS} (during turn-off)
  - The current charging capacitor C_{pk} can be denoted as:

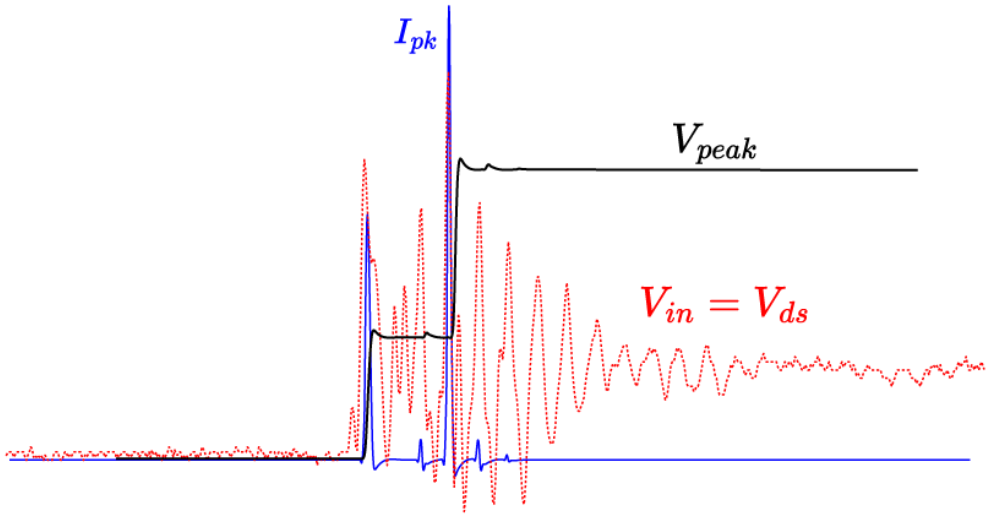
$$i_C(t) = I_{\mathrm{pk}}(t) = \begin{cases} C_{\mathrm{pk}} \dfrac{\mathrm{d}v_{\mathrm{in}}(t)}{\mathrm{d}t}, & v_{\mathrm{in}}(t) > v_{\mathrm{pk}}(t) + v_{d,\mathrm{th}}, \\ 0, & \text{otherwise.} \end{cases}$$

  - In which the final (peak) voltage is denoted as:

$$v_{\mathrm{pk}}(t) = v_{\mathrm{pk}}(0) + \frac{1}{C_{\mathrm{pk}}} \int_0^t i_C(\tau)\,\mathrm{d}\tau.$$

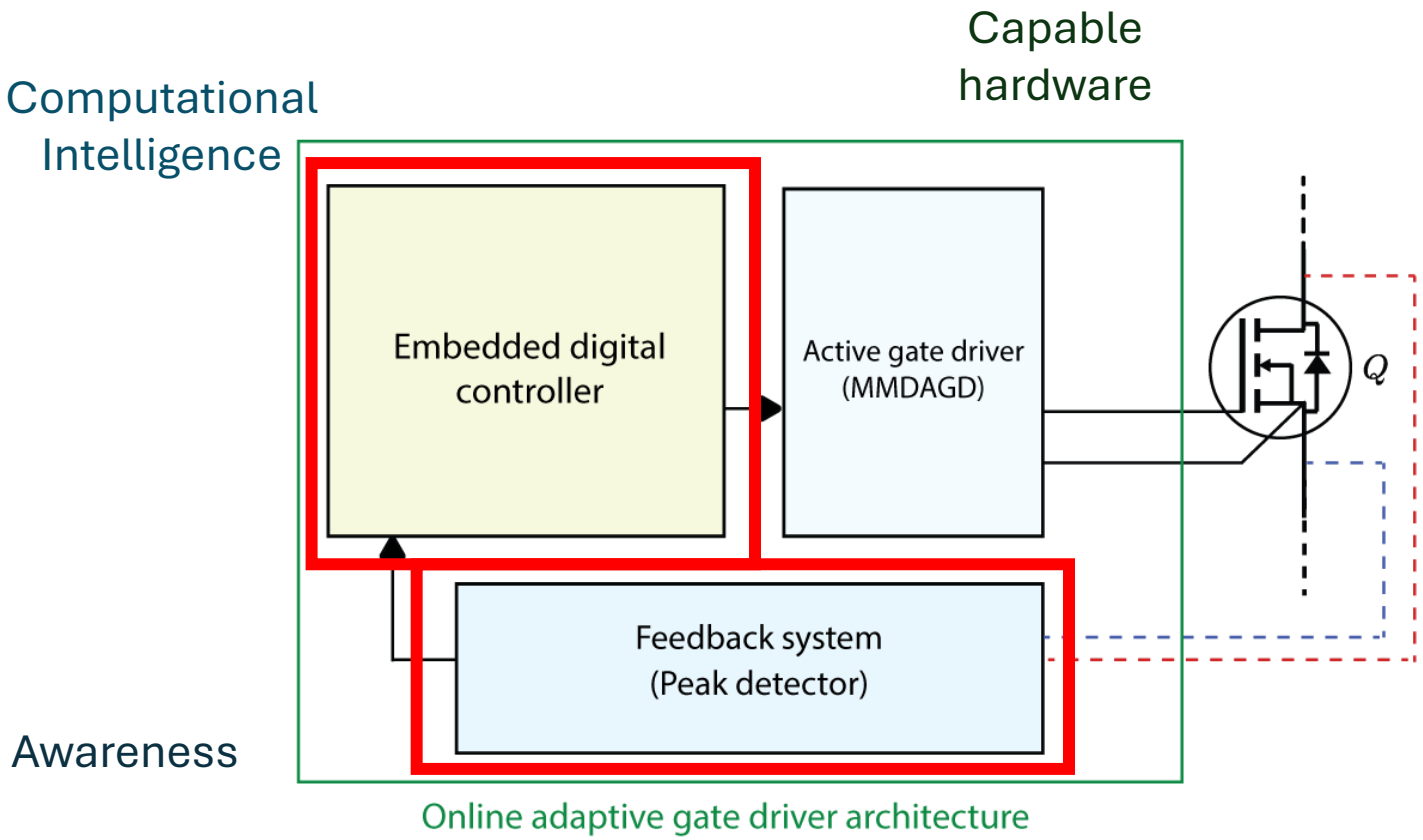


Simplified peak detector circuit



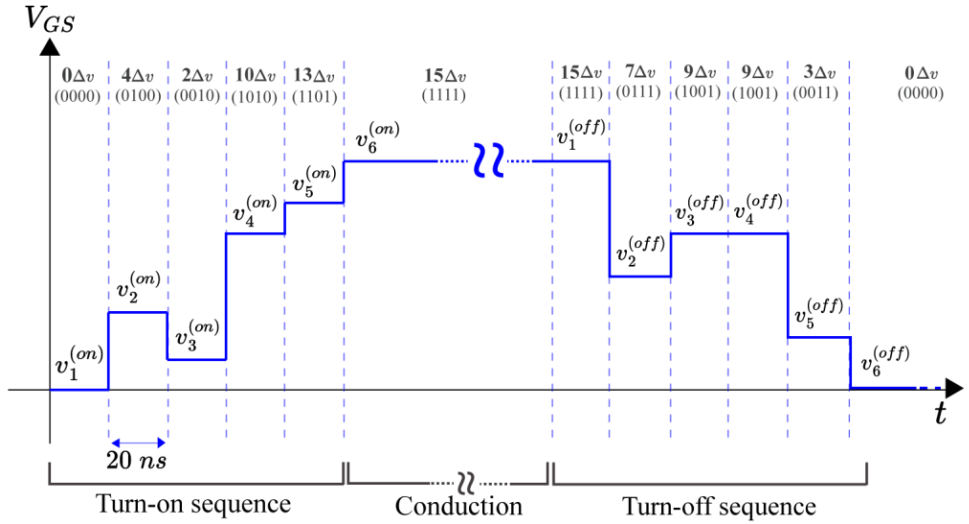
Peak detector example using Vds

Computational model-free active gate driver control



- How can we choose $v_i \in$, such that we minimize overshoot while maintaining low switching loss?

- For switching energy losses keep the switching event as short as possible (e.g. 20 ns, 3 steps)
- For minimizing overshoot and ringing, we will optimize in real-time
- N-dimensional problem with implicit formulation, with up to ~15^6 possible solutions



- A turn-on/turn-off profile (or sequence) is defined as k steps: $\mathbf{v} = [v_1, v_2, \ldots, v_k]$

MMDAGD feasible set:

$$\mathcal{V} = \{0, \Delta v, 2\Delta v, \ldots, (2^l - 1)\Delta v\}$$

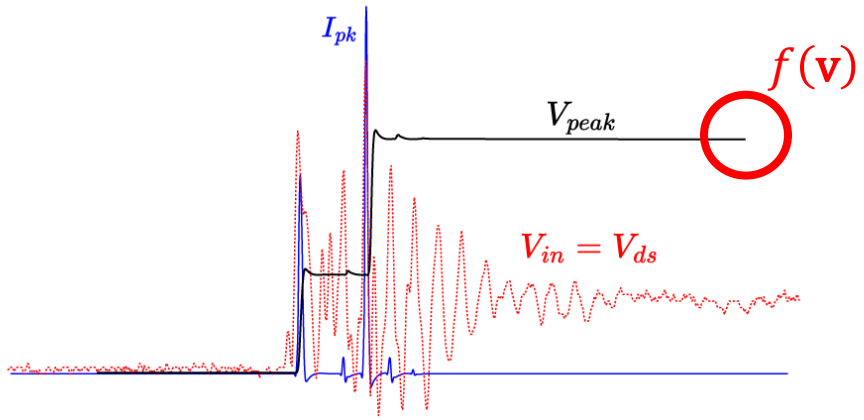
- Optimization objective function:

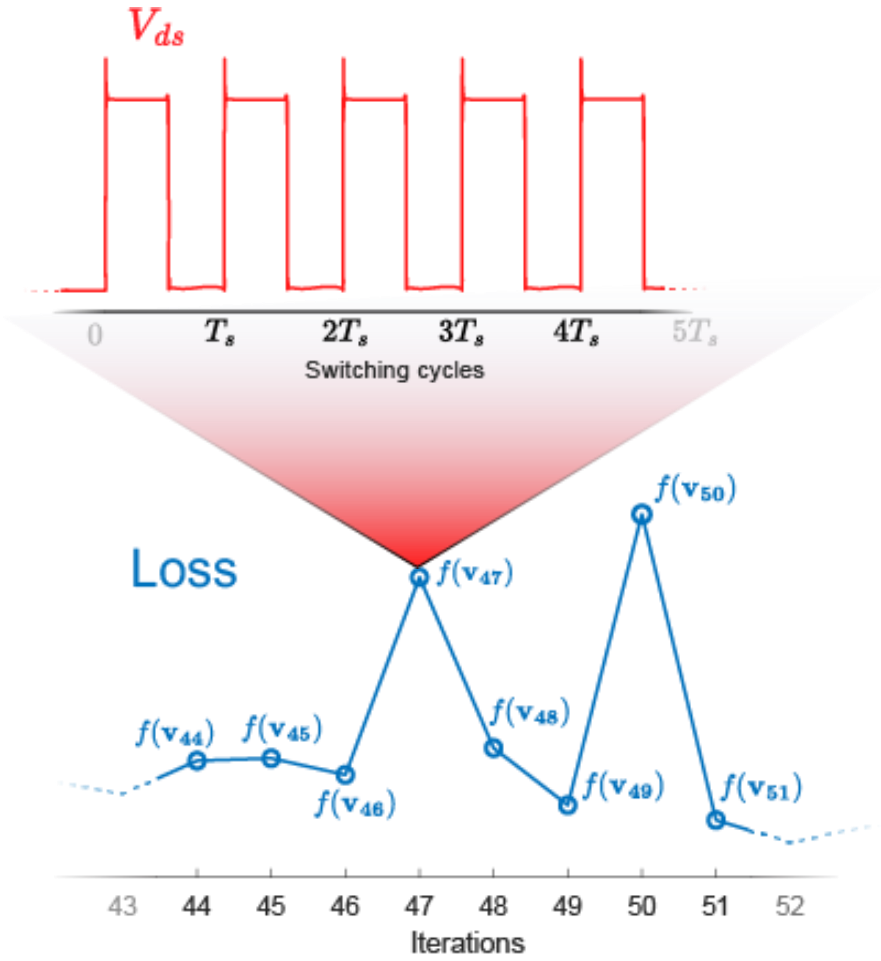
$$\mathbf{v}^* = \arg\min_{\mathbf{v}\in\mathbb{R}^k} f(\mathbf{v}) \quad \text{s.t.} \quad v_i \in \mathcal{V} \quad \forall i = 1, \ldots, k.$$

- $f(\mathbf{v})$: The cost (or loss) function
- $\mathbf{v}^*$: Optimal solution

The waveform optimization algorithm: Loss (cost) function

- Because we do not have any model, we must experiment with different waveforms in order compute a 'loss' (or cost)
- Hence, we define $f(\mathbf{v})$ as a experiment of one or multiple switching cycles in the operating converter
- Physically, $f(\mathbf{v})$ is the averaged output voltage of the peak detector (over one or multiple switching cycles).





Waveform optimization algorithm 1 / 2 (Coordinate descent)

Coordinate descent algorithm:

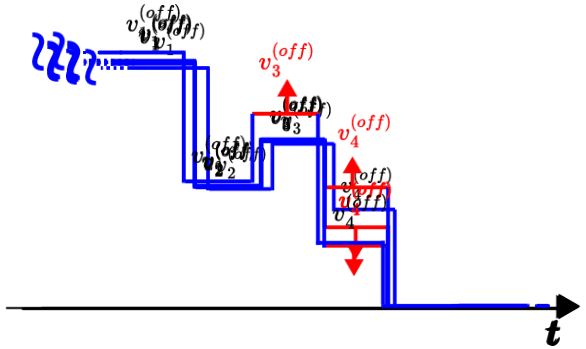
- Step 1) Initialize waveform randomly
- Step 2) Start by increasing the last element in the positive direction by Δv

$$f(v_1, \ldots, v_i + \Delta v, \ldots, v_k) < f(v_1, \ldots, v_i, \ldots, v_k)$$

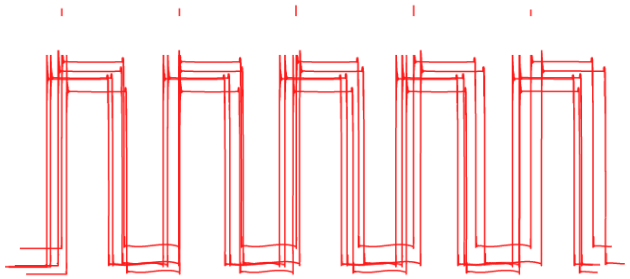
- Step 3) If loss improved continue until no further improvement; If not improved, probe negative direction

$$f(v_1, \ldots, v_i - \Delta v, \ldots, v_k) < f(v_1, \ldots, v_i, \ldots, v_k)$$

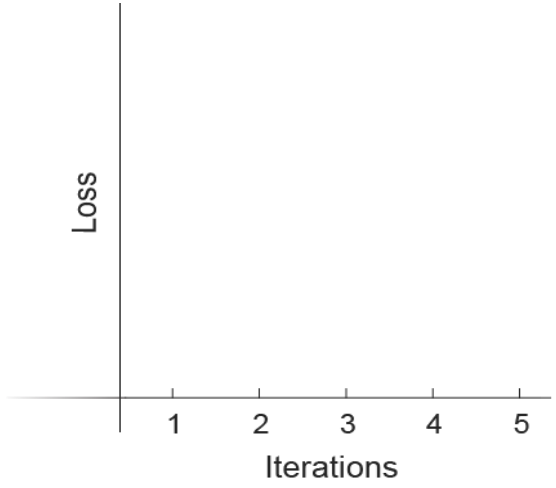
- Step 4) Continue until no longer improves; Repeat same for all $v_i \in \mathbf{v}$



V_{GS} Turn-off sequence



Switching cycles



Waveform optimization algorithm 2 / 2 (Gradient descent)

- Step 1) Initialize waveform randomly
- Step 2) Create a 'neighbourhood' of candidate waveforms and evaluate all of them

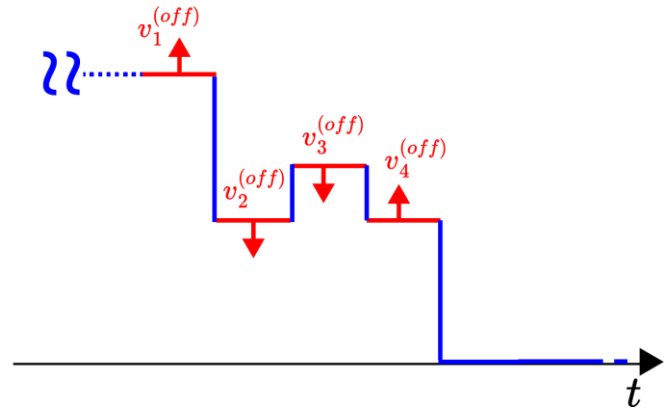
$$\mathcal{N}(\mathbf{v}) = \Big\{ \mathbf{v}' \in \mathbb{R}^k \;\Big|\; v_i' \in \{v_i - \Delta v, v_i, v_i + \Delta v\}, \; v_i \in \mathcal{V},\ \forall i \in \{1, \ldots, k\} \Big\}.$$

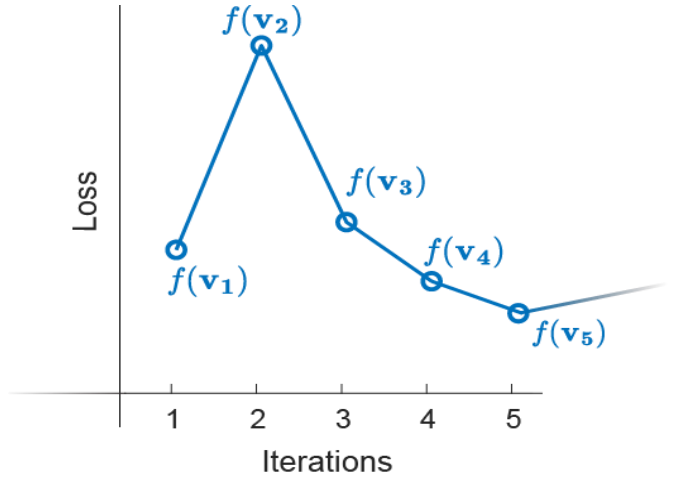
- Step 3) Pick the one which yields the lowest loss

$$\mathbf{v}^{(t+1)} = \arg \min_{\mathbf{v}' \in \mathcal{N}(\mathbf{v}^{(t)})} f(\mathbf{v}').$$

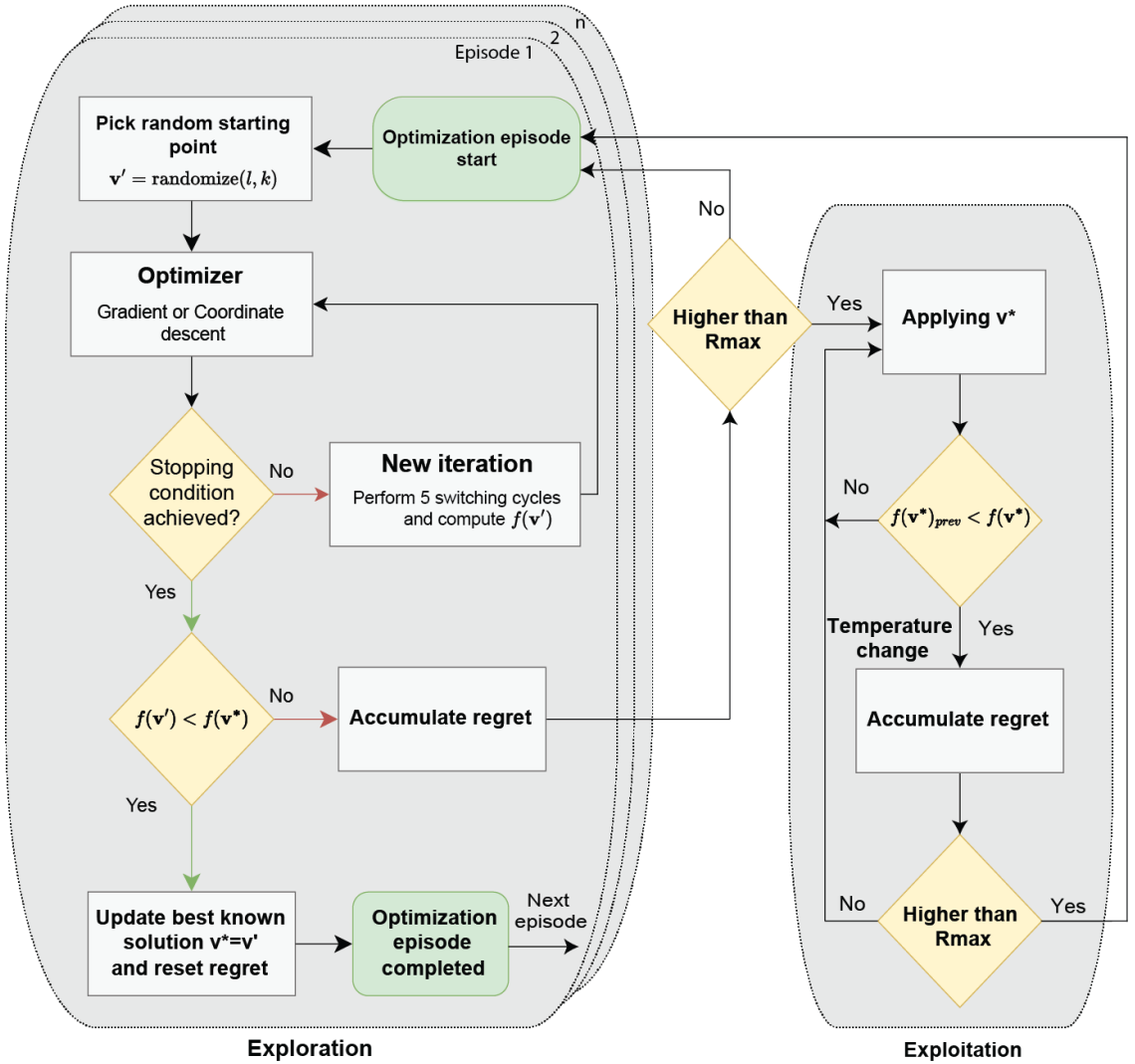
- Step 4) Repeat iteratively, until a local minimum is reached:

$$f(\mathbf{v}^{(t+1)}) \geq f(\mathbf{v}^{(t)})$$



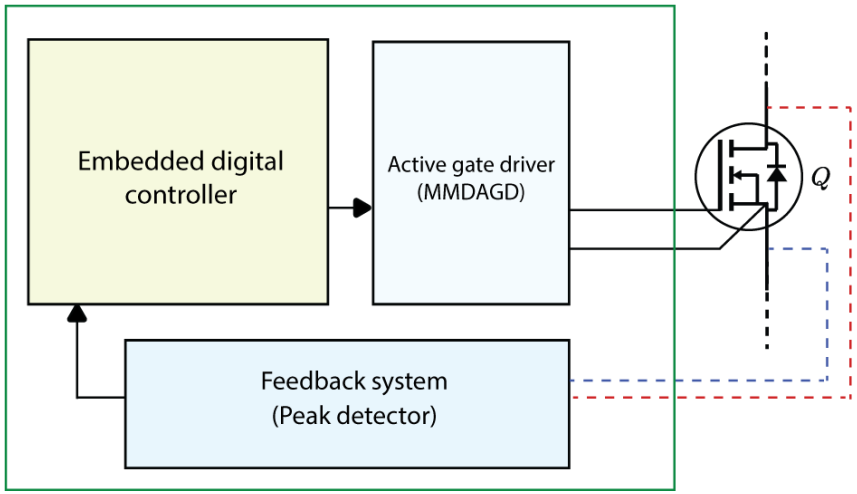


The waveform optimization algorithm: Full picture

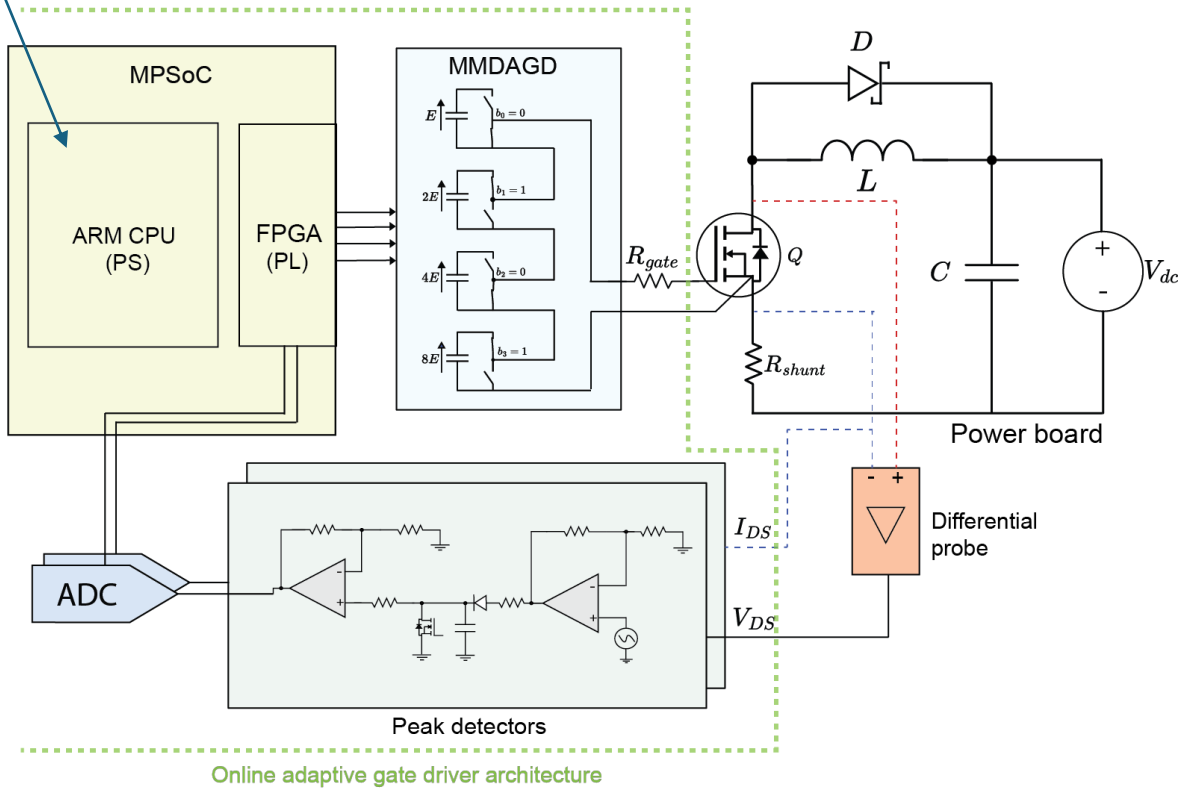


Hardware realization

The optimization algorithm runs on the CPU! FPGA is used to drive MMDAGD



Online adaptive gate driver architecture



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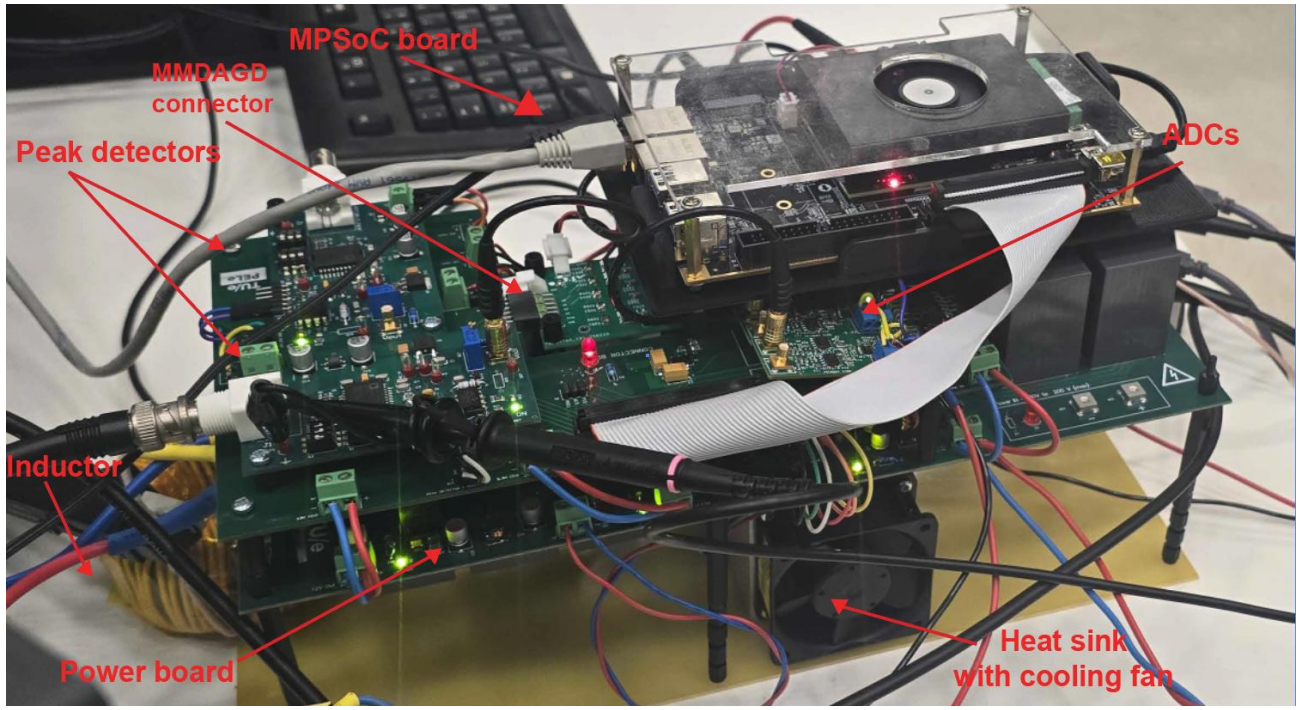
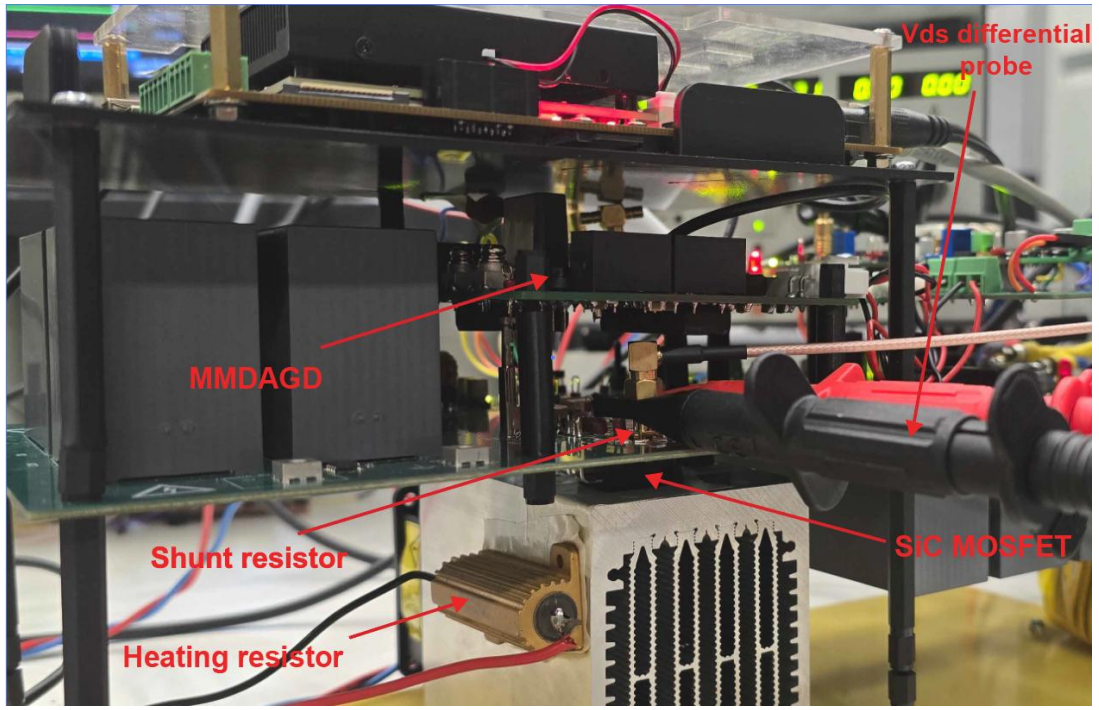
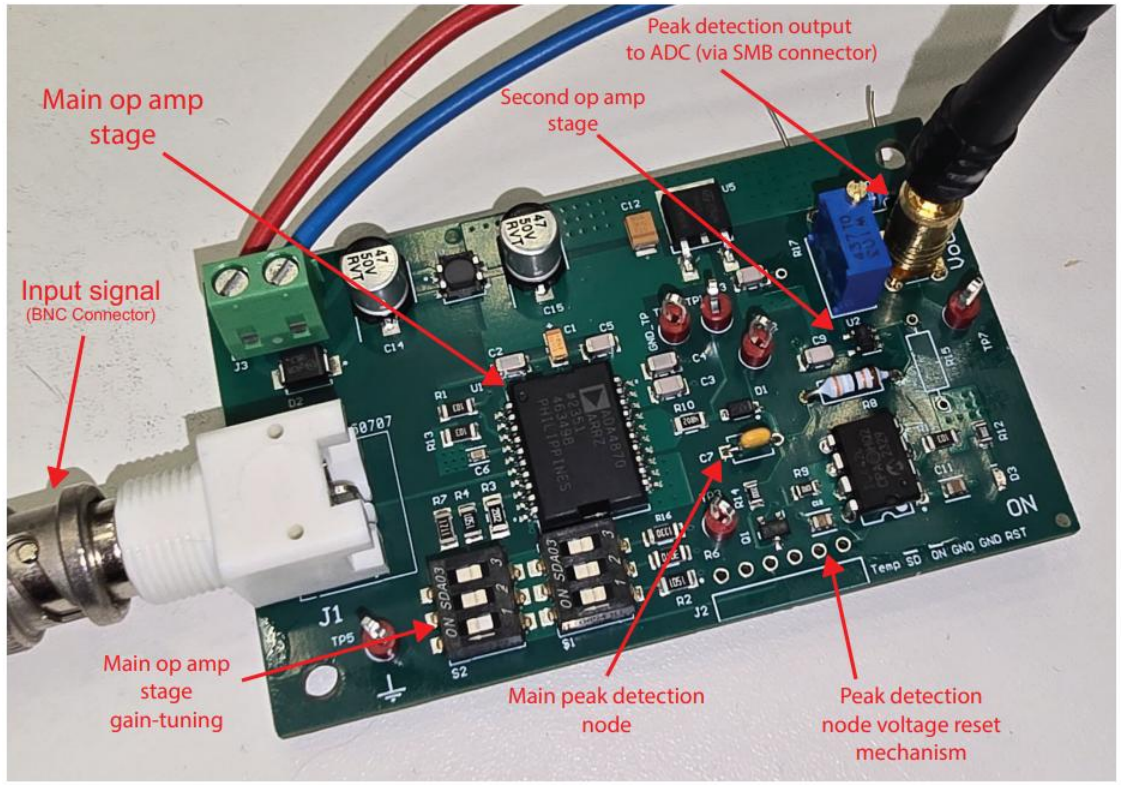


Front side

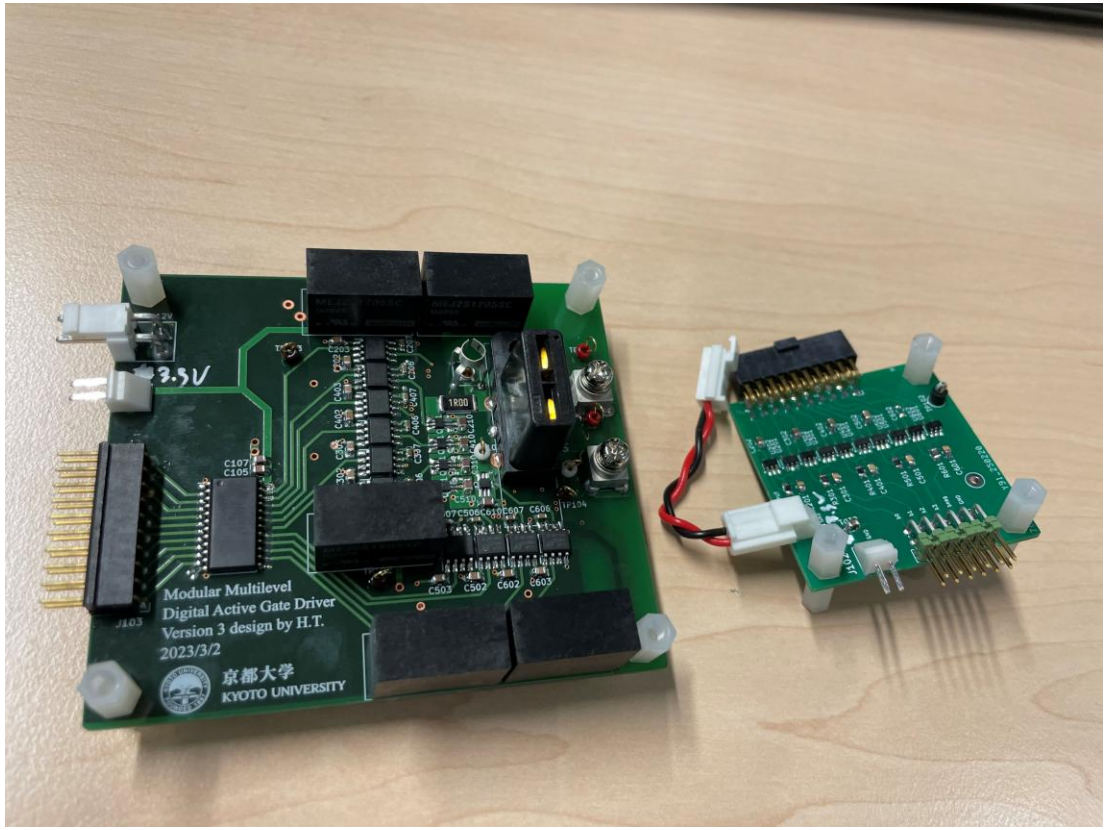


Back side

Peak detector realization



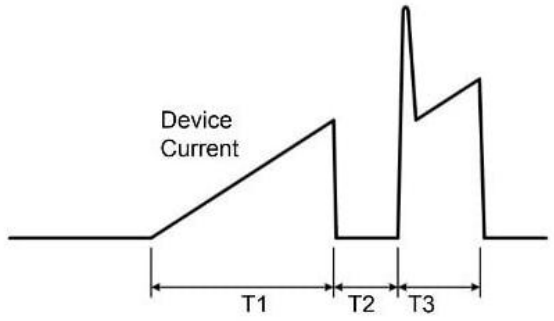
Hardware realization: MMDAGD

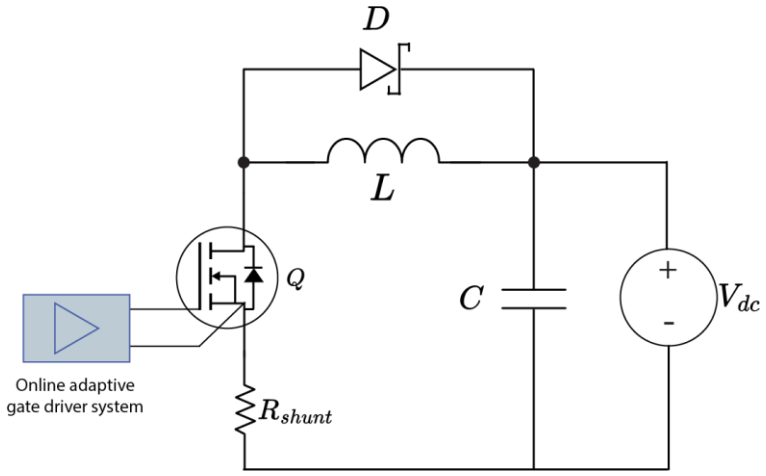


- 4-level MMDAGD prototype
- MMDAGD prototype by dr. Hajime Takayama

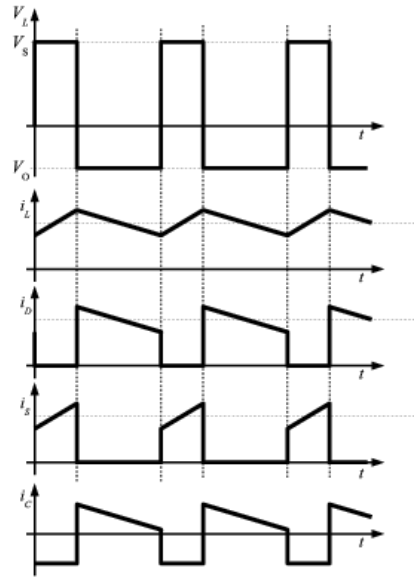
[1]: Takayama, H., Fukunaga, S. and Hikihara, T., 2023, September. Binary-weighted modular multi-level digital active gate driver. In 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe) (pp. 1-8). IEEE.

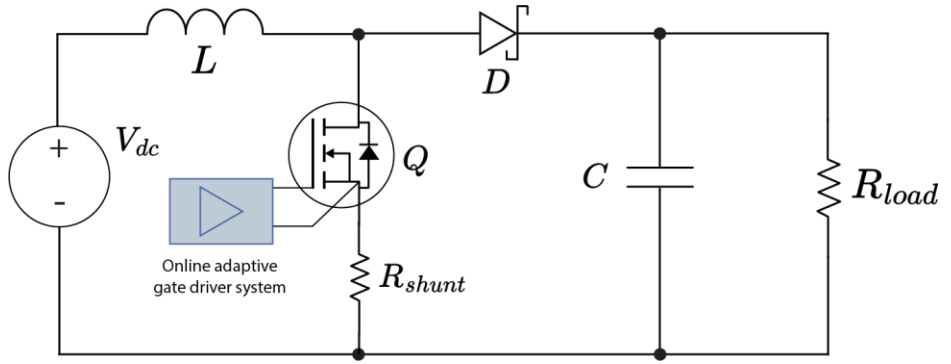
Double pulse test configuration





Boost configuration

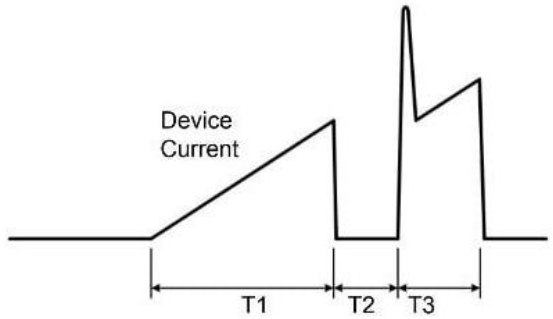


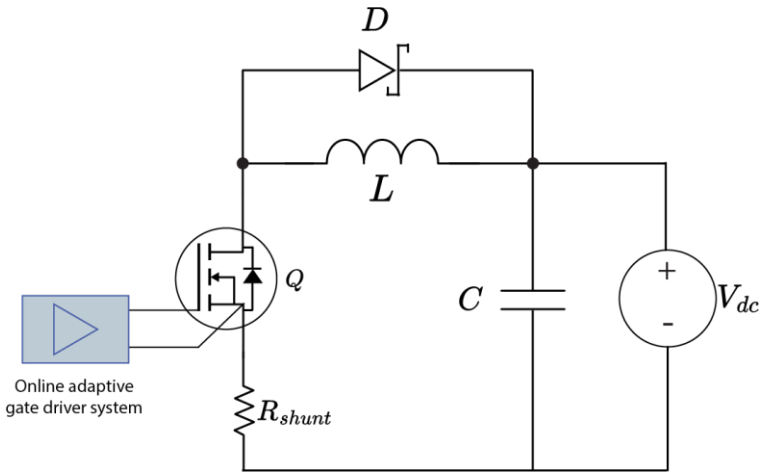


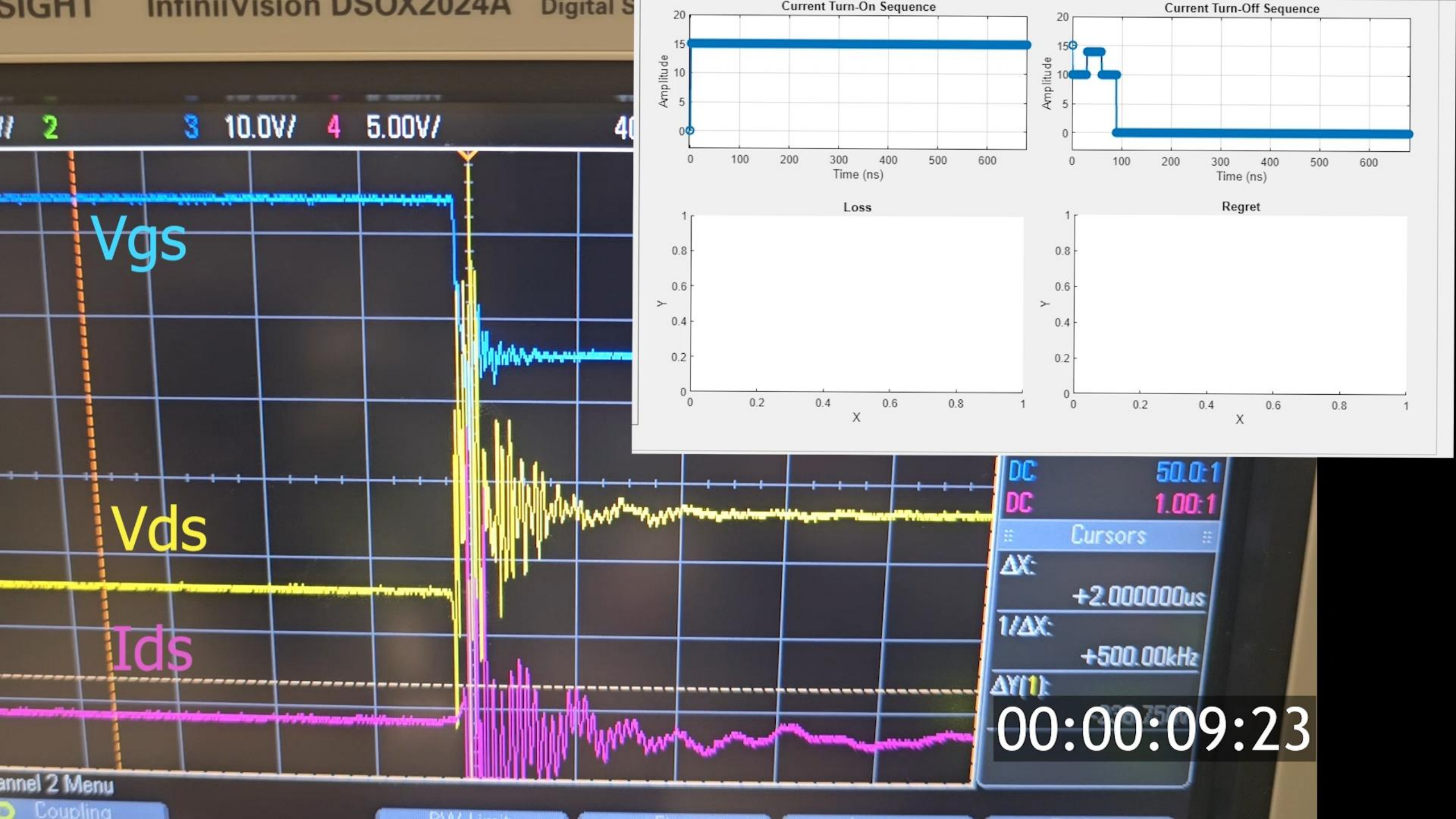
Experiment configuration:

- Coordinate descent as optimizer
- Maximum regret threshold 0.8
- Vdc = 80V
- Ids ~40 A (T1=400 us, T2=T3=20 us)
- 3 steps
- Step-duration: 30 ns

Double pulse test configuration






InfiniiVision DSOX2024A
10.0V/
5.00V/
Vgs
Vds
Ids
Current Turn-On Sequence
Current Turn-Off Sequence
Amplitude
Time (ns)
Loss
Regret
X
Y
DC 50.0:1
DC 1.00:1
Cursors
ΔX:
+2.000000us
1/ΔX:
+500.00kHz
ΔY(1):
00:00:09:23
Channel 2 Menu
Coupling

Power converter settings:

- $V_{DC} \approx 35V$
- $D = 0.5$
- $V_o \approx 70V$
- $P_o \approx 125\ W$
- $F_{sw} = 10\ kHz$

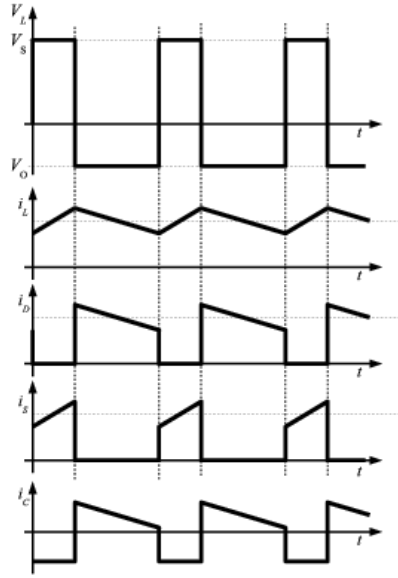
MMDAGD Settings:

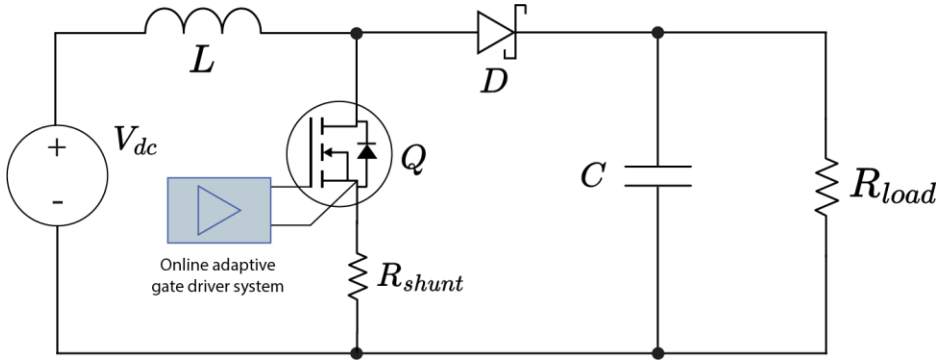
- k = 4 steps
- Step-duration: 20 ns

Algorithm settings:

- Max. regret = 1
- Coordinate-descent opt.

Boost configuration






1 50.0V/ 2 5.00A/ 3 10.0V/ 4 1.00V/
-250.0ns
100.0ns/
Trig'd
3
Vgs
Vds
IL
Ids
00:00:09:02
Acquisition
Normal
1.00GSa/s
Channels
DC 50
DC 10.0
DC 50.0
DC 1.00
Measurements
Top(2):
Low signal
Avg - FS(2):
5.22A
Avg - FS(3):
7.14V
Freq(3):

Power converter settings:

- $V_{DC} \approx 40V$
- $D = 0.5$
- $V_o \approx 80V$
- $P_o \approx 150\ W$
- $F_{sw} = 20\ kHz$

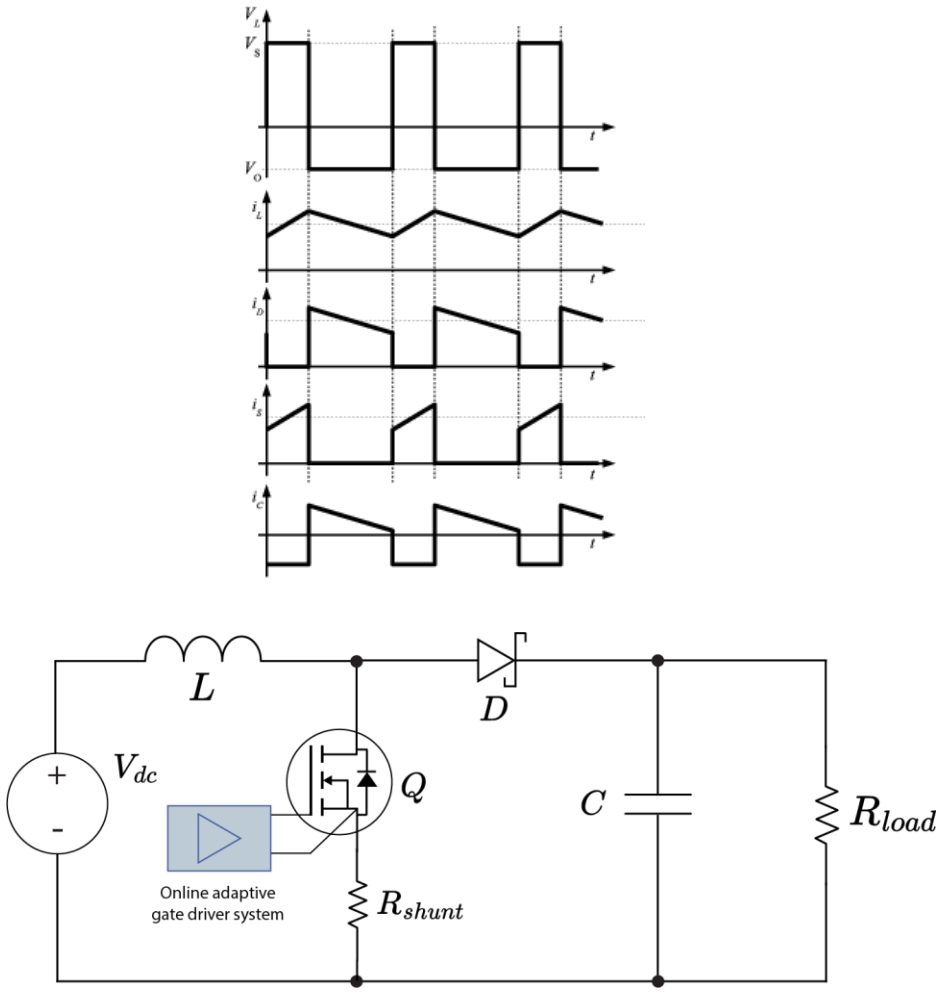
MMDAGD Settings:

- k = 3 steps
- Step-duration: 30 ns

Algorithm settings:

- Max. regret = 1
- Gradient descent

Boost configuration




Vgs
Vds
IL
IDS
DC
DC
DC
DC
Top(2):
Avg - FS(2
Avg - FS(3):
00:00:00:00
Sprache, Langue, Idioma, Lingua, 语言, Language

Power converter settings:

- $V_{DC} \approx 40V$
- $D = 0.5$
- $V_o \approx 80V$
- $F_{sw} = 10\ kHz$

MMDAGD Settings:

- k = 3 steps
- Step-duration: 30 ns

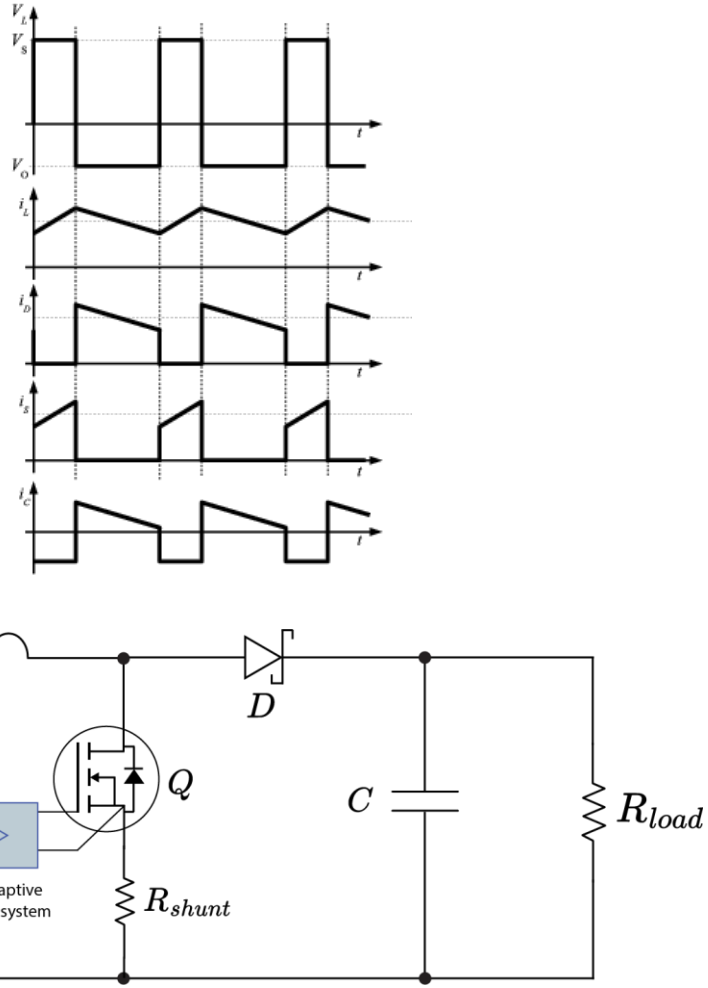
Algorithm settings:

- Max. regret = 2
- Coordinate descent

Experiment sequence:

Increase the load such that current flowing through inductor goes from 2.5A to 3.5A

Boost configuration




Digital Storage Oscilloscope
200 MHz
2 GSa/s
50.0V/ 2 5.00A/ 3 10.0V/ 4 1.00V/
-224.8ns
200.0ns/
Trig'd
3
Vgs
Vds
Ids
IL
00:00:27:06
Acquisition
Normal
1.00GSa/s
Channels
DC 500:1
DC 10.0:1
DC 50.0:1
DC 1.00:1
Measurements
Top(2):
Low signal
Avg - FS(2):
3.498A
Avg - FS(3):
5.99V

Experiment configuration

Power converter settings:

- $V_{DC} \approx 40V$
- $D = 0.5$
- $V_o \approx 80V$
- $F_{sw} = 10\ kHz$

MMDAGD Settings:

- k = 3 steps
- Step-duration: 30 ns

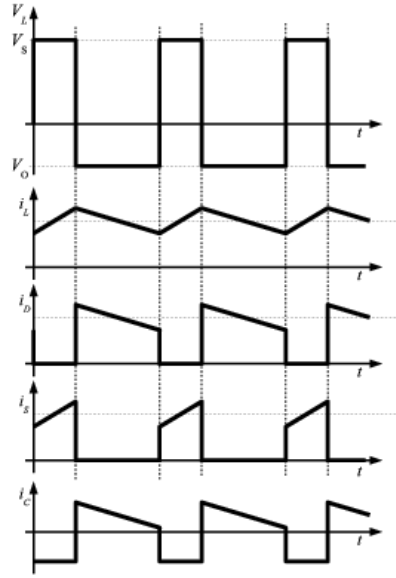
Algorithm settings:

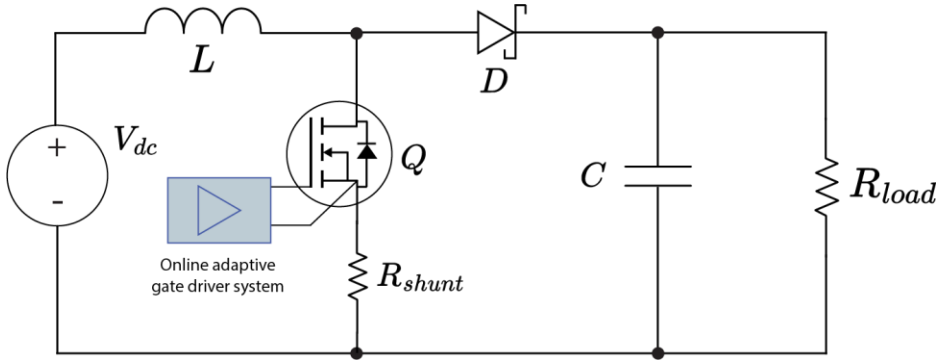
- Max. regret = 1
- Coordinate descent

Experiment sequence:

Heat the device from room temperature (24°C to 105°C), while operating as a boost converter, to observe how the online adaptive gate driver reacts.

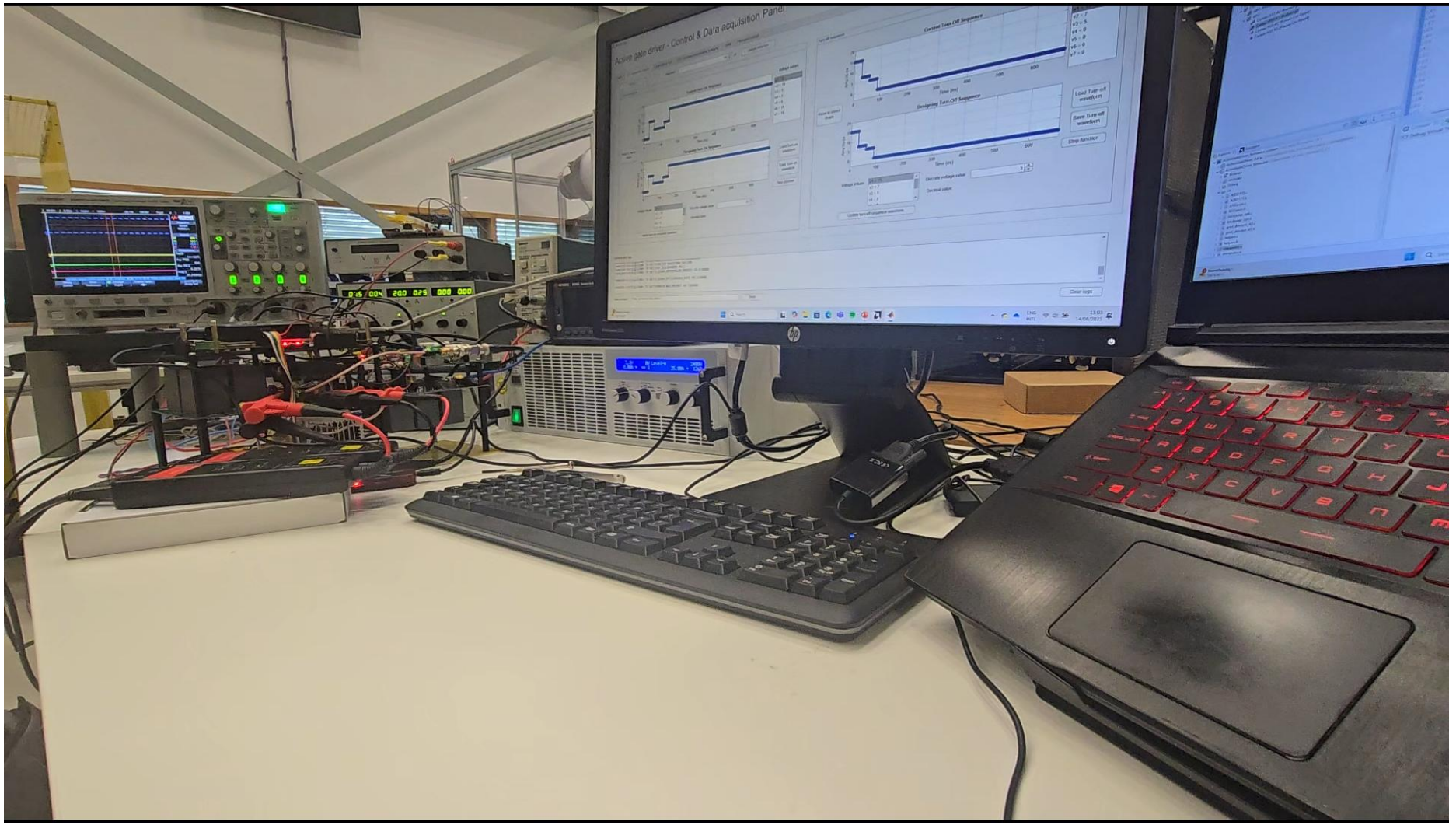
Boost configuration






Trig'd
3
KEYSIG
TECHNOLO
Acquisition
Normal
1.00GSa/s
Channels
DC
DC
DC
DC
Measurements
Top(2):
Low signa
Avg - FS(2):
4.30A
Avg - FS(3):
Vgs
Vds
IL
00:00:00:00

Now lets apply optimized Vgs profile to my converter (at 200V output)



Thank you for your attention!

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