



# D&E

*Hoe wordt uw leven als System Engineer eenvoudiger ?*



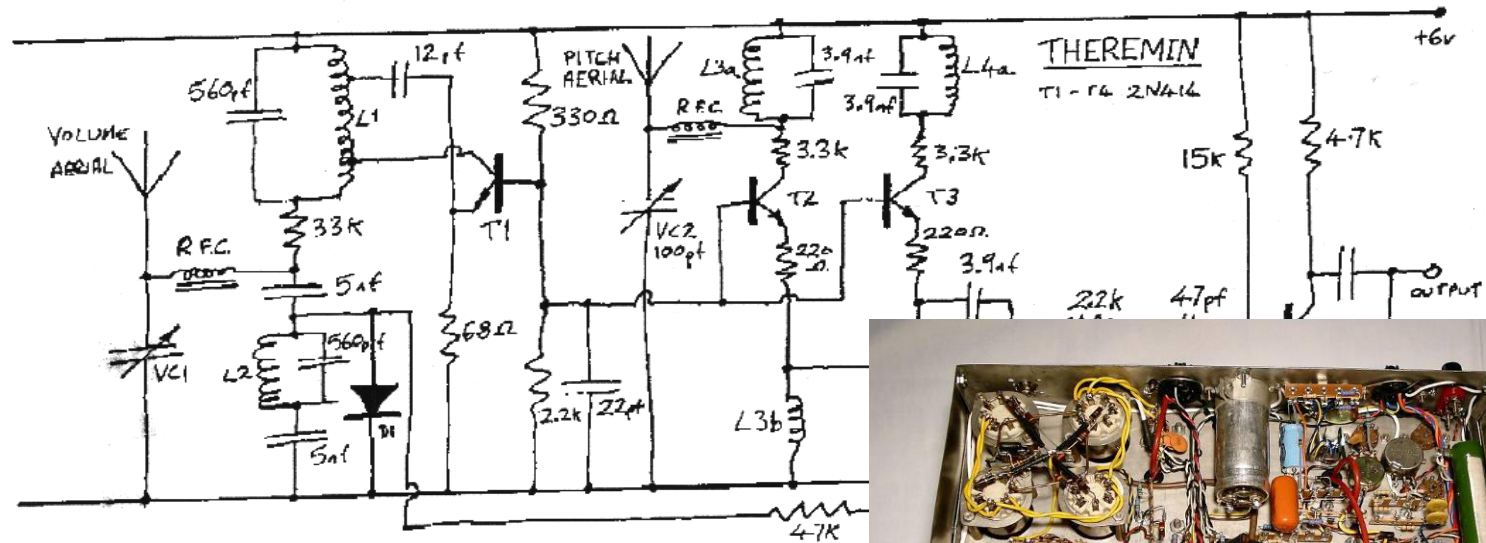
Ruben Smits  
Transfer BV

# Lets meet...



- Joe Designer
- Electronic engineer for a medium sized company

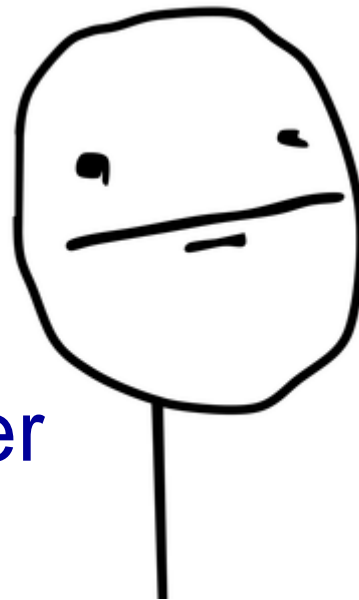
# Where it all begins...



# But there is more...

- MCAD Engineer

- Database Manager



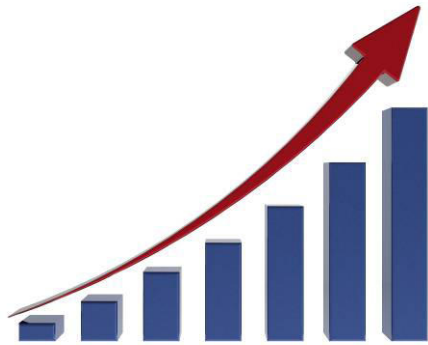
- Purchase Manager

- Test Engineer

- Repair Engineer

# Typical Organizational Pain Points...

**Time To Revenue**



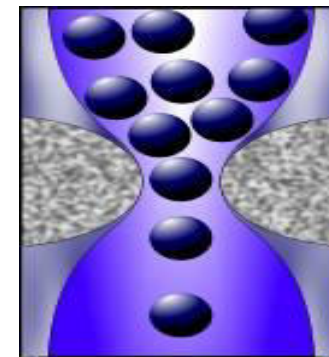
**Collaboration**



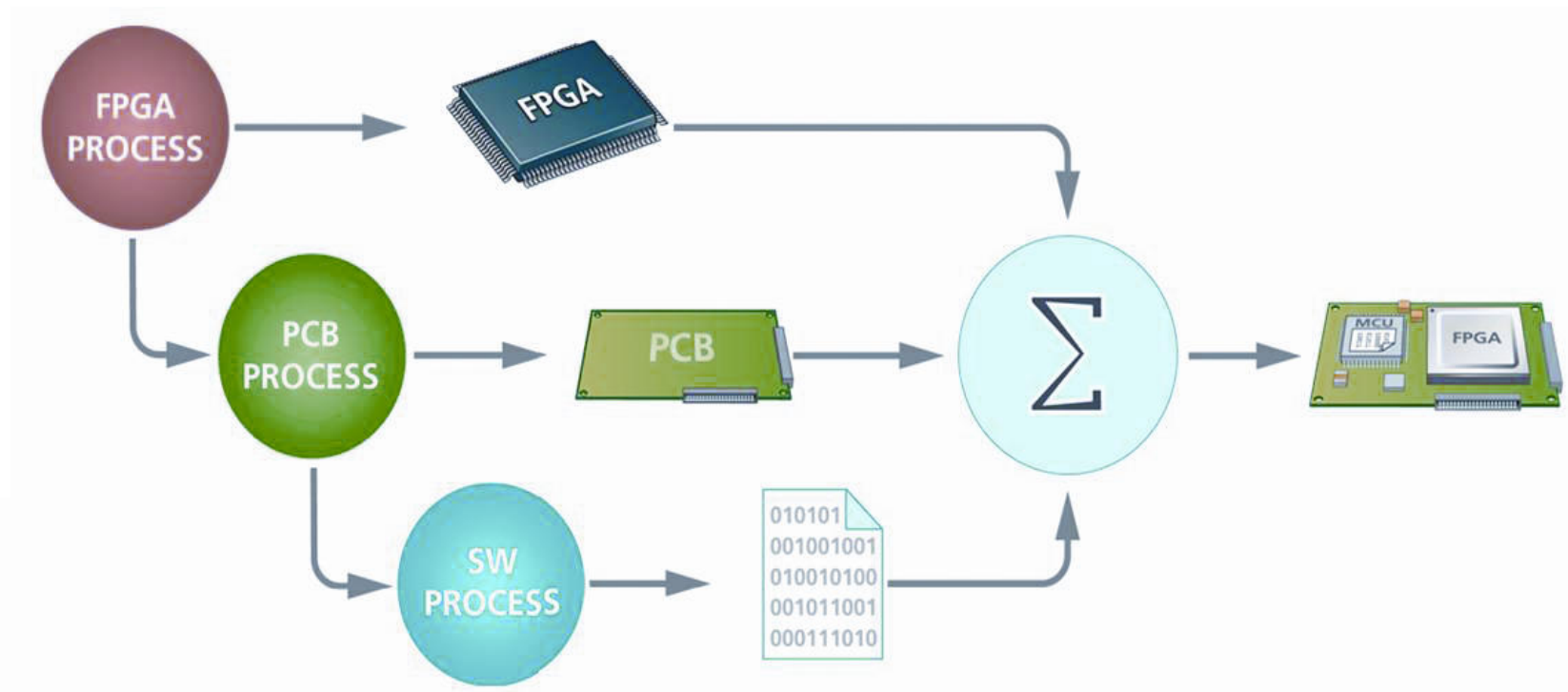
**Differentiation**



**Process Bottleneck**

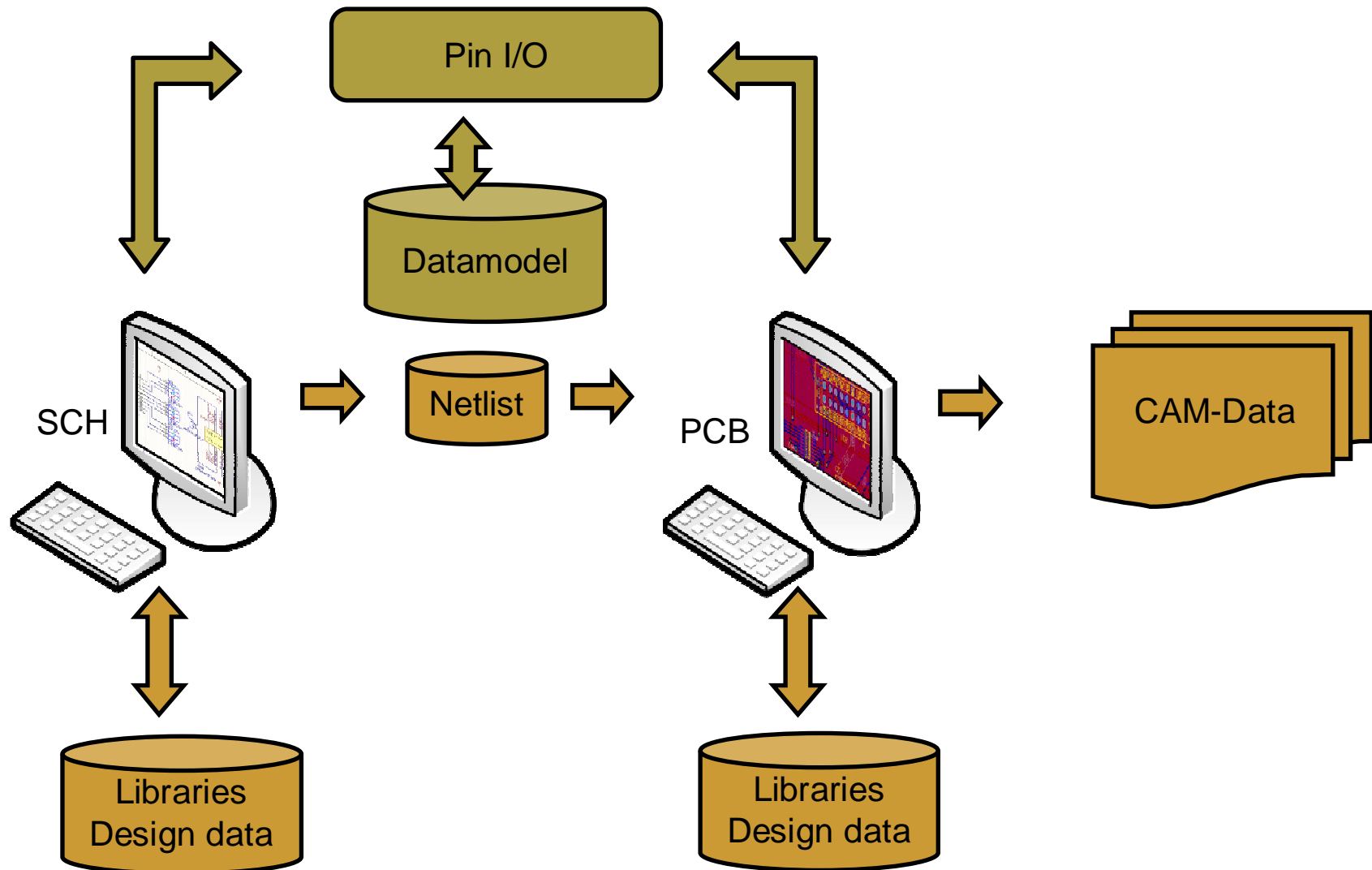


# What needs to be designed?



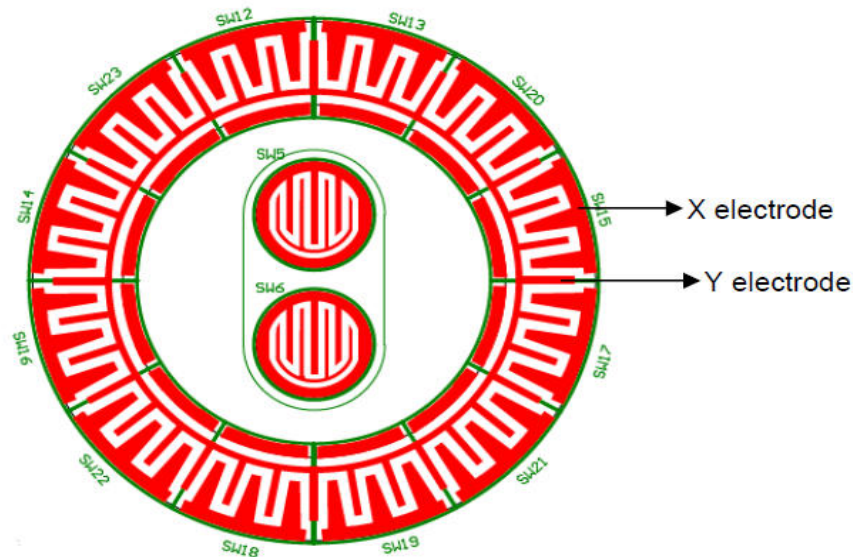


# Additional tools for communication



# Designing Capacitive Touch Footprints

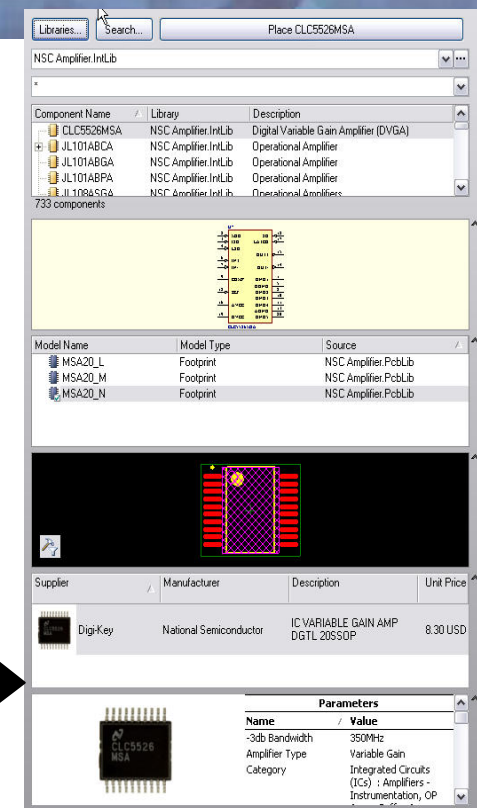
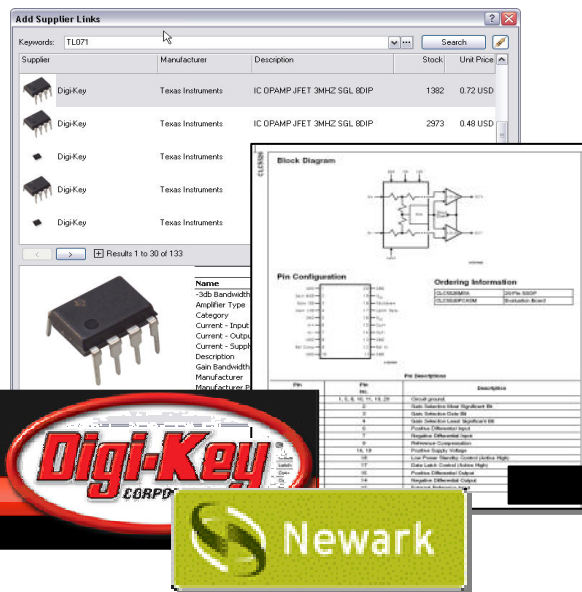
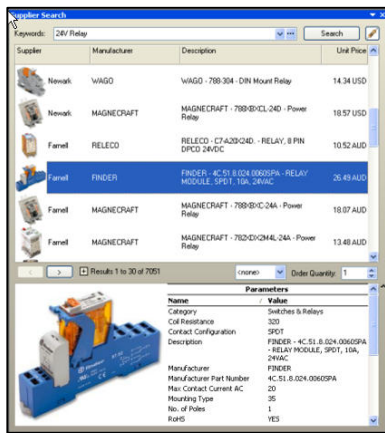
- Traditionally, any changes on this complex footprint will cause a complete redesign.





# Component & Library Management

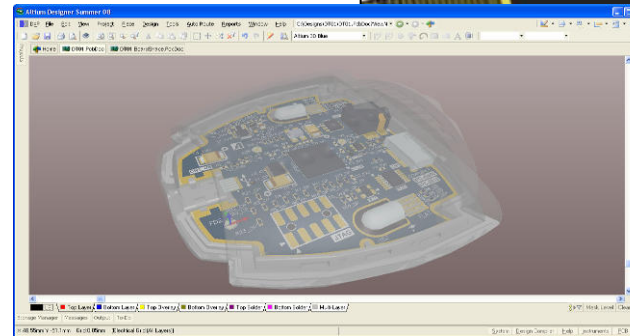
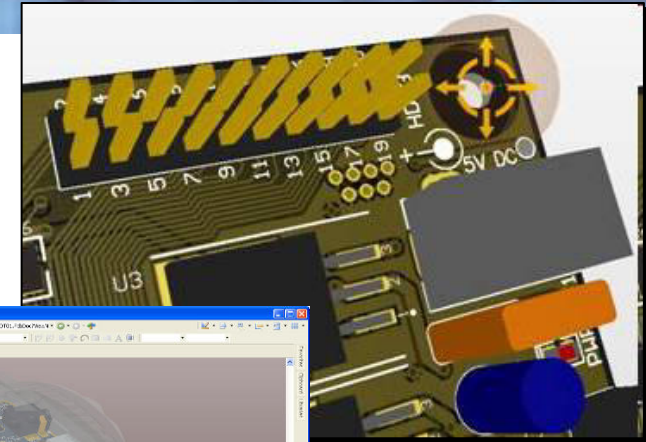
- Component starter library
- Component information link to Newark & Digi-Key
- Component versioning
- IPC Footprint wizard
- 3D STEP models



90% of board cost is determined by the component selection!  
Is your library easily managed and replicated?  
Are you considering ECAD / MCAD 3D fit checks?

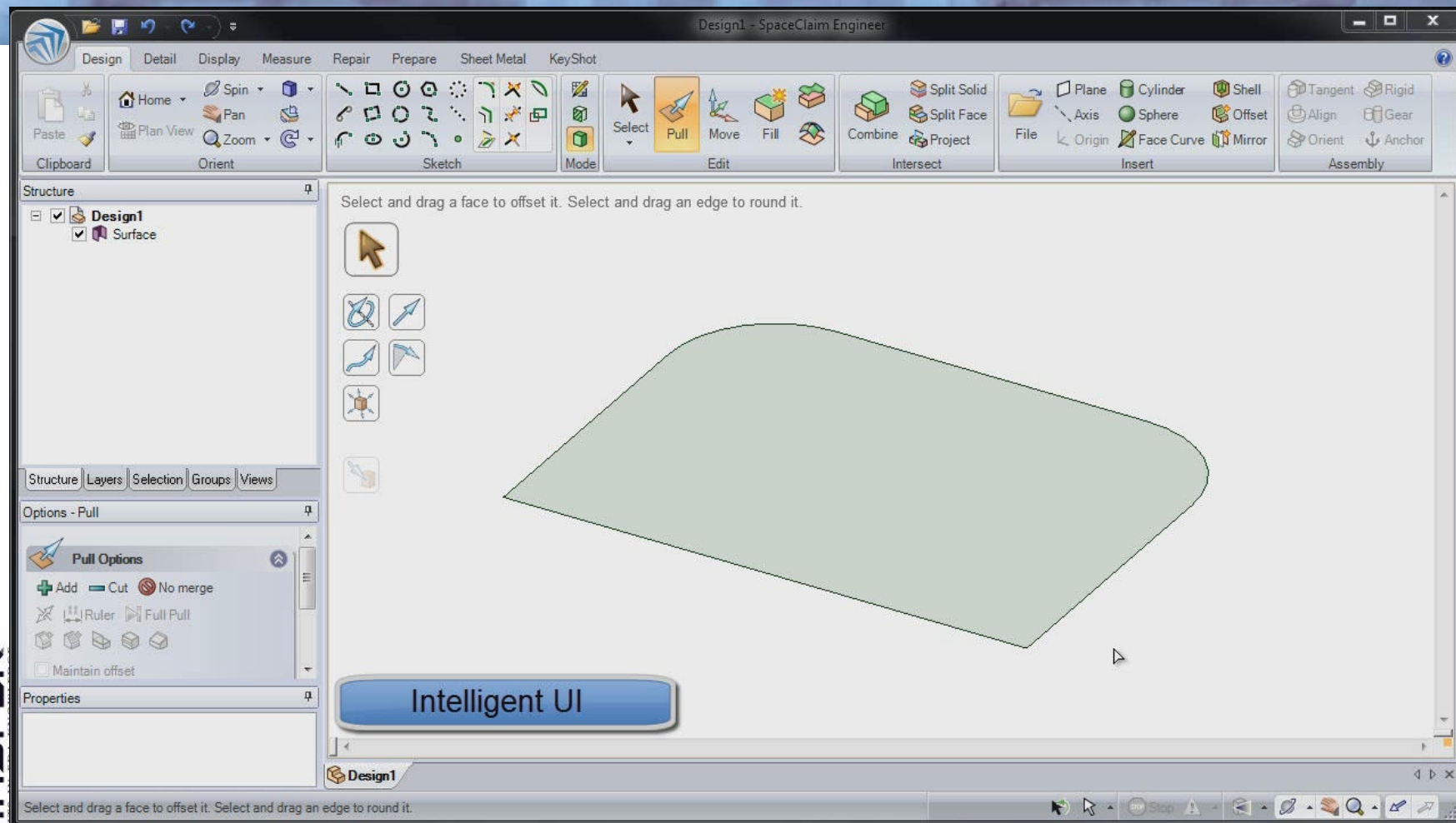
# ECAD / MCAD 3D Integration

- 3D PCB layout environment
  - Dynamic 3D
  - Critical Part 3D Placement
- Full STEP model support
- Basic 3D model creation
  - Extrusion
- MCAD tool support
  - PTC
  - Solidworks
- MCAD clearance checking
- Full assembly STEP export



Have you had PCB fit problems?  
Does your system support the STEP standard?  
How do you do ECAD/MCAD fit checks today?

# MCAD Made Easy...



# Concentrate on your Secret Sauce

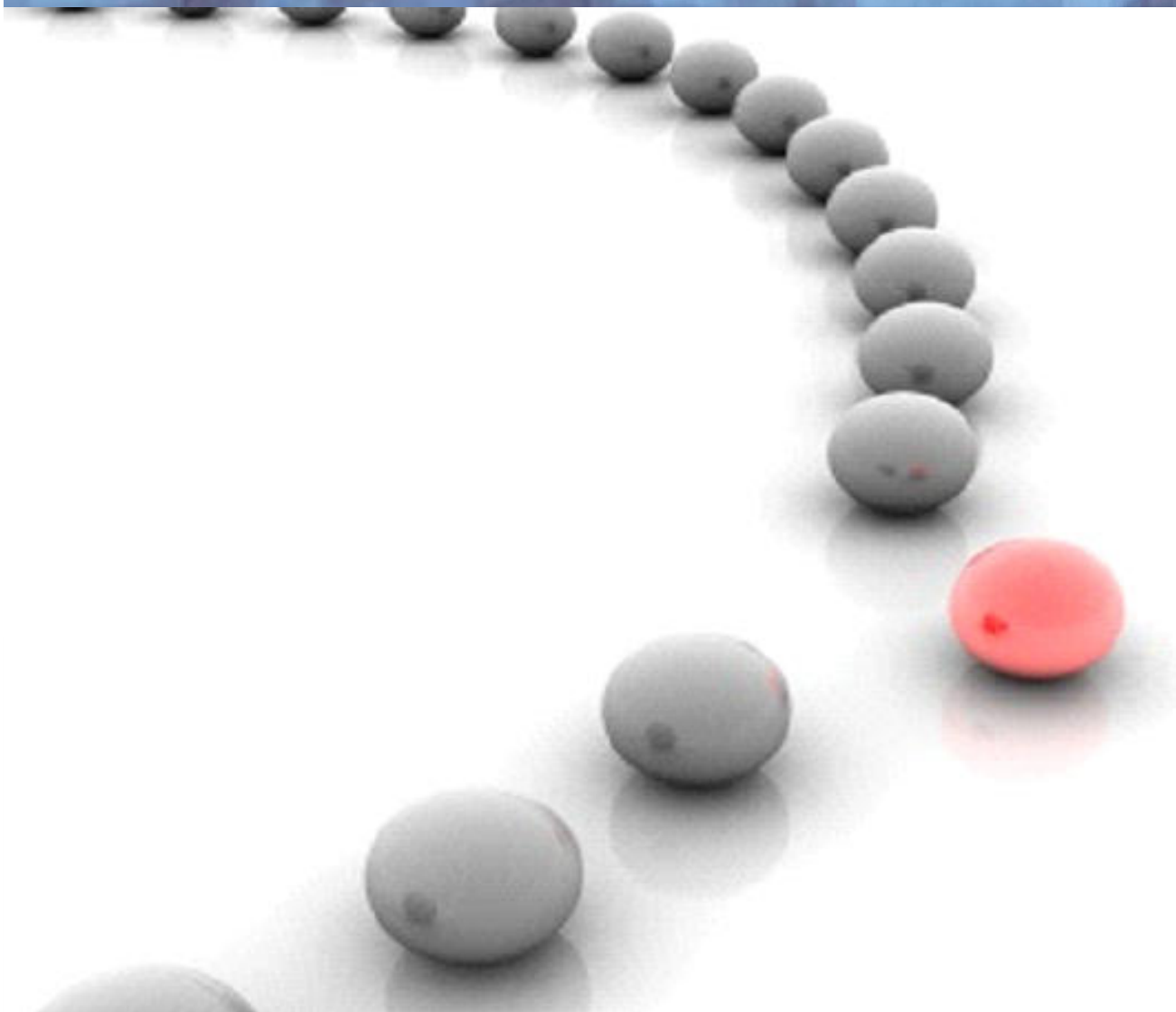
Internet

Serial Communications

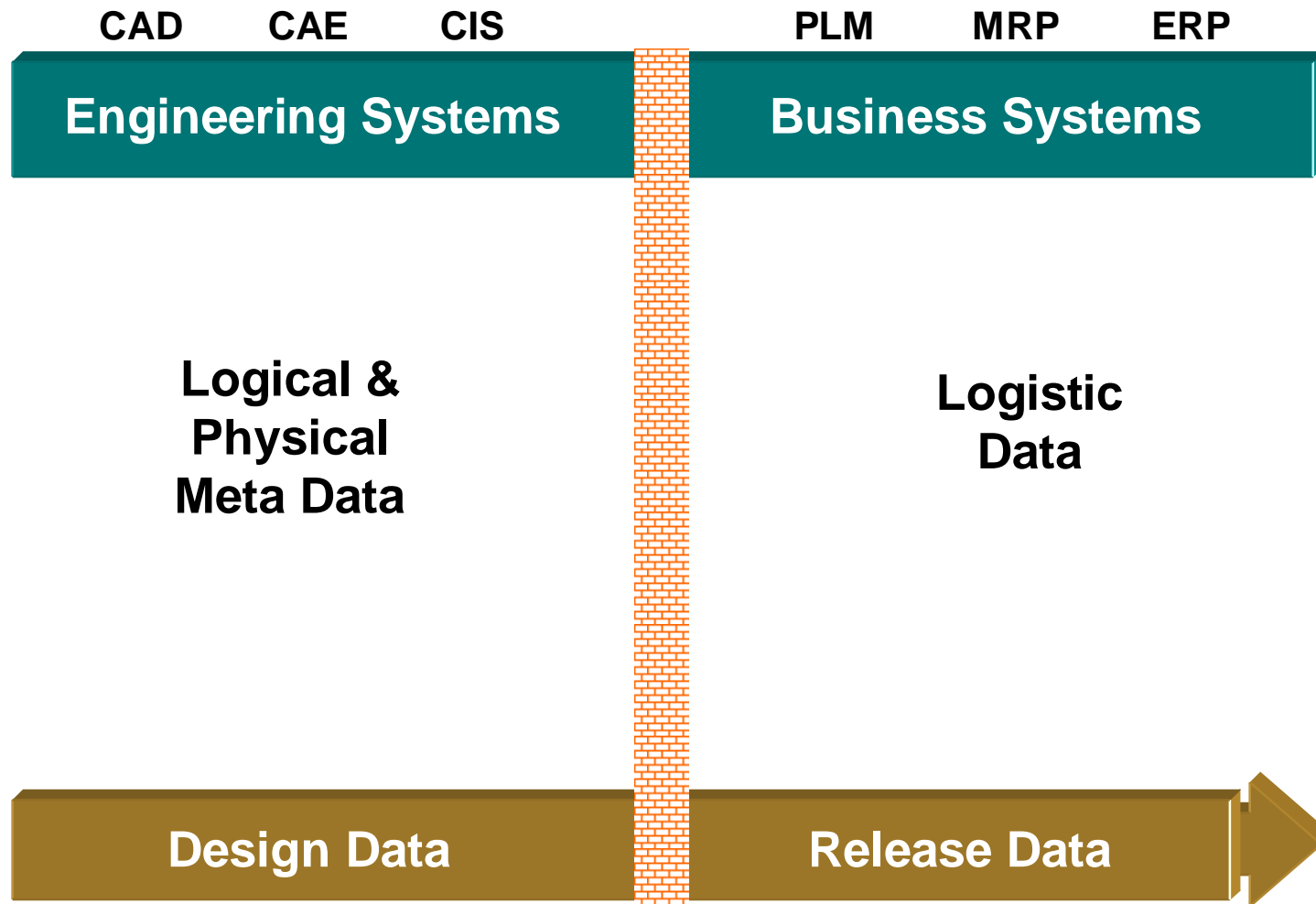
Touch Screen

| 1

***SOFTWARE***

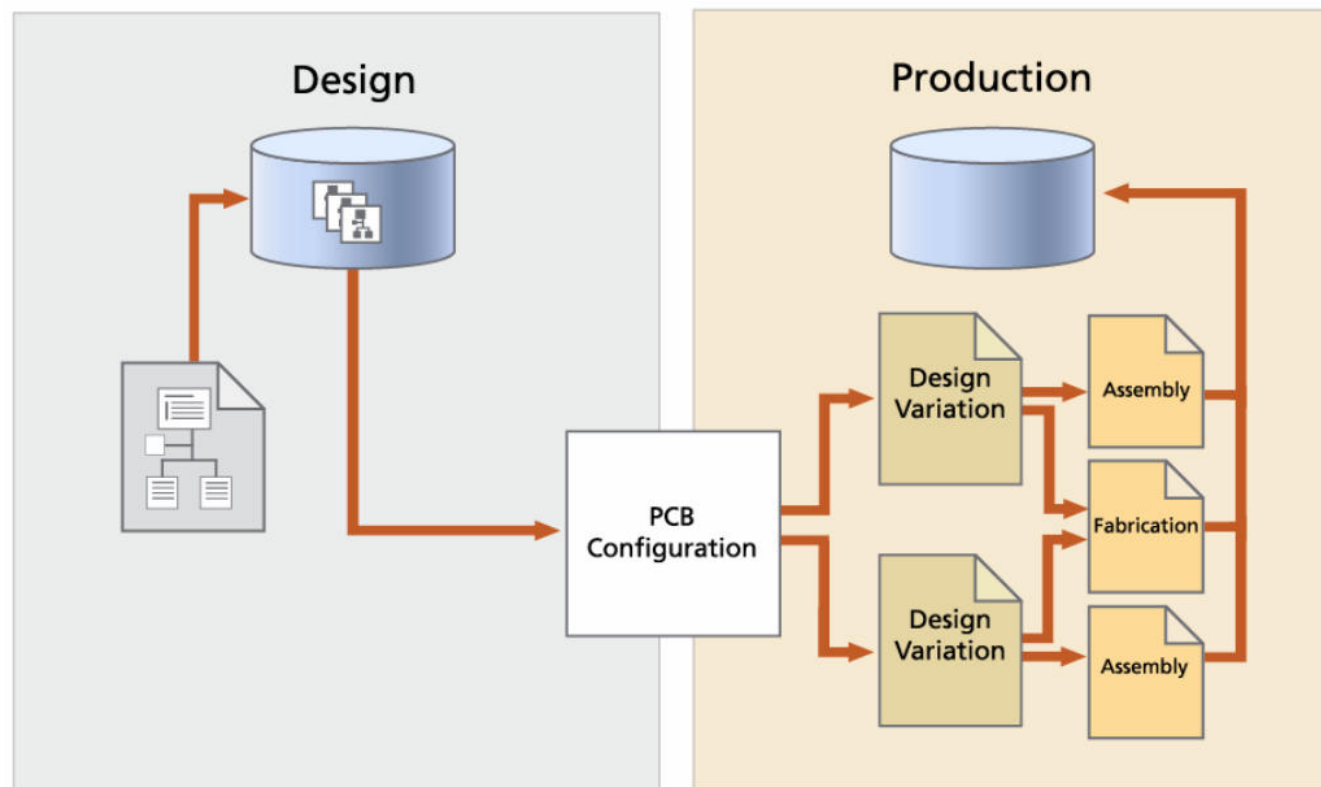


# Positioning E-CAD





# Release To Production



# Project Release Management

- When a particular configuration for a project is released, a snapshot of the design source is taken, validated and archived along with any generated output

Altium Designer Release 10 (Beta Build 19878) - Workgroup [Workspace1.DsnWrk] - Released - Free Documents. Licensed to Altium Limited - Do not use. Nick Martin signed in.

Released

Item: D-820-0006

Timeline (Show All)

Revision	State	Date-Time
01.A.1	In Design	10-Apr-09 16:21
01.A.2	In Design	12-Apr-09 15:27
01.A.3	In Design	13-Apr-09 17:27
01.A.4	In Design	14-Apr-09 13:27
01.A.5	In Design	14-Apr-09 17:27
01.A.5	In Prototype	15-Apr-09 11:32
01.B.1 (Prototype)	In Design	21-Apr-09 13:34
01.A.5	Closed Prototype	21-Apr-09 16:57
01.B.2	In Design	22-Apr-09 07:53
01.B.2	In Prototype	28-Apr-09 16:19
01.B.2	Closed Prototype	30-May-09 09:19
01.C.1 (Prototype)	In Design	30-May-09 13:34
01.C.1	In Prototype	02-Jun-09 16:19
01.C.1	Closed Prototype	14-Jun-09 09:19
01.D.1 (Prototype)	In Design	16-Jun-09 13:34
01.D.2	In Design	16-Jun-09 16:34
01.D.3	In Design	17-Jun-09 21:28
01.D.3	In Prototype	18-Jun-09 16:19
01.D.3	In Production	27-Jun-09 09:19
02.A.1 (Model)	In Design	28-Jun-09 10:32
02.A.2	In Design	28-Jun-09 11:53
02.A.3	In Design	29-Jun-09 13:53
02.A.4	In Design	30-Jun-09 15:01
02.A.5	In Design	02-Jul-09 13:53
02.A.5	In Prototype	04-Jul-09 11:37
02.A.5	Closed Prototype	18-Jul-09 11:37
02.B.1 (Prototype)	In Design	19-Jul-09 10:32
02.B.2	In Design	20-Jul-09 11:53
02.B.2	In Prototype	21-Jul-09 08:21
02.B.2	In Production	19-Aug-09 09:19
01.D.3	Deprecated	20-Aug-09 09:47
01.D.3	Obsolete	18-Sep-09 17:59
03.A.1 (Model)	In Design	18-Oct-09 11:22
03.A.2	In Design	21-Oct-09 14:57
03.A.2	In Prototype	23-Oct-09 18:37
03.A.2	In Production	27-Nov-09 09:21
02.B.2	Deprecated	28-Nov-09 09:47
02.B.2	Obsolete	29-Dec-09 17:59
01.C.1	In Prototype	26-Apr-10 18:03

Model 01  
Obsolete

Prototype 01.A	Prototype 01.B	Prototype 01.C	Prototype 01.D
Rev. 01.A.1 In Design 10-Apr-09 16:21	Rev. 01.B.1 In Design 21-Apr-09 13:34	Rev. 01.C.1 In Design 30-May-09 13:34	Rev. 01.D.3 Obsolete 18-Sep-09 17:59
Rev. 01.A.2 In Design 12-Apr-09 15:27	Rev. 01.B.2 In Design 22-Apr-09 07:53	In Prototype 02-Jun-09 16:19	
Rev. 01.A.3 In Design 13-Apr-09 17:27	In Prototype 28-Apr-09 16:19	In Prototype 26-Apr-10 18:03	
Rev. 01.A.4 In Design 14-Apr-09 13:27	Closed Prototype 30-May-09 09:19		
Rev. 01.A.5 In Design 14-Apr-09 17:27			

Model 02  
Obsolete

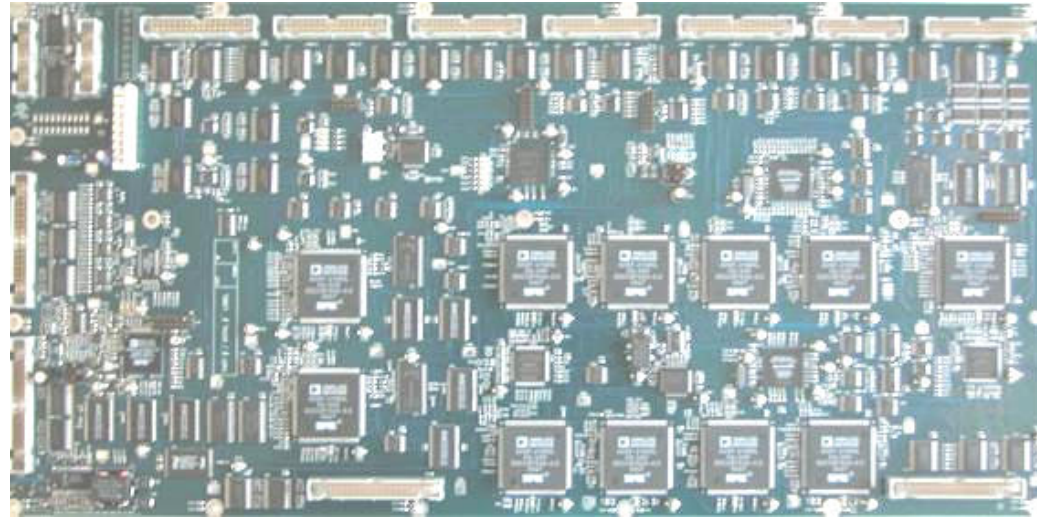
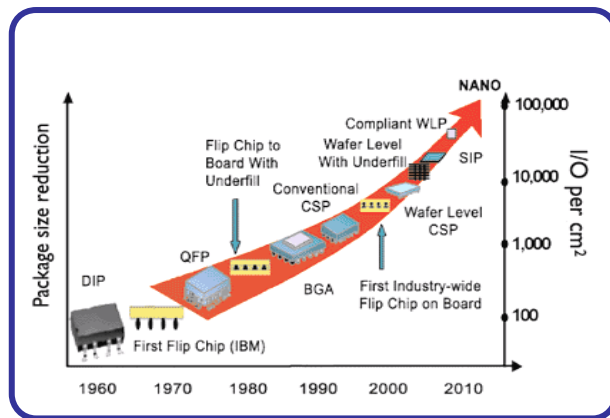
Prototype 02.A	Prototype 02.B
Rev. 02.A.1 In Design 28-Jun-09 10:32	Rev. 02.B.1 In Design 19-Jul-09 10:32
Rev. 02.A.2 In Design 28-Jun-09 11:53	Rev. 02.B.2 In Design 20-Jul-09 11:53
Rev. 02.A.3 In Design 29-Jun-09 13:53	In Prototype 21-Jul-09 08:21
Rev. 02.A.4 In Design 30-Jun-09 15:01	Deprecated 28-Nov-09 09:47
	Obsolete 29-Dec-09 17:59
Rev. 02.A.5 In Design 02-Jul-09 13:53	
In Prototype 04-Jul-09 11:37	
Closed Prototype 18-Jul-09 11:37	

Model 03  
In Production

Prototype 03.A
Rev. 03.A.1 In Design 18-Oct-09 11:22
Rev. 03.A.2 In Design 21-Oct-09 14:57
In Prototype 23-Oct-09 18:37
In Production 27-Nov-09 09:21

System | Design Compiler | E-DesignData | Help | Instruments | >>

# Design Testability



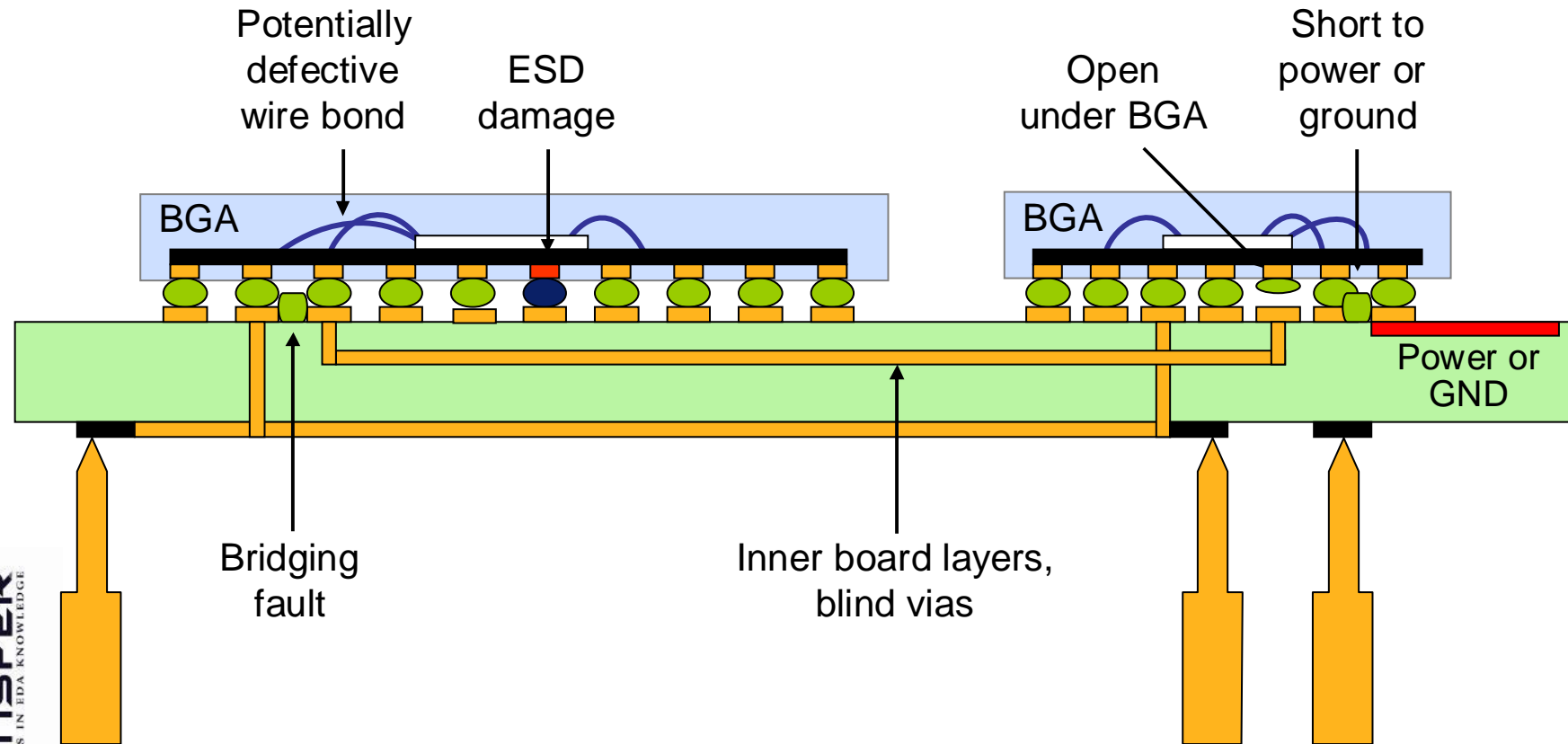
**Find the failures before your customers do!**

**More than 90% of the PCBs produced will contain at least one structural fault**

Ref: Charles Robinson and Amit Verma, Teradyne Inc., APEX 2002

# Design Testability

**In-circuit testing will have difficulty finding these types of faults**

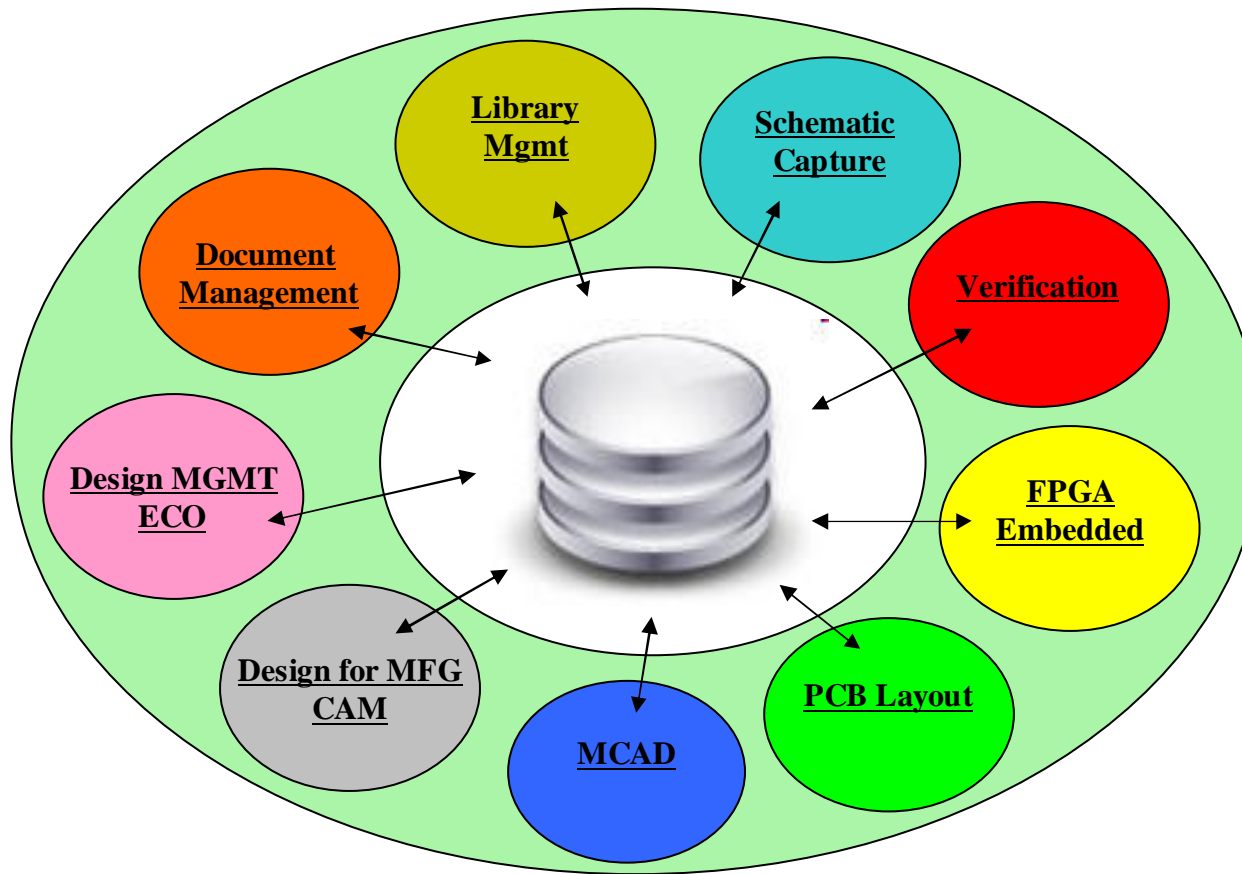


# The traditional approach...





# ONE single Data Model



# Unified Design

The screenshot displays the Altium Designer Summer 09 interface, illustrating a unified design workflow for an FPGA project. The main workspace shows a PCB layout of the Xilinx Spartan-IE PQ208 Rev1.01. The left panel features the 'XC2S300E-6PQ208C Pin States on JTAG 0' window, listing pin configurations for BANK 4, including I/O (DLL, L31F, L30N, L29N, L28N, L27N) and LEDs (7, 6, 5, 4, 3, 2, 1, 0). The right panel shows the 'SL\_FPGA\_Complete.SchDoc' window, displaying a VHDL code snippet for 'vhd1' and 'HDL.Vhd', including a 'Trig' signal and a 'W[7..0]' output. The bottom panel shows the 'Instrument Rack - Soft Devices' window, which includes a 'REQUEST FREQUENCY' table, a 'CORE U7 (CLKGEN)' section, and a 'CORE U8 (LAY8)' section. The 'REQUEST FREQUENCY' table shows a running frequency of 5 Hz. The 'CORE U7 (CLKGEN)' section shows a running frequency of 5 Hz. The 'CORE U8 (LAY8)' section shows a running frequency of 5 Hz. The bottom right corner shows a waveform viewer with a digital signal trace. The bottom status bar indicates the project is 'XC2S300E-6PQ208C Pin States on JTAG 0' and the design is 'System Design Compiler Instruments Help LAX-U8 VHDL PCB'.

Altium Designer Summer 09 - D:\Demo\Unified Design\SL1 Xilinx Spartan-IE PQ208 Rev1.01.PcbDoc - Unified Design.PrjPcb. Licensed to Altium Limited - Do not use. Not signed in.

XC2S300E-6PQ208C Pin States on JTAG 0

FPGA Project Top Level Document BSDL Information

PCB Project And Component Link Rebuild Links

BANK 4

I/O (DLL), L31F  
I/O, L30N  
I/O, VREF 4, L30F  
I/O, L29N  
I/O, L28N  
I/O, L27N  
I/O, VREF 4, L27F  
LEDS(7)  
LEDS(6)  
LEDS(5)  
LEDS(4)  
LEDS(3)  
LEDS(2)  
LEDS(1)  
LEDS(0)

SL\_FPGA\_Complete.SchDoc

vhd1  
HDL.Vhd

Trig  
W[7..0]  
LED[7..0]  
t  
TTY: ledflashvhd1

0040

Instrument Rack - Soft Devices

JTAG 1.1 CORE U7 (CLKGEN)

REQUEST FREQUENCY

50	20	10	5	1	Baud Rates	Other Frequency
500	250	200	100	50	25	10
500	250	200	100	50	25	10
500	250	200	100	50	25	10

Set Time Base 150 MHz Run Options Invert

Running

5 Hz

Instrument Title

ARM RUNNING Options

DATA VIEWS

ANALOG Show Waves Show Panel

DIGITAL Show Waves 8-Channel Logic Analyzer

Inputs

9[7..0]  
08  
108  
101

Outputs

Synchronize Digital I/O Module

Instrument Rack - Hard Devices

0 -CLK 1

1 Group: LED\_LAX[7:0] 02

2 LED\_LAX[7] 0

3 LED\_LAX[6] 0

4 LED\_LAX[5] 0

Update Auto Install Component Library

XC2S300E-6PQ208C Pin States on JTAG 0

Messages

X:103mm Y:23.5mm Grid:0.1mm (Electrical Grid)

System Design Compiler Instruments Help LAX-U8 VHDL PCB

Start

Posteingang - Micros... D:\Presento\FED Con... Album Designer Sum... Microsoft PowerPoint...

NVIDIA Systemsteuer... Live! Cam Center

17:18 Freitag 25.09.2009

# Thank You!

- Questions?

