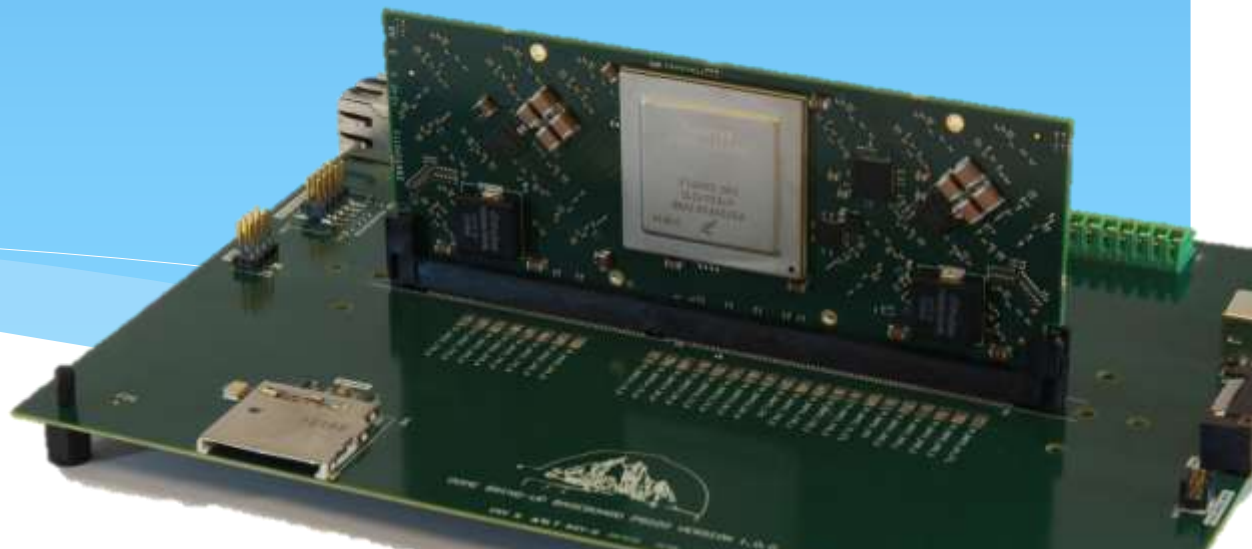
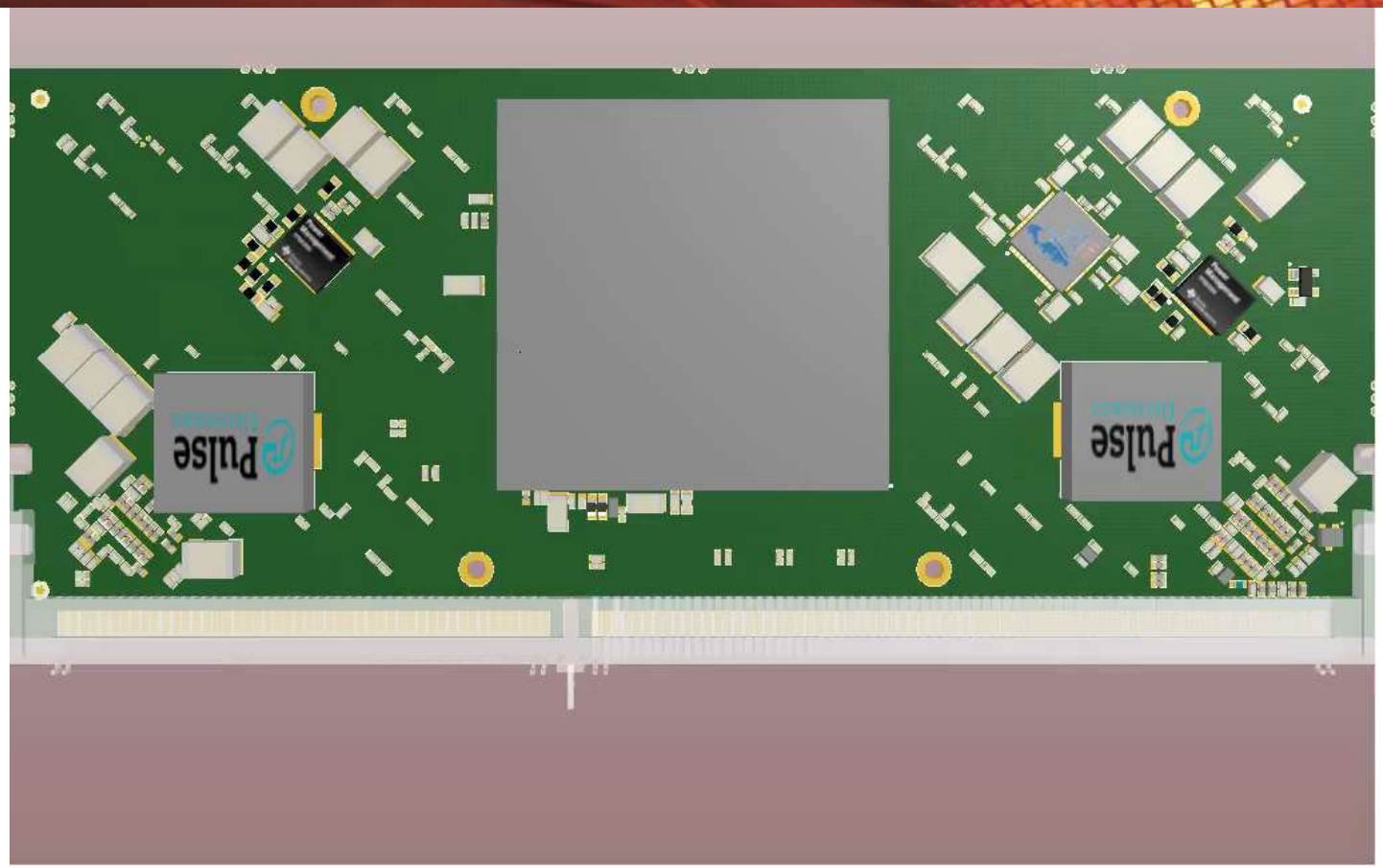
Dome Project

TRANSFER
DESIGN WORKS

ASTRON

IBM





Subjects

- Introduction
- DOME project
- Expectations before start of project
- Challenges
- The engineering part
- Results
- Lessons learned
- Currently running projects
- Benefits for Transfer
- Q & A

Introduction

- Henk de Jonge
- CTO at Transfer DSW (Formerly DsignWorx) since 2010
- Started on the Dome project in 2012
- Project Management for the various DOME projects:
  - Processor Module
  - Processor Baseboard Module
  - Switch Power Test Module
  - Switch Module Daughterboard
  - Switch Module Motherboard

Introduction Transfer

- **Design Automation Solutions**
  - PCB
  - ASIC/FPGA
  - System Design
- **Consulting Services**
  - EDA Integration
  - Library management
- **Educational Services**
  - Tool based
  - Methodology
- **Engineering services**

Design Automation Solutions

- Altium — Unified Electronic Devel. Solution
- JTAG Technologies — JTAG Design for test
- BoardPerfect — EDA Autorouter
- SpaceClaim — Smart 3D tool for engineers
- Simplified Solutions — 3D component models
- Desktop EDA — 3D (IDF) interface to AD

DOME Project

- SKA (Square Kilometer Array)
- Big Bang
- Big Data
- Bilateral
  - The Netherlands
  - Switzerland
  - South Africa
  - Australia
  - United Kingdom
  - Italy
  - …

DOME

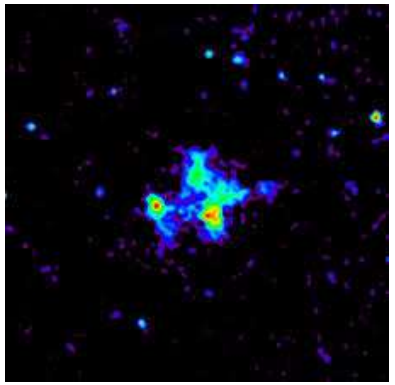
DOME User Platform

DOME Project - LOFAR

- LOFAR project (Low Frequency Array)
  - Low frequency -> High wavelength -> Large scaled antenna's
- Astron (Dwingeloo Dr.)

LOFAR

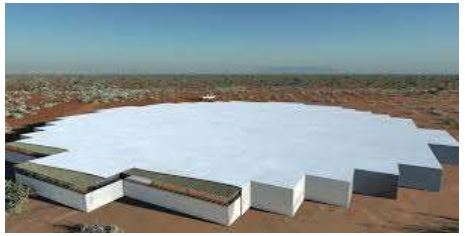
Antenna's



Imaging

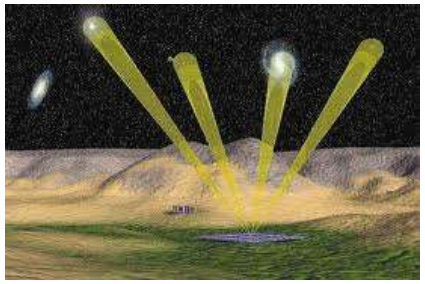
DOME Project -SKA

- SKA (Square Kilometer Array) Project



South Africa

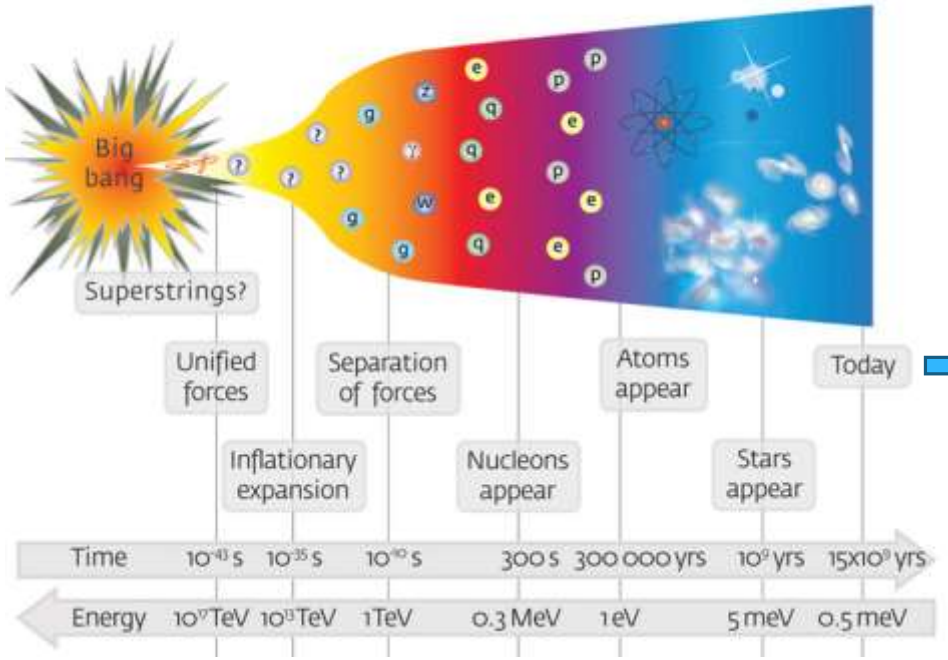
Australia



Beamforming

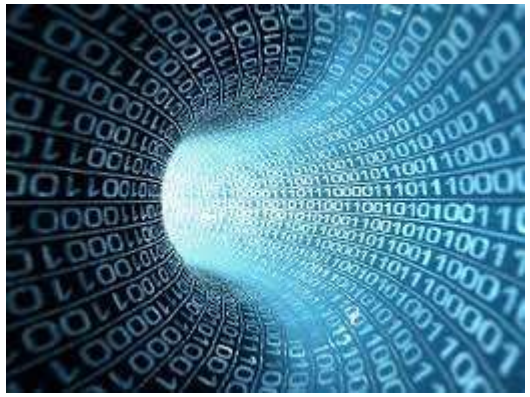
DOME Project – Big Bang

- Big Bang



DOME Project – Big Data

- Big Data - SKA project
  - Big Bang
- Exascale computing



- 2014 – 15 petaflops
- 2024 – 15 exaflops

Source: Wikipedia, the free encyclopedia

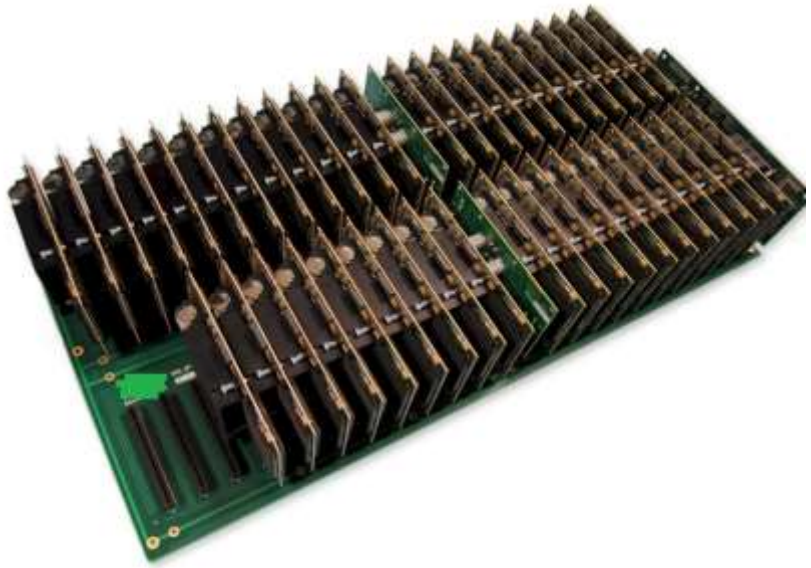
Exascale computing refers to computing systems capable of at least one exaFLOPS. Such capacity represents a thousandfold increase over the first petascale computer that came into operation in 2008. (One exaflops is a thousand petaflops or a quintillion, 10^{18}, floating point operations per second.)

DOME Project – Big Data

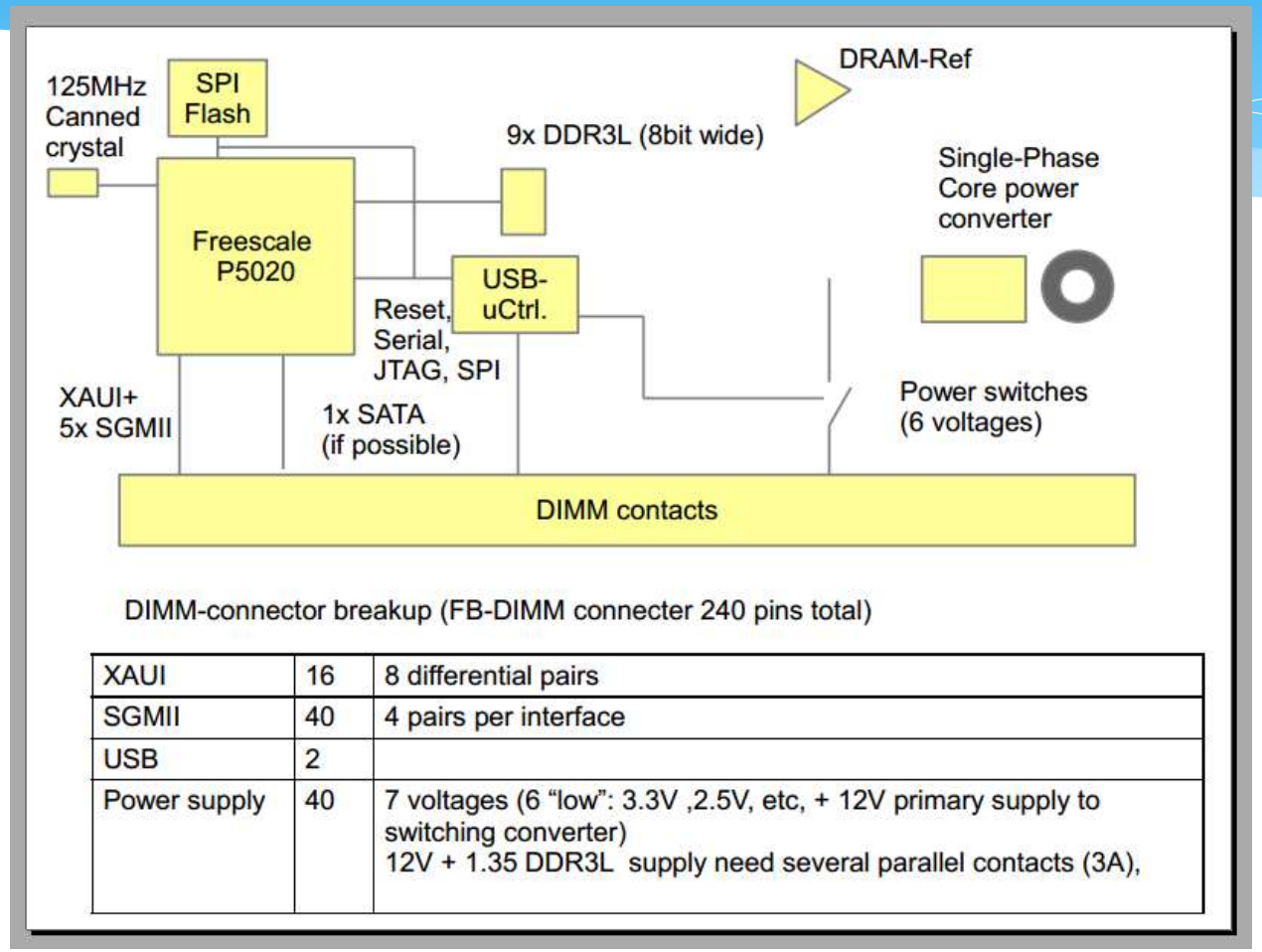
- Big Data - Ordinary world
  - Traffic
  - Bank transaction systems
    - 12 msec -> 4 msec ->
  - Shopping behaviour
    - Special discounts while shopping
  - Internet Search engines
  - …

DOME Project – Area

- 3 Main Areas:
  - Green Computing
  - Nano-photonics
  - **Data & Streaming**
- 7 Research Projects:
  - Algorithms & Machines
  - Access Patterns
  - Nano Photonics
  - Accelerators
  - Compressive Sampling
  - RT Communication
  - **Microservers**



Processor PCB – High level spec



DIMM-connector breakup (FB-DIMM connecter 240 pins total)

XAUI	16	8 differential pairs
SGMII	40	4 pairs per interface
USB	2	
Power supply	40	7 voltages (6 “low”: 3.3V ,2.5V, etc, + 12V primary supply to switching converter) 12V + 1.35 DDR3L supply need several parallel contacts (3A),

Processor PCB - Challenges

- Area PCB: 130 x 55 mm (~ DIMM size)
- 9 Twin-Die DDR3-IC's, total of 9 GB RAM
- Large BGA package
- 12 V -> 1V & 12 V -> 1.1 V power supply on-board, 20 Amps per supply
- Component height (board – to – board pitch as small as possible)

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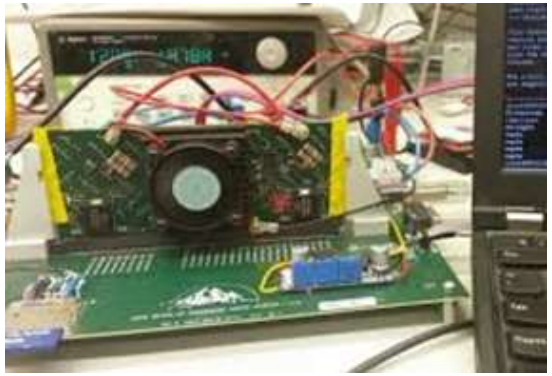
Processor Bring-up Baseboard - Challenges

- uServer mother board to test the on-board peripherals
- Area: 220mm x 160mm
- Mounted vertically (room for testing)
- Mechanically secured with screws that also provide the 12V supply
- The 12V power supply via the uServer module cooling mount
- All power supplies needed to run the P5020/P5040 compute module, can be supplied by the power connector (Lab power supply)

Processor Bring-up Baseboard - Challenges

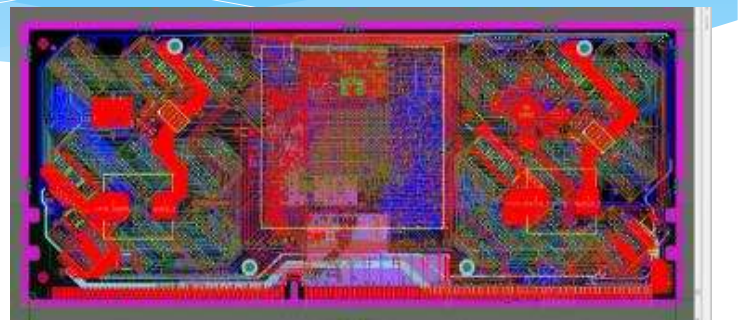
- The Bring-up baseboard needs the following high-speed interfaces:
  - USB-B (Slave)
  - Gigabit Ethernet
  - SD-Card
  - S-ATA (2x)
  - JTAG Debug header for PSOC3 Miniprog programmer
  - I/O connector for XAUI
  - Header for UART interface



Engineering the PCB's

Real R&D development Project:

- Change of specifications
  - Double DDR3 amount (18 instead of 9 IC's)
  - Double S-ATA ports
- DIMM pin out discussions (continuous change of pin outs)
- Preliminary datasheets (processor)
- 10-layer, 1.2 mm thick PCB, more than 60.000 (!) traces, arcs and vias
- No room for test pads



Engineering Tools

- Altium Designer
  - Schematic entry
  - PCB Layout
  - PCB 3D Design
  - Technical Product Documentation
- Saturn PCB
  - Controlled Impedance calculations
    - Single ended
    - Differential
- Signal Integrity simulation has been outsourced to Sintecs
- Cooling simulation and implementation will be done by IBM

SATURN PCB DESIGN, INC
Turnkey Electronic Engineering Solutions

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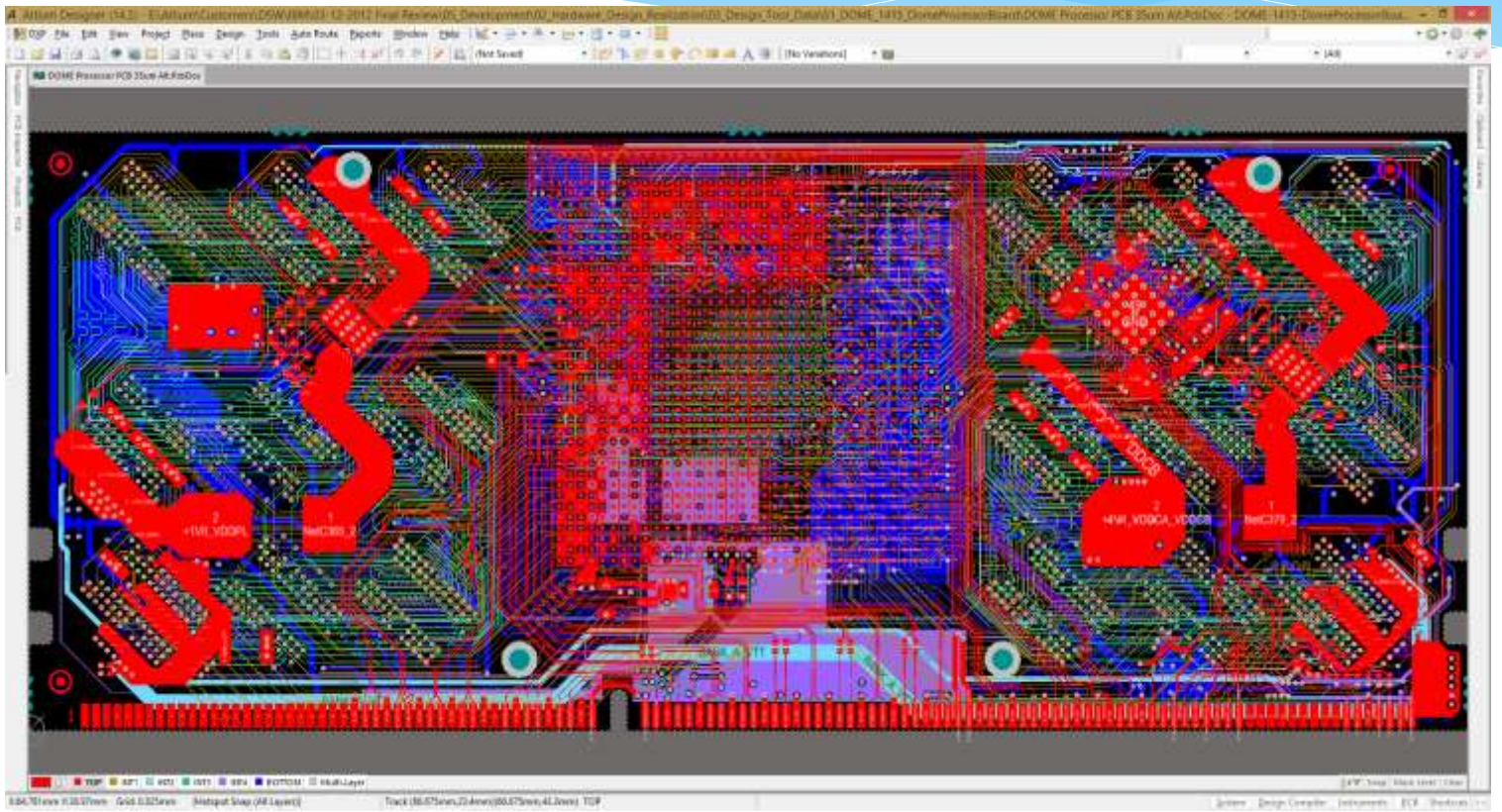
Engineering Tools

- Altium Designer



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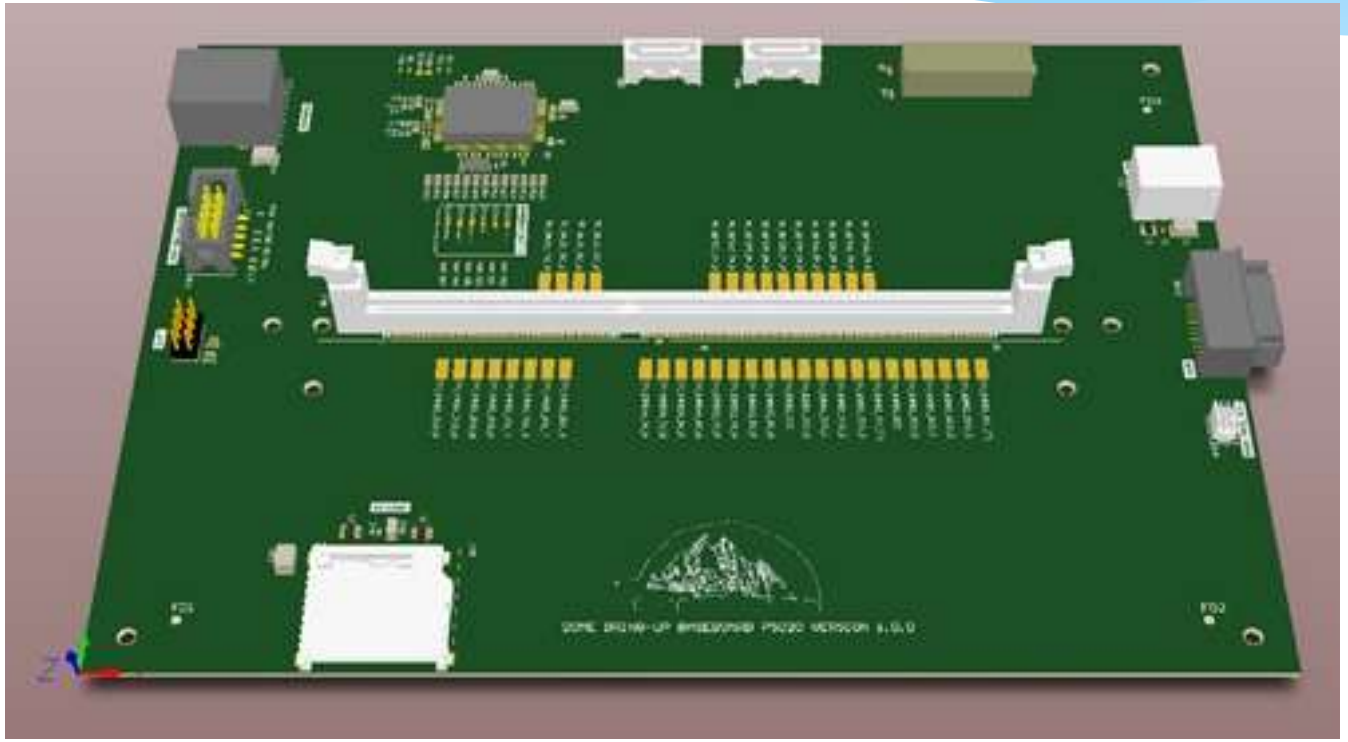
Processor Bring-up Baseboard



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Currently running projects

- Mini Base Board
- Network Switch Module
  - Daughterboard
  - Motherboard

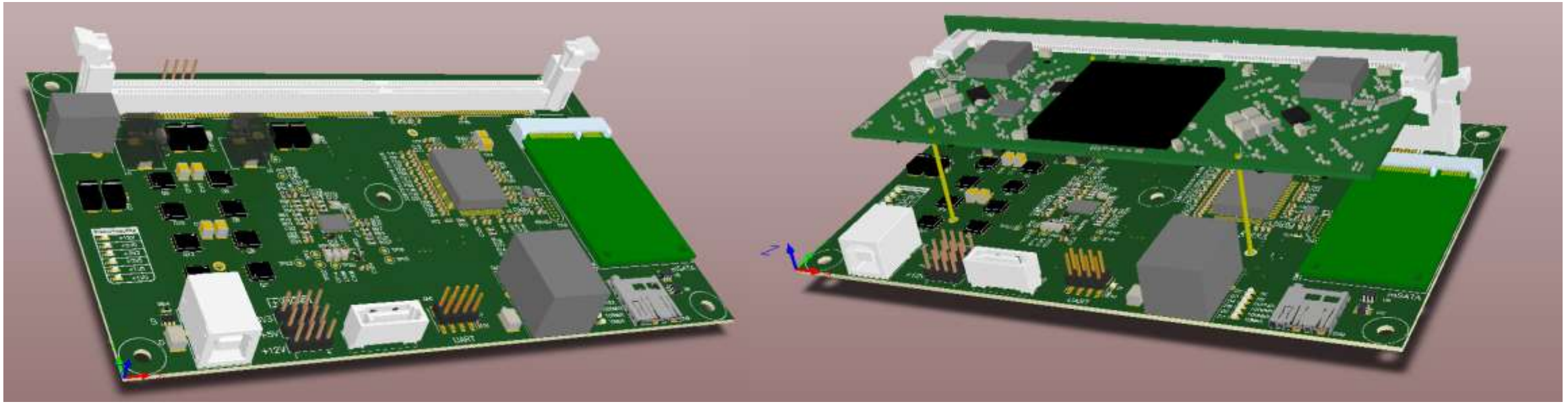
Mini Baseboard – Challenges

- Area PCB: 150 x 100 mm
- The processor module must be placed co-planary
- 90 degree DIMM connector
- Gigabit Ethernet
- USB
- SD card
- S-ATA connector
- PSOC programming header

Mini Base Board

- Software development board for processor module
- Single power supply
- External cooling possibilities
- Access to Ethernet & S-ATA interface
- USB access
- Storage possibility (SSD & SD-card)

Mini Base Board



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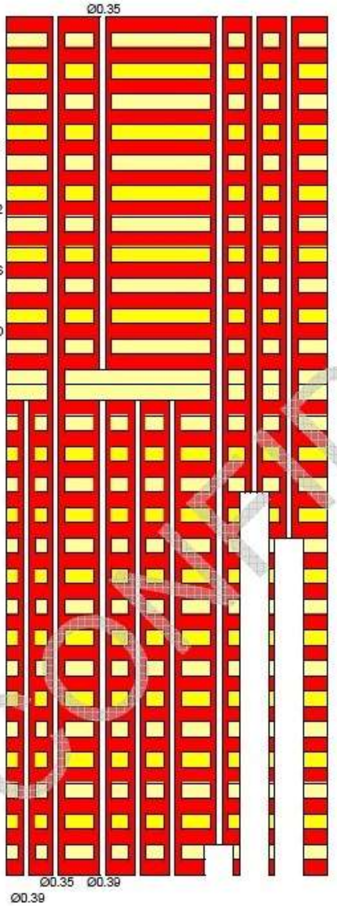
Network Switch Module

- Used for interfacing the processor modules
- 24 channel 10 Gbit Ethernet
- 2x 60 Amp @ 1V power supply
- 1x 15 Amp @ 1.1V power supply
- Microcontroller used for configuration, power up sequence & diagnosis

Network Switch Module Motherboard

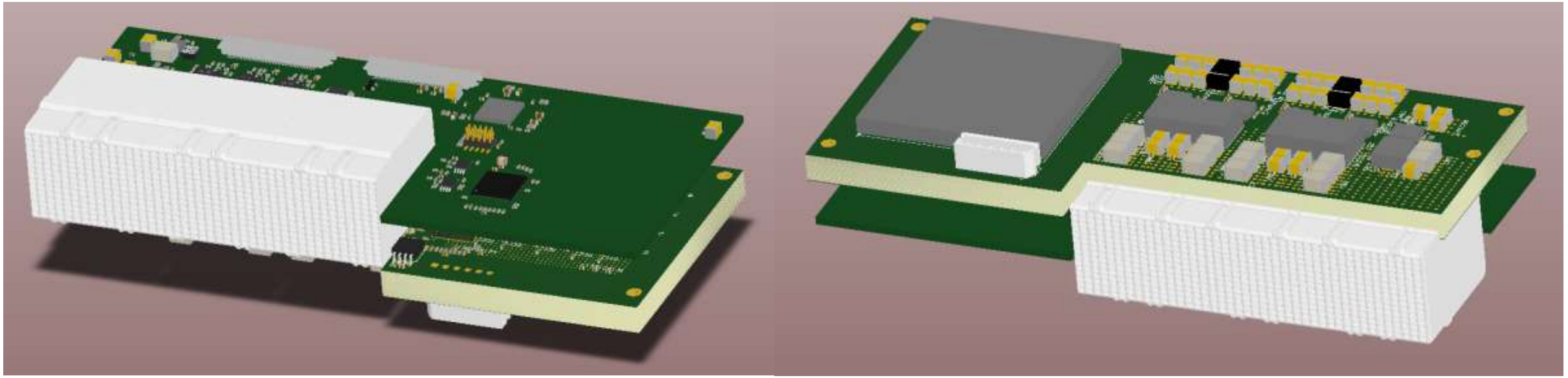
Altium names	LG	Function
Bottom Layer	01	Comp
GND 7	02	Ground
Signal 2	03	Sig 1
GND 6	04	Ground
VDD	05	PowerVDD
GND 5	06	Ground
VDDS	07	PowerVDD2
GND 4	08	Ground
AVDD	09	PowerVDDS
GND 3	10	Ground
+12V	11	PowerAVDD
GND 2	12	Ground
Shield 7	13	Ground
Diff 6	14	Diff 1
Shield 6	15	Ground
Diff 5	16	Diff 2
Shield 5	17	Ground
Diff 4	18	Diff 3
Shield 4	19	Ground
Diff 3	20	Diff 4
Shield 3	21	Ground
Diff 2	22	Diff 5
Shield 2	23	Ground
Diff 1	24	Diff 6
Shield 1	25	Ground
Signal 1	26	Sig 2
GND1	27	Ground
Top Layer	28	Comp

Aufbauplan



Abacus	Material	Pressungen 1	2	3	4	Enddicke nach dem Pressen
	Cu 5+25->15+25dp	0.040				
xx2	FR408HRIS PP 2013 59%	0.100				
	Cu 35	0.035				
xx1	FR4408HRIS	0.100				
	Cu 35	0.035				
xx2	FR408HRIS PP 2013 59%	0.100				
	Cu 35	0.035				
xx1	FR4408HRIS	0.100				
	Cu 35	0.035				
xx2	FR408HRIS PP 2013 59%	0.100				
	Cu 35	0.035				
xx1	FR4408HRIS	0.100				
	Cu 35	0.035				
xx2	FR408HRIS PP 2013 59%	0.100				
	Cu 35	0.035				
xx1	FR4408HRIS	0.100				
	Cu 35	0.035				
xx2	FR408HRIS PP 2013 59%	0.100				
	Cu 35	0.035				
xx1	FR4408HRIS	0.100				
	Cu 35	0.035				
xx2	FR408HRIS PP 2013 59%	0.100				
	Cu 5+25	0.030				
800785	PREPREG49N			0.086		
800785	PREPREG49N			0.086		
	Cu 5+25		0.030			
xx2	FR408HRIS PP 2013 59%		0.100			
	Cu 18		0.018			
xx1	FR4408HRIS		0.100			
	Cu 18		0.018			
xx2	FR408HRIS PP 2013 59%		0.100			
	Cu 18		0.018			
xx1	FR4408HRIS		0.100			
	Cu 18		0.018			
xx2	FR408HRIS PP 2013 59%		0.100			
	Cu 18		0.018			
xx1	FR4408HRIS		0.100			
	Cu 18		0.018			
xx2	FR408HRIS PP 2013 59%		0.100			
	Cu 18		0.018			
xx1	FR4408HRIS		0.100			
	Cu 18		0.018			
xx2	FR408HRIS PP 2013 59%		0.100			
	Cu 18		0.018			
xx1	FR4408HRIS		0.100			
	Cu 18		0.018			
xx2	FR408HRIS PP 2013 59%		0.100			
	Cu 18		0.018			
xx1	FR4408HRIS		0.100			
	Cu 18		0.018			
xx2	FR408HRIS PP 2013 59%		0.100			
	Cu 18		0.018			
xx1	FR4408HRIS		0.100			
	Cu 18		0.018			
xx2	FR408HRIS PP 2013 59%		0.100			
	Cu 5+25->15+25dp		0.040			
	Dicken	1.520	1.822	0.172	0.000	3.514

Network Switch Module



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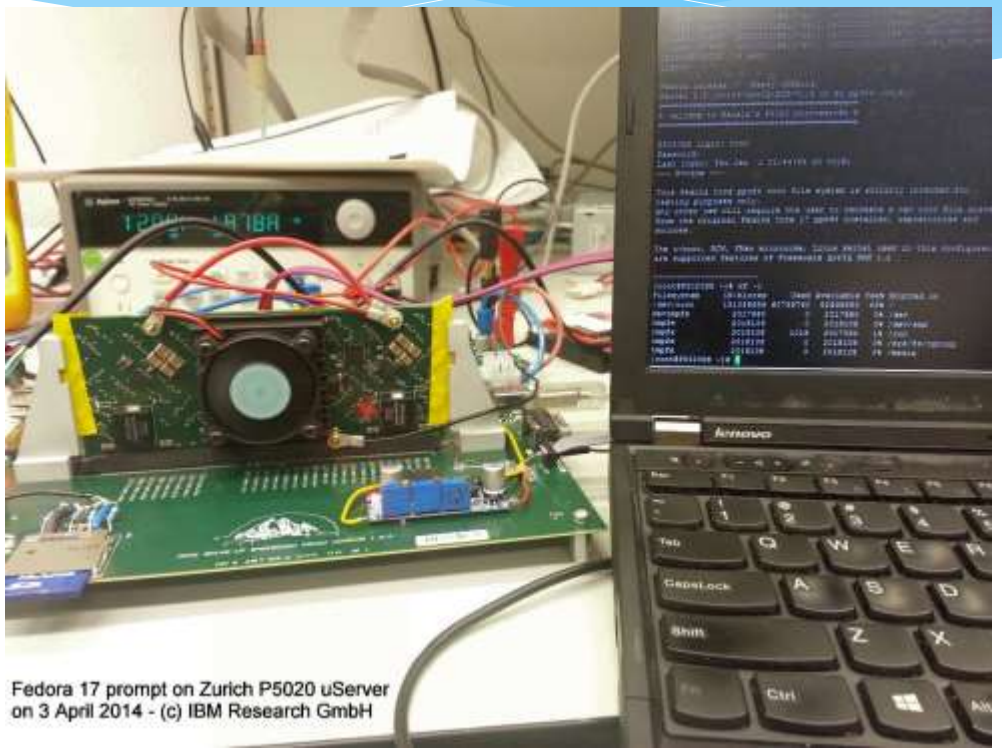
Lessons learned

- Out of the box thinking
  - Power through cooling body
- Extended on-board diagnosis
  - JTAG Boundary Scan
    - Simulation/testing & functional diagnosis at the same time
- Signal Integrity
  - High-Speed design course

Benefits from the project

- Major growth in experience
- Growth in manpower
  - Increased from 3 to 6 employees
- Easier to get projects from customers
  - Workmanship/Experience
- Helped to improve products of our software suppliers

Results



What's in for YOU!

- Challenge the DOME participants for JOINT microserver business development
- Together, let's define power-efficient processing concepts for your future business!

- Contact us: info@transferdsw.nl

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Q & A

Any questions?

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