

DESIGN AUTOMATION EMBEDDED SYSTEMS

FPGA - EMBEDDED - INTERNET OF THINGS - PCB TECHNOLOGIEËN

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System on Module FPGA based with integrated processor



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Agenda

- **Introduction**
 - Adelco Electronics
 - iWave Systems
- **Advantages using FPGA on standard Qseven SOM**
- **Design Challenges**
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- **Design Examples**
- **Summary**
- **Questions**

Adelco Electronics

- **Founded in April 2003**
- **Solution provider for Displays, Embedded Computing and Wireless Products**
- **Experienced and technically skilled sales team providing application support**
- **Headquarter in Capelle aan den IJssel/NL**
- **Sales office in Belgium**



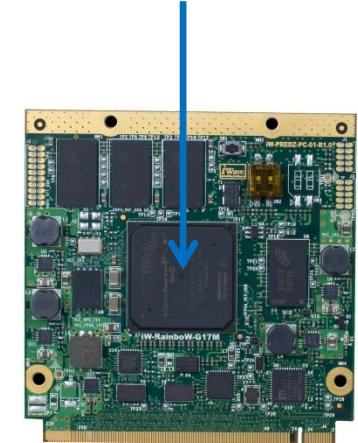
iWave Systems

- **15+ Years of Experience in Embedded Product Design Services**
- **Based in Bangalore/India**
- **180+ Team Size, 140+ Engineers**
- **Expertise in Design & Development of System On Modules (SoM)**
- **Quick Customization to “Time to Market”**
- **Onsite and Offshore Design Support**
- **Through Partners in Europe, USA & Singapore**



Advantages using FPGA on standard Qseven SoM

- **Implementing custom proprietary hardware IP with the use of an external FPGA, where standard ARM CPUs cannot be used.**
- **Providing simple single-chip solution for complex requirements:
ARM + FPGA = SoC**
- **Standard Qseven form-factor architecture used in design**
- **Custom Secure IP solution**
- **Cost-effective and Time-to-market benefits**
- **The only Qseven ARM solution offered in the market with PCIe x4 lane support available through SoC.**



Design Challenges

- **Meeting the SoC power requirements within the small form-factor**
- **Implementing the high speed and differential signal requirements of SoC design**
- **Meeting the high density PCB layout requirements within a small form-factor**
- **Mapping the SOC's flexible IO's to meet the Qseven standard interface requirements**



Product Details

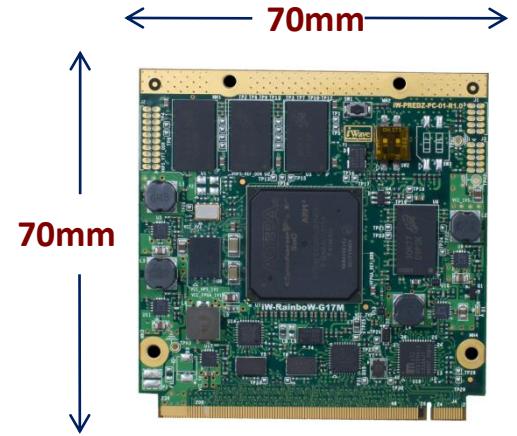
Cyclone V SoC Qseven SOM

iW-RainboW-G17M-Q7



Highlights

- ARM Cortex A9 Dual core with FPGA with up to 110KLEs
- Integrated transceivers and hard memory controller
- Easy available FPGA IP cores for integration
- R2.0 Qseven compatible module
- First ARM based SOM module with PCIe x 4 lane support



Top view



Bottom view

Benefits:

- Technical support
- Customization
- Longevity 5+ years
- Quick time to market
- Board Support Packages Available

Features and Specification

CPU:

- Altera's Cyclone V SX SoC FPGA
 - Integrated Dual core ARM Cortex-A9 Hard Processor System(HPS)
 - FPGA with upto 110K LEs

Memory:

- 512MB DDR3 with ECC for HPS
- 16MB QSPI Flash
- 256MB DDR3 for FPGA
- EPCQ flash*/QSPI Flash for FPGA
- EEPROM*

On Board Peripherals Support:

- JTAG Header for FPGA*
- JTAG Header for HPS*
- DIP Switch for boot settings
- RTC controller

80 Pin Expansion Connector:

- FPGA IOs (Up to 45 Single Ended IOs - SE IOs)
- 9 TX LVDS Pairs / 18 SE IOs
- 11 RX LVDS Pairs / 22 SE IOs

Power Input: 5V DC

Operating Temp: -40°C to +85°C Industrial

Qseven PCB Edge Connector Interfaces:

- From HPS:
 - Gigabit Ethernet - 1 No (On-SOM PHY)
 - USB 2.0 Host - 4 Ports (On-SOM HUB)
 - CAN x 1 Port
 - SD/MMC (8 bit)
 - I2C x 2 Ports
 - SPI x 1 Port
 - Debug UART x 1 Port
 - 2nd UART x 1 Port
 - Other Control IOs - Through HPS
- From FPGA:
 - LVDS LCD - 2 Ports (FPGA Soft IP)/ 23 SE IOs
 - AC97/I2S Audio (FPGA Soft IP)/ 5 SE IOs
 - PWM
 - FPGA IOs- 8 CMOS
- From FPGA High Speed Transceivers:
 - SATA (FPGA Soft IP)
 - PCIe Gen2 x 4 Lane

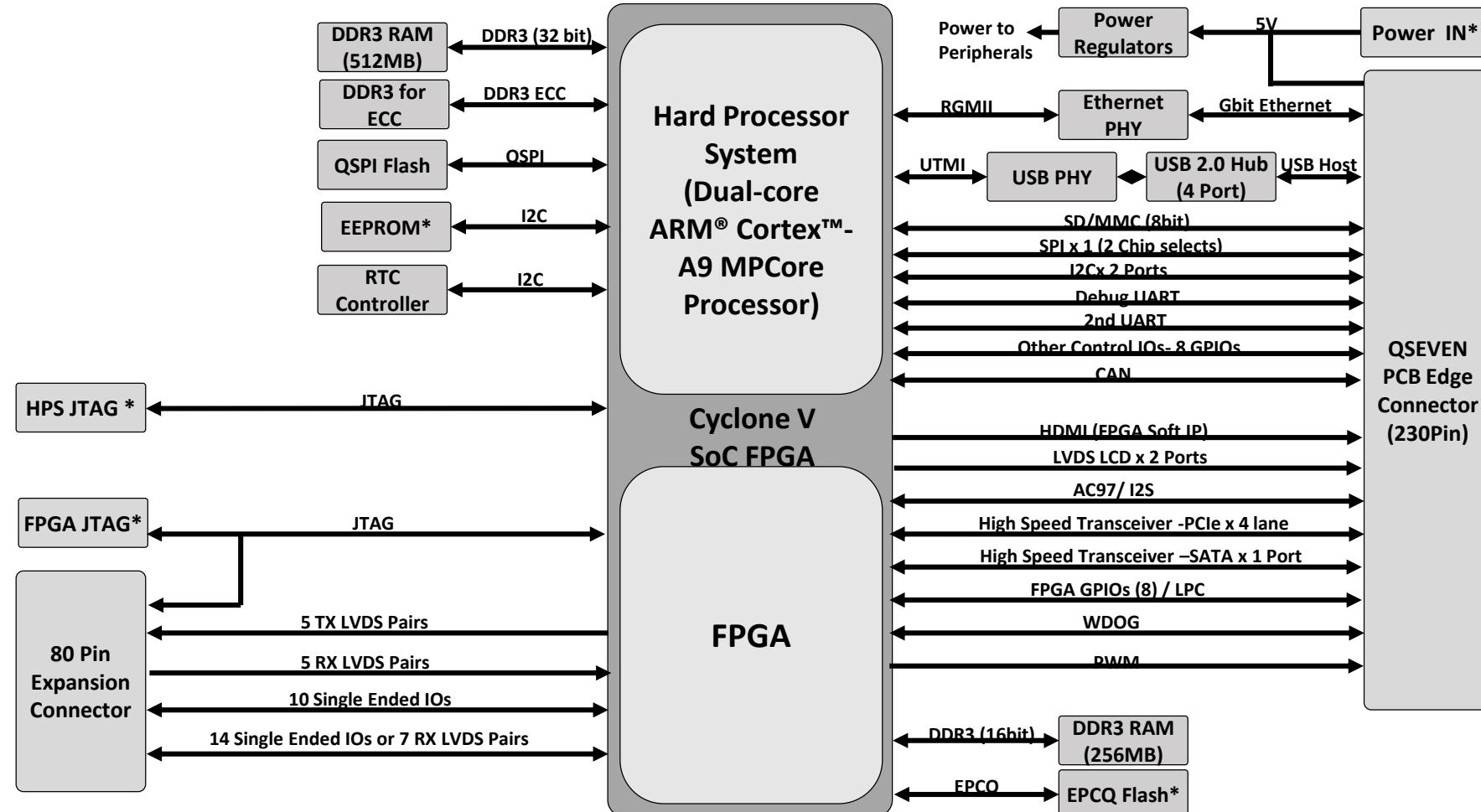
Form Factor: 70 x 70 mm Qseven Spec 2.0

OS Support: WEC7 & Linux

*Optional



Block Diagram



*Optional

Development Kit

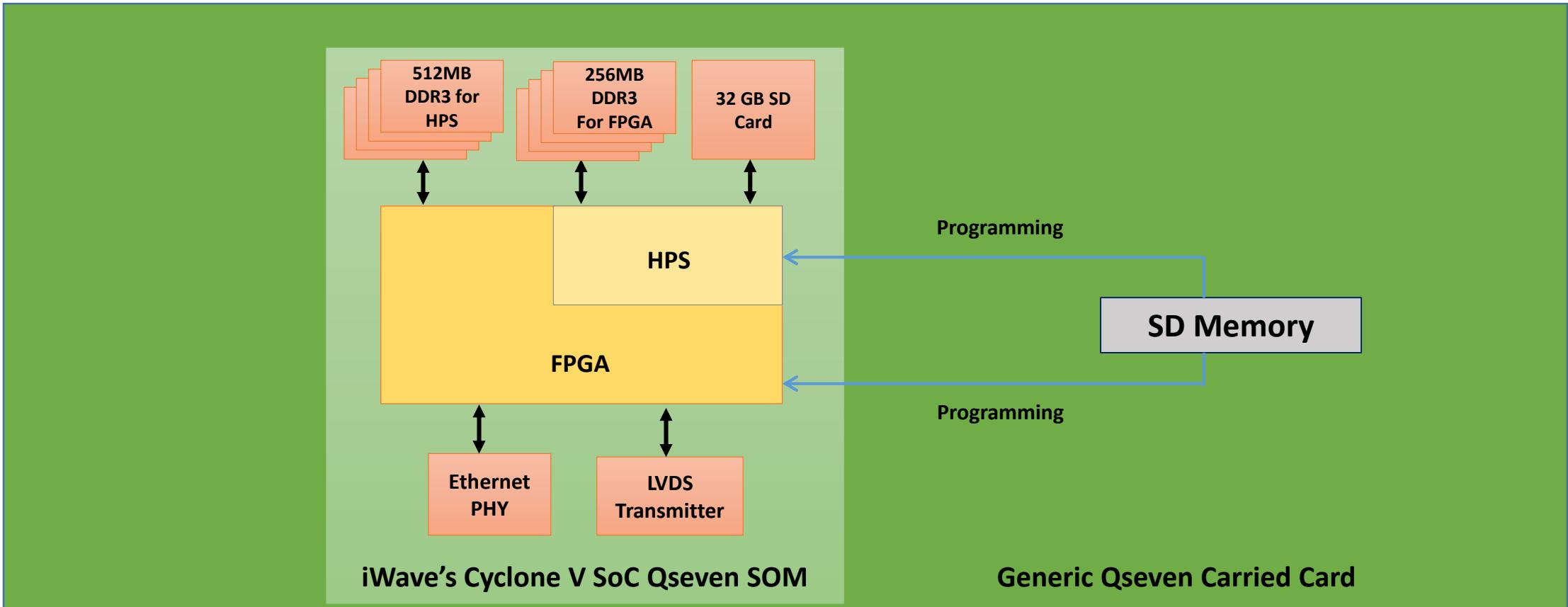
- **CPU: Altera's Cyclone V 5CSXFC6 SoC FPGA**
- **RAM: 512MB HPS / 256MB FPGA**
- **Gigabit Ethernet**
- **Standard SD - 1 Port (Boot & OS Storage)**
- **SATA 3.0 - 1 Port**
- **Data UART- 1 Port**
- **CAN – 1 Port**
- **Debug Console through Micro USB**
- **USB 2.0 Host - 3 ports**
- **PCIe x 1 slot**
- **LVDS - 2 Port**
- **7" TFT Display with Capacitive touch**
- **Sensors, GPIO's, RTC, JTAG Header (optional)**
- **AC'97 codec - Audio IN/OUT Jacks**



Programming

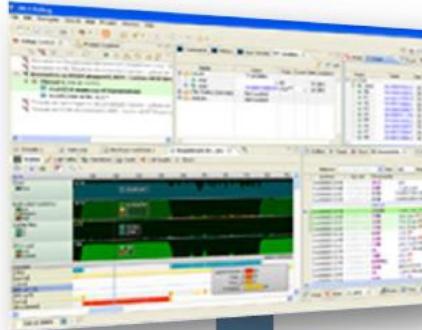
- The FPGA can be configured/programmed in either of below ways:**
 - **With the Quartus Programmer Tool (FPGA fabric)**
 - **From Hard Processing System (HPS)**
- The different FPGA configuration options from HPS software using U-boot and Eboot**
- For iWave's Cyclone V SoC, the selected method of programming the FPGA is from U-boot/Eboot. FPGA configuration file(.rbf) is stored in the standard SD memory.**
- The U-boot/Eboot will read .rbf file from the SD memory and then programs the .rbf files to the FPGA fabric.**

Programming



Debugging: One device, Two Tools?

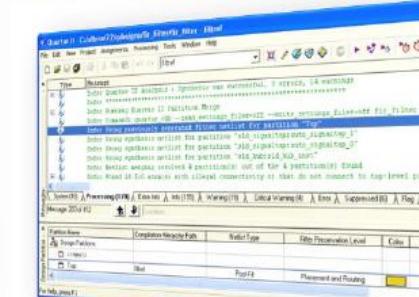
ARM DS-5 Toolkit



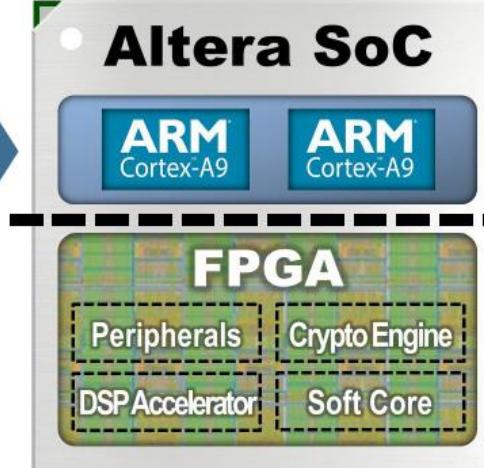
- Dedicated JTAG connection
- Visualize & control CPU subsystem



Altera Quartus® II Software



JTAG



- Dedicated JTAG connection
- Visualize & control FPGA

Debugging: One device, Two Tools?

ARM® DS-5™ Toolkit



- Dedicated JTAG connection
- Visualize & control CPU subsystem

Altera Quartus™ II Software

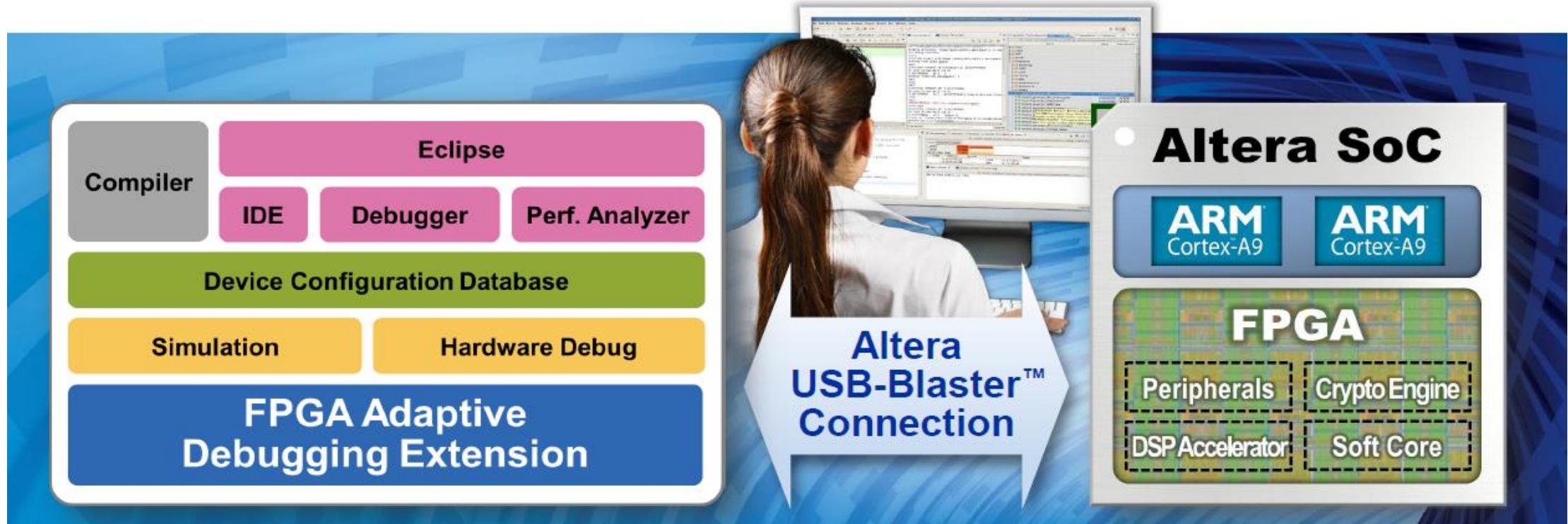


- Dedicated JTAG connection
- Visualize & control FPGA

Debugging Barrier

- No single tool/cable to visualize and control both CPU and FPGA domains
- No way for CPU and FPGA to cross trigger and correlate hardware and software events
- No “fixed” debugger can address the needs of “changing” FPGA hardware

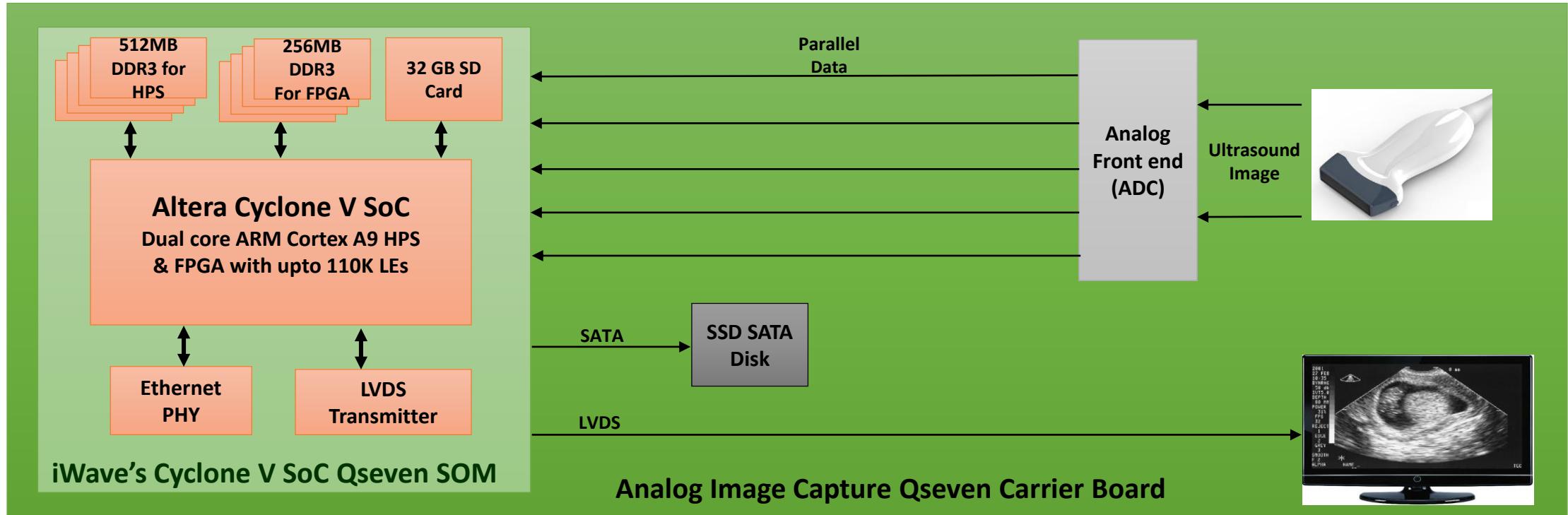
FPGA: Adaptive Debugging



ARM Development Studio 5 (DS-5™) Altera Edition Toolkit

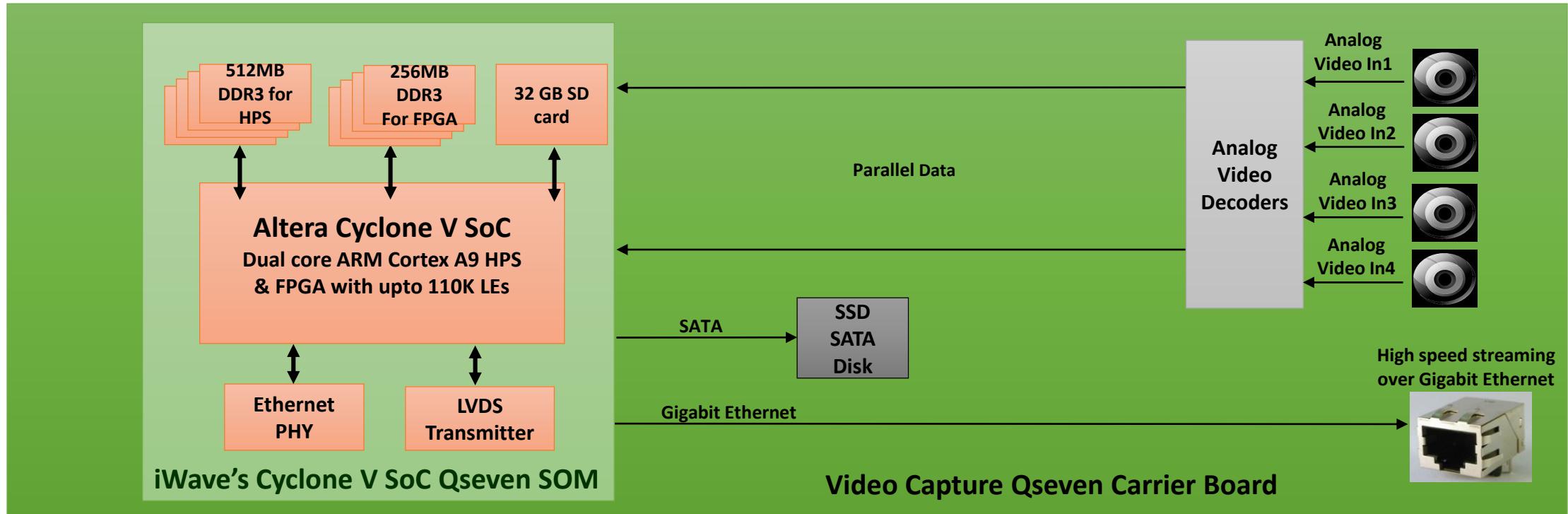
- Removes debugging barrier between CPUs and FPGA
- Exclusive OEM agreement between Altera and ARM
- Result of innovation in silicon, software, and business model

Examples



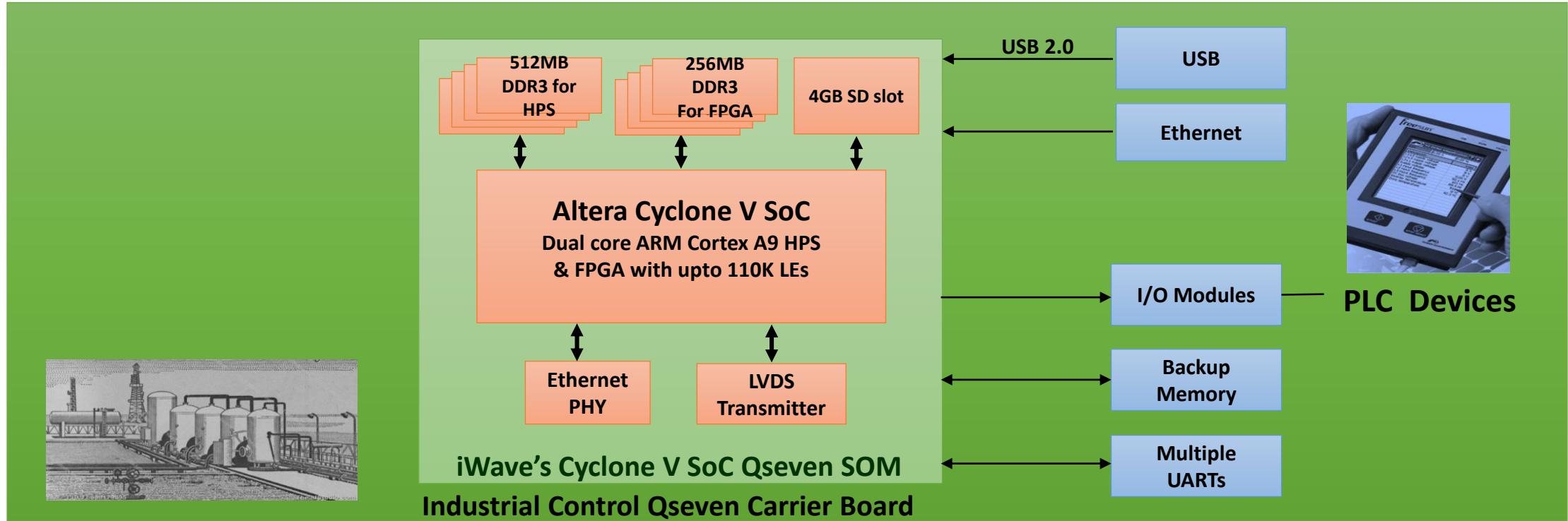
- **High speed image capture using SOC's FPGA IF**
- **Image processing through the Dual core CPU**
- **High speed mass storage on SATA SSD disk**
- **LVDS Display Interface Support**

Examples



- **High speed video capture using SOC's FPGA IF**
- **Video & Graphic processing through Dual core CPU**
- **High speed mass storage on SATA SSD disk**
- **High speed video streaming over Gigabit Ethernet**

Examples



- **SD, USB, I2C, SPI, Ethernet, GPIO interfaces will be used from the ARM CPU.**
- **By using the FPGA's PCIe interface, PCIe to multiple UARTs, PCIe to memory interface and other PLC specific IO interfaces will be developed.**

Summary

System on Module FPGA based with integrated processor

- **Implementing custom proprietary hardware IP**
- **Standard Qseven form-factor**
- **Cost-effective and Time-to-market benefits**
- **PCIe x4 lane support**

Questions?



You are welcome to visit our boot!

- To discuss your design opportunities
- To see more demo's!



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