

Quadra **Solutions** Limited

People. **Knowledge.** Innovation.

**Save Time & Money with
an Integrated Design
Flow**



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Save Time & Money with an Integrated Design Flow

For many years it has been acceptable to use individual point tools to analyse and verify your high speed layouts and critical nets, but today's high performance FPGAs, DSPs and Micro-Processors require a more sophisticated approach

The **CADSTAR High Speed Design Suite** lets you adopt an integrated design flow to create, implement, analyse, verify and document all of your constraints in one seamless environment

Who cares about Integration?

- > You and your colleagues
 - > Design, Layout, Production, Test
 - > Fast, Accurate, Secure, Repeatable
- > Your Partners
 - > Consultants, Fabrication, Assembly, Test
 - > Accurate, Timely, Complete
- > Management
 - > Internal, External (customers)
 - > On schedule, to Budget



Why is Integration important?

> Integration:

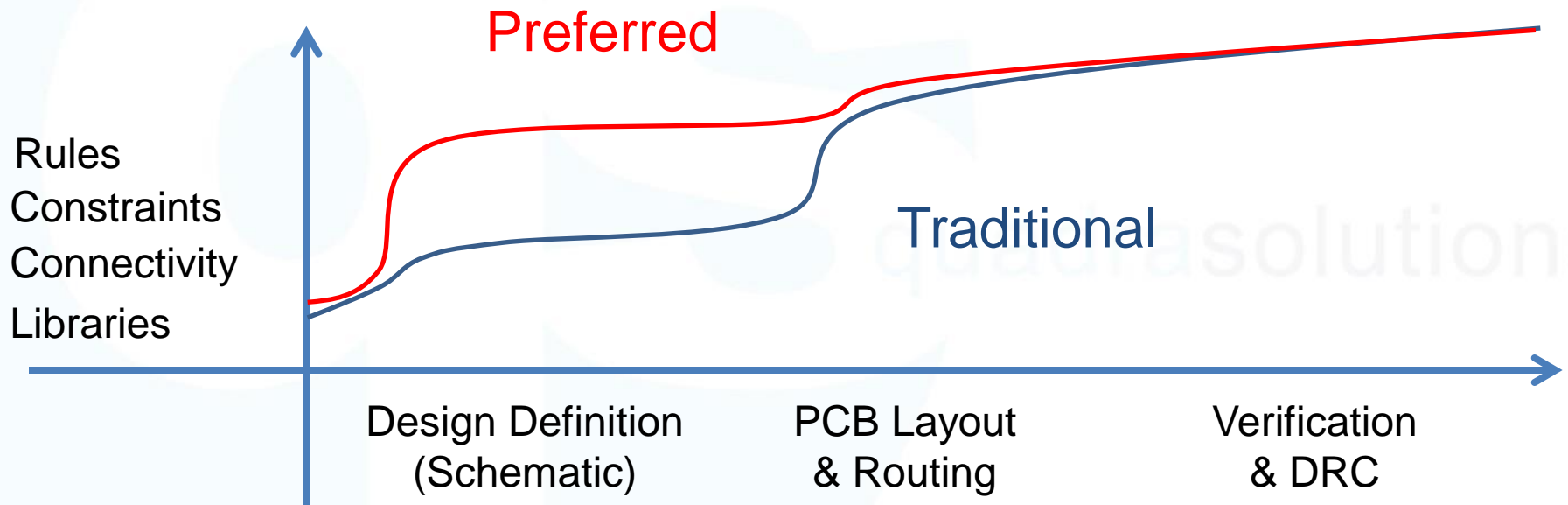
- > Enables a single repository for all critical data in the design flow
- > Eliminates the need for data translation between tools
- > Reduces risk and potential for error
- > Saves time!

What data can you share?

- > Libraries
 - > Electrical (Symbol, Component, Part)
 - > Mechanical (3D)
 - > Simulation & Modelling (Spice, IBIS, etc.)
- > Electronic Design Data
 - > Schematic, PCB Layout, ReUse blocks, etc.
- > Rules & Constraints
 - > Manufacturing, Electrical

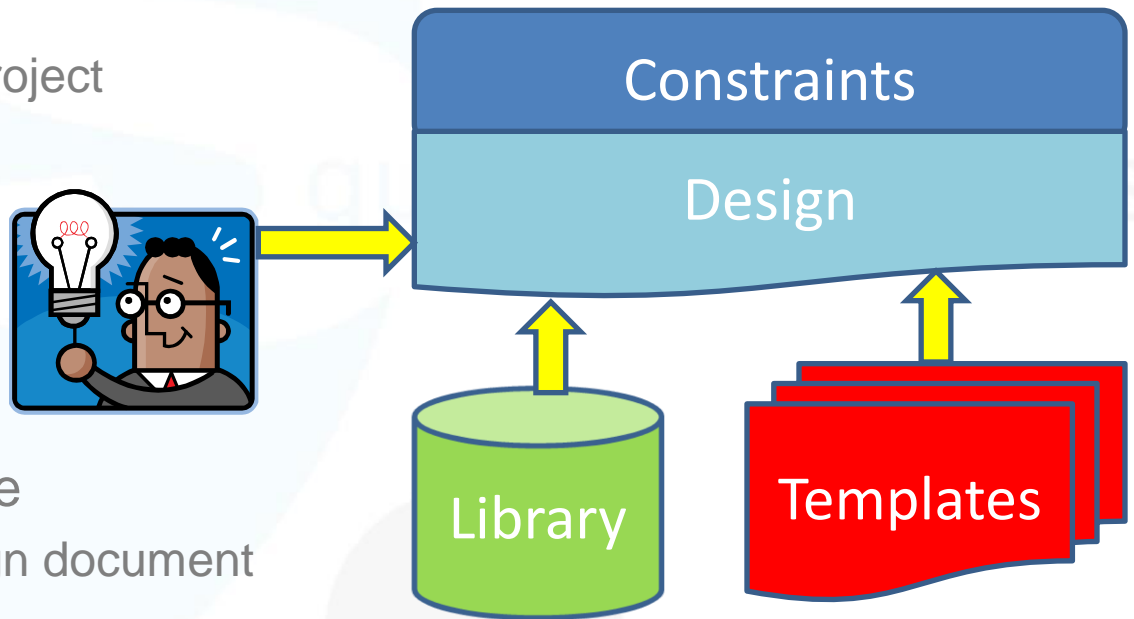
When is Data Required?

> Builds up during the design process

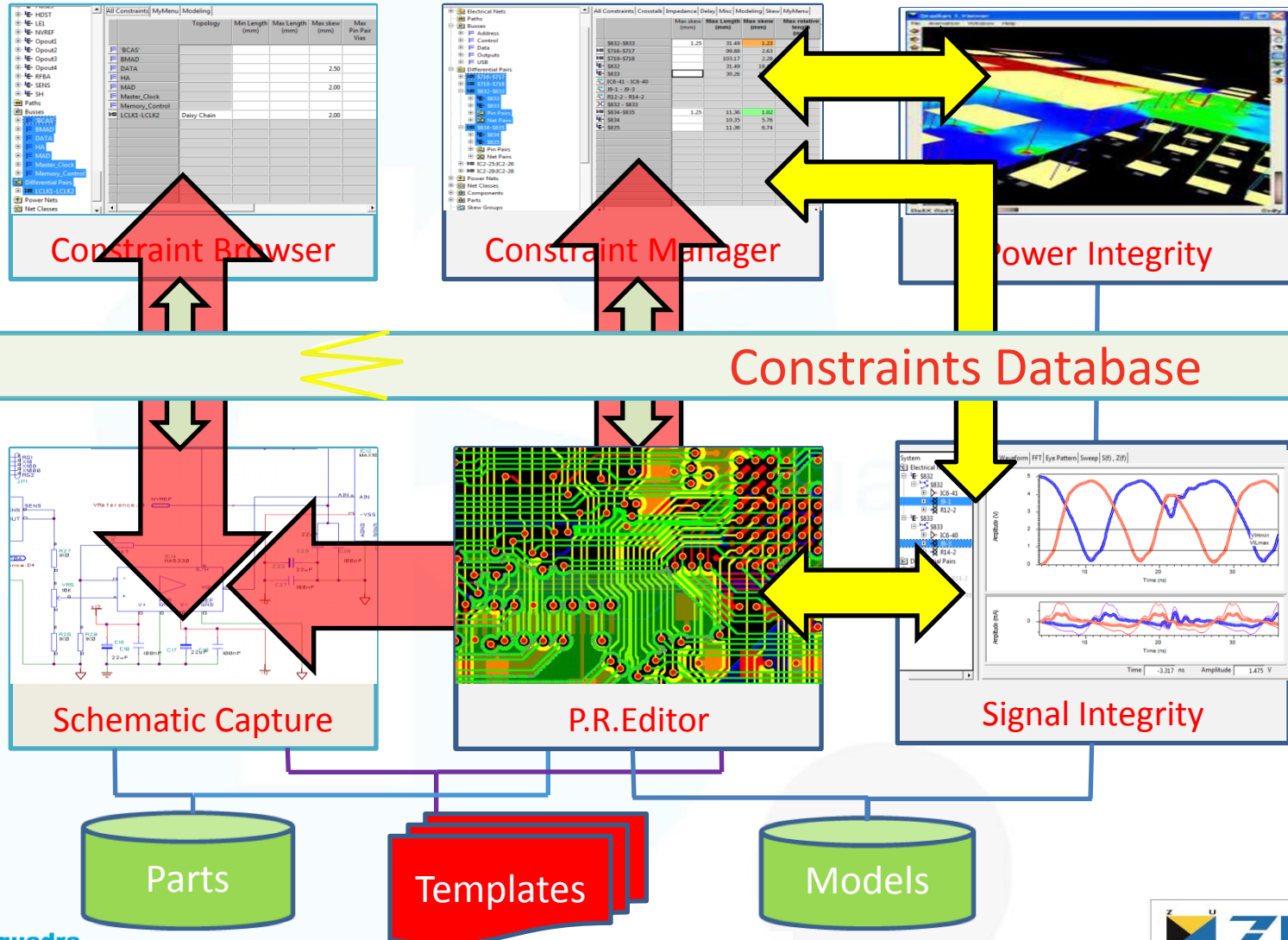


Where does the data reside?

- > Libraries
 - > CAD Library or Database
 - > Company, User, Project
- > Rules
 - > Templates
 - > Company, User, Project
- > Design Data
 - > Project folder
 - > Variants
- > Constraints
 - > Constraints database
 - > Linked to the design document



How integration works in the CADSTAR design flow



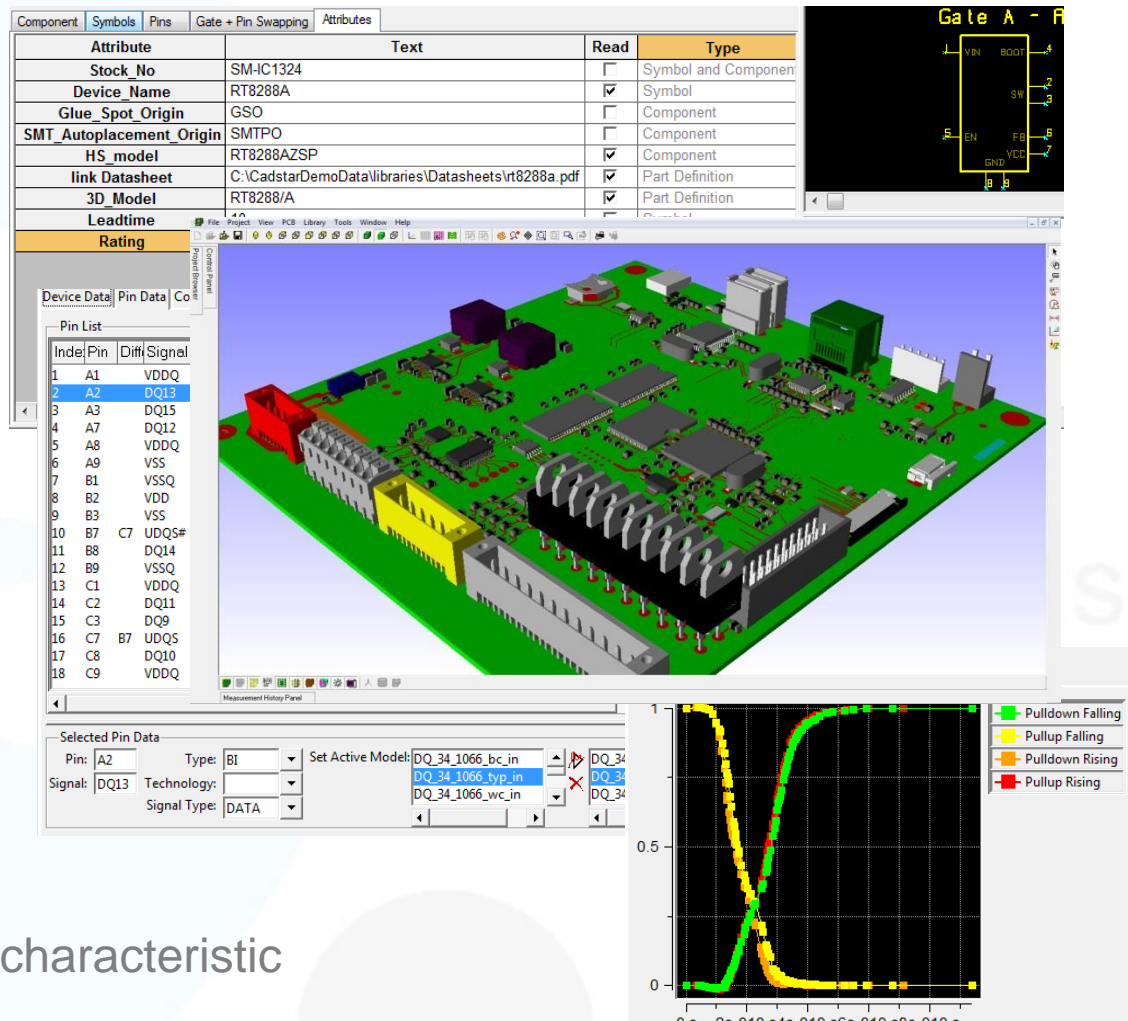
Libraries

> CAD

- > Electrical
 - > Design
 - > Selection
- > Data-centric
 - > Information
- > Lifecycle
 - > History
 - > Versioning

> Models

- > Simulation
 - > Packaging
 - > Pin types and characteristic
- > 3D



Templates

> Library creation

> Symbols, Footprints, Documentation

> Standards (Corporate, National, External)

> Attributes

> Schematic

> Structure

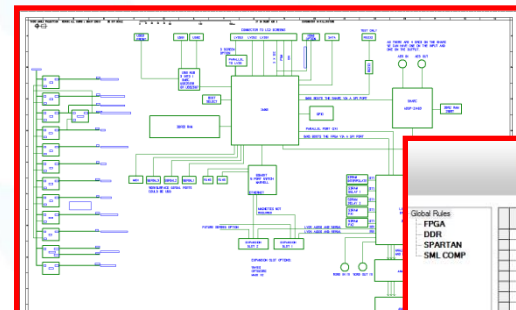
> Conventions

> PCB

> Layer Stack

> Rules set

> Manufacturing



Route to SMD Pad

Design Rule	Layer	Defined	Value (Thou)	Type
Comp Placement to Comp Placement	Default	<input checked="" type="checkbox"/>	5.00	Spacing
Copper to Board	Default	<input checked="" type="checkbox"/>	40.00	Spacing
Copper to Copper	Default	<input checked="" type="checkbox"/>	10.00	Spacing
Hole to Hole	Default	<input checked="" type="checkbox"/>	8.00	Manufacture
Maximum Micro	Default	<input checked="" type="checkbox"/>	0.00	Manufacture
Minimum Micro	Default	<input checked="" type="checkbox"/>	0.00	Manufacture
Minimum Thicker Track Length	Default	<input checked="" type="checkbox"/>	0.00	Manufacture
Minimum Thinner Track Length	Default	<input checked="" type="checkbox"/>	0.00	Manufacture
...

Layers

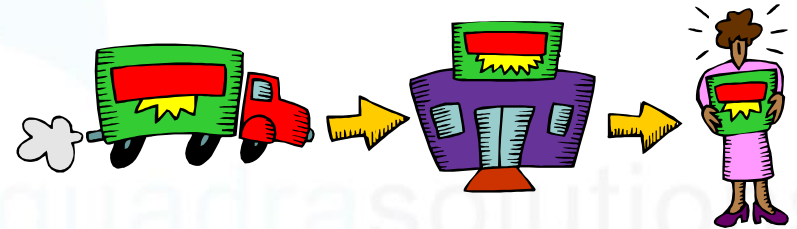
Name	Type	Thickness (Thou)	Embedding	Material	Reference Plane
Top Resist Core	Construction	0.01	None	Resist	
Top Die	Electrical	1.40	Above	Copper Fill	
Prepreg1	Construction	4.00	None	Prepreg	
Layer 2	Powerplane	1.40	Above	Copper Fill	
Core1	Construction	4.00	None	Fiberglass	
Layer 3	Electrical	1.40	Below	Copper Fill	
Prepreg2	Construction	7.10	None	Prepreg	
Layer 4	Electrical	1.40	Above	Copper Fill	
Core2	Construction	4.00	None	Fiberglass	
Layer 5	Powerplane	1.40	Below	Copper Fill	
Prepreg3	Construction	7.10	None	Prepreg	
Layer 6	Powerplane	1.40	Above	Copper Fill	
Core3	Construction	4.00	None	Fiberglass	
Layer 7	Electrical	1.40	Below	Copper Fill	
Prepreg4	Construction	7.10	None	Prepreg	
Layer 8	Electrical	1.40	Above	Copper Fill	
Core4	Construction	4.00	None	Fiberglass	
Layer 9	Powerplane	1.40	Below	Copper Fill	
Prepreg5	Construction	4.00	None	Prepreg	
Bottom Die	Electrical	1.40	Below	Copper Fill	
Bottom Resist C	Construction	0.01	None	Resist	

Physical Board Thickness = 59.32in

Material Details: Material: Prepreg, Use for Layer Type: Construction, Permittivity: 4.3, Loss Tangent: 0.05, Resistivity: 1.750000e-8 Ohm/m

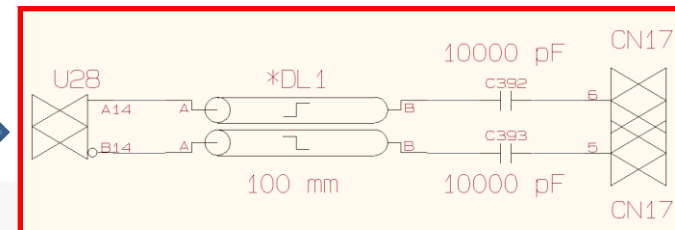
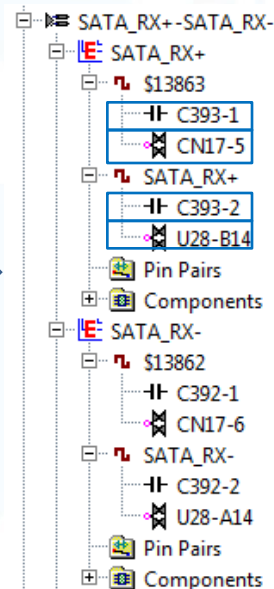
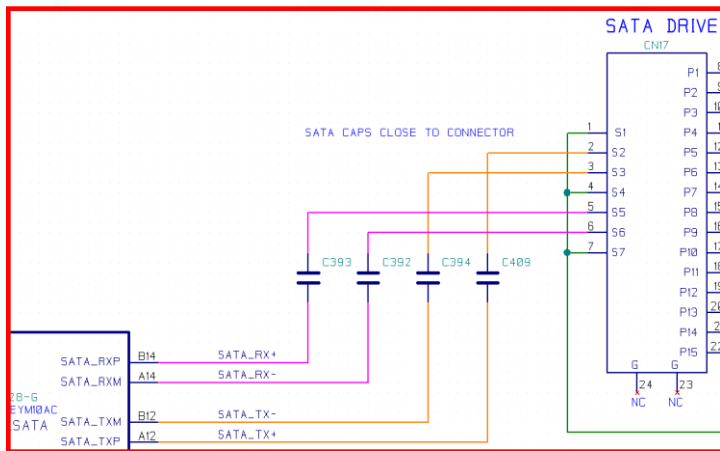
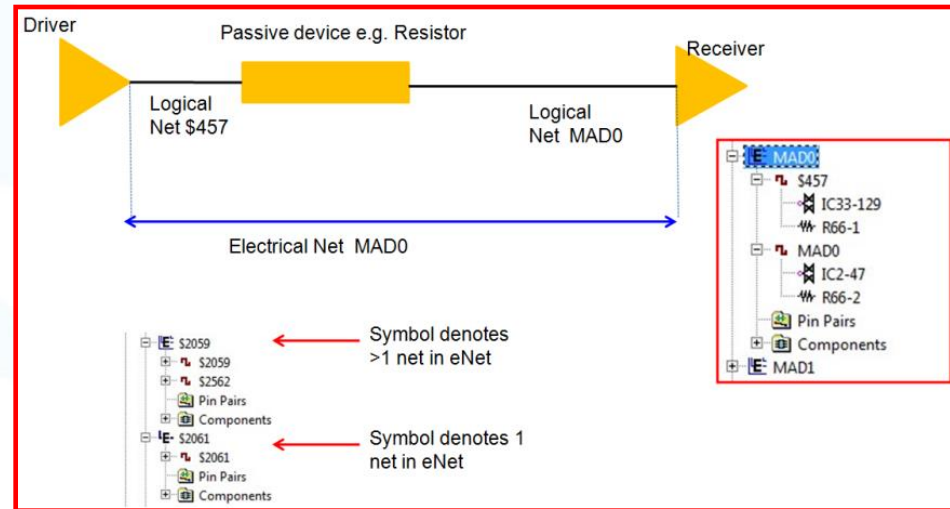
Constraint Definition Process

- > Automation
 - > Net conversion from Logical to Electrical
 - > Classification
- > Organisation
 - > Organisation
 - > Structure
- > Constraint Entry
 - > Group
 - > Net
 - > Pin-Pair



Automation - eNet Conversion

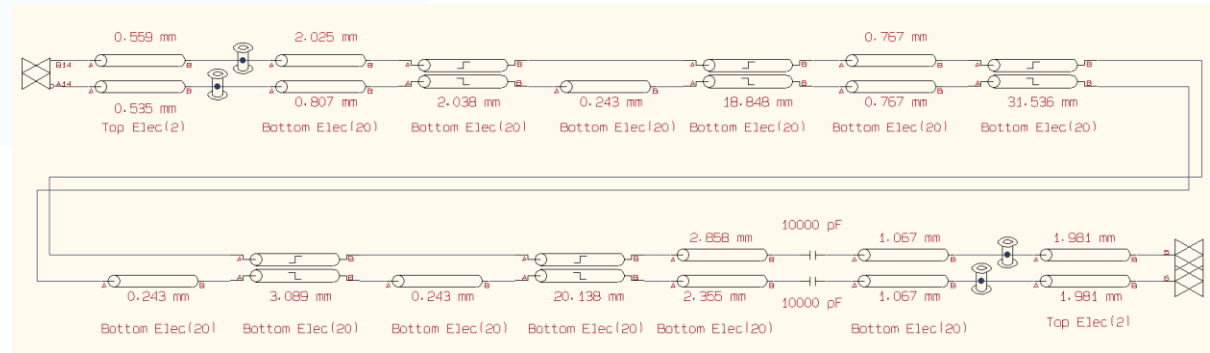
- > Concatenation of nets to include
 - > terminators
 - > Serial or Differential
 - > exclude power connections
 - > Pull up/down
 - > filtering



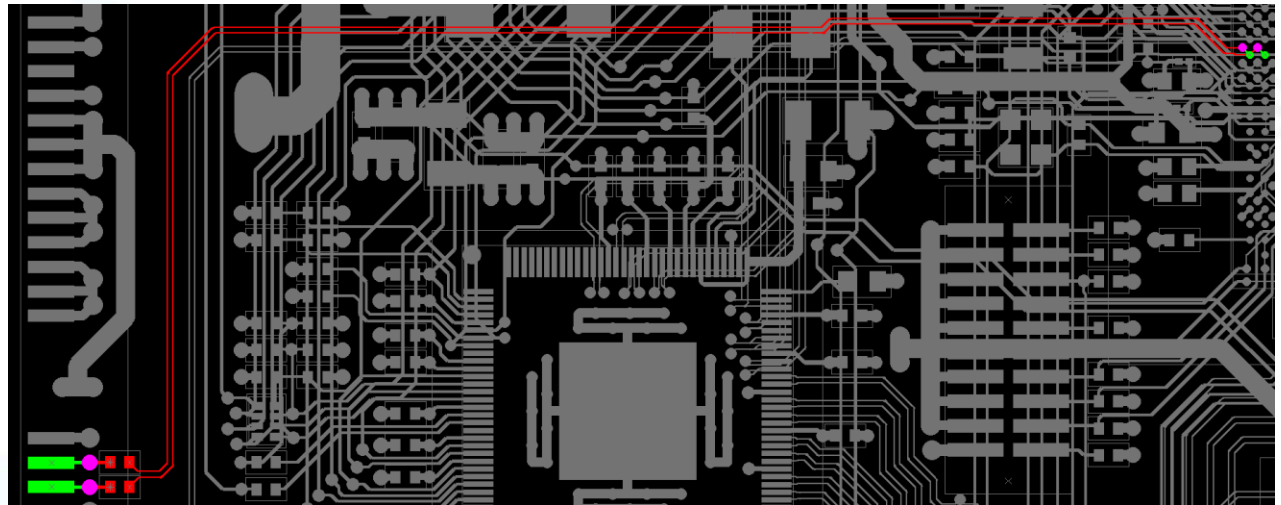
eNet Physical Results - Example

> Results


> Topology



> Routing

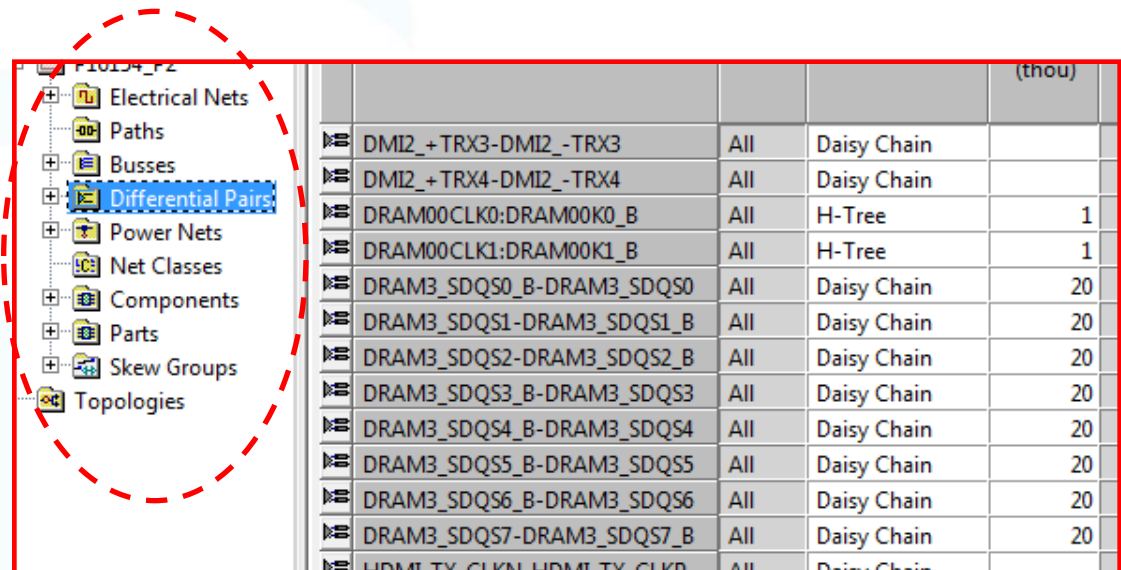


High Speed Design - Engineering Process

- 
- > Identify critical nets
 - > Busses, Diff Pair, Clocks....
 - > Establish constraint values
 - > Datasheet, Calculation, Signal Integrity Verification, other
 - > Implement net constraints
 - > Length, Delay, Skew, Topology
 - > Build constraint groups
 - > Busses, Groups, Nets, Pins
 - > Action Place & Route
 - > To physical design rules
 - > To Constraints
 - > Extend Analysis and Verification
 - > Measure, analyse and simulate
 - > HighSpeed Router
 - > Signal Integrity
 - > Power Integrity
 - > 3D
 - > Document Results
 - > Verify conformance of the design to initial objectives
 - > Statistics
 - > Reports

Constraints - Classification

- > Automatic extraction
 - > Power Nets
 - > Component Types & Values
 - > Busses
 - > Differential Pairs



				(thou)
DMI2_+TRX3-DMI2_-TRX3	All	Daisy Chain		
DMI2_+TRX4-DMI2_-TRX4	All	Daisy Chain		
DRAM0CLK0:DRAM0K0_B	All	H-Tree	1	
DRAM0CLK1:DRAM0K1_B	All	H-Tree	1	
DRAM3_SDQS0_B-DRAM3_SDQS0	All	Daisy Chain	20	
DRAM3_SDQS1-DRAM3_SDQS1_B	All	Daisy Chain	20	
DRAM3_SDQS2-DRAM3_SDQS2_B	All	Daisy Chain	20	
DRAM3_SDQS3_B-DRAM3_SDQS3	All	Daisy Chain	20	
DRAM3_SDQS4_B-DRAM3_SDQS4	All	Daisy Chain	20	
DRAM3_SDQS5_B-DRAM3_SDQS5	All	Daisy Chain	20	
DRAM3_SDQS6_B-DRAM3_SDQS6	All	Daisy Chain	20	
DRAM3_SDQS7-DRAM3_SDQS7_B	All	Daisy Chain	20	
HDMI_TX_CLKN-HDMI_TX_CLKP	All	Daisy Chain		

Start>

> Create structure in the design with:

- > Net Class
- > Bus
- > Sub-Bus
- > Diff Pair
- > Pin Pair
- > Path

	Path	Direction	Signal	Length	Delay	Capacitance	Inductance	Resistance	Capacitance	Inductance	Resistance
Buses	D2+-D2-	All	Daisy Chain						63	77	
	D1+-D1-	All	Daisy Chain						63	77	
	DA1_In-DB1_In	All	Daisy Chain						63	77	
	DA2_In-DB2_In	All	Daisy Chain						63	77	
	Ethernet_RX+-Ethernet_RX-	All	Daisy Chain						63	77	
	Ethernet_TX+-Ethernet_TX-	All	Daisy Chain						63	77	
	Address Bus A[0-24]	All							63	77	
	Control	All							63	77	
	Data_Bus_D[0-31]	All							63	77	
	SubBus1	All							63	77	
	SubBus2	All							63	77	
	SubBus3	All							63	77	
	SubBus4	All							63	77	
	Outputs	All							63	77	
	USB	All							63	77	
Differential Pairs	D1+-D1-	All							63	77	
	D2+-D2-	All							63	77	
	DA1_In-DB1_In	All							63	77	
	DA2_In-DB2_In	All							63	77	
	Ethernet_RX+-Ethernet_RX-	All							63	77	
Power Nets	Ethernet_TX+-Ethernet_TX-	All							63	77	

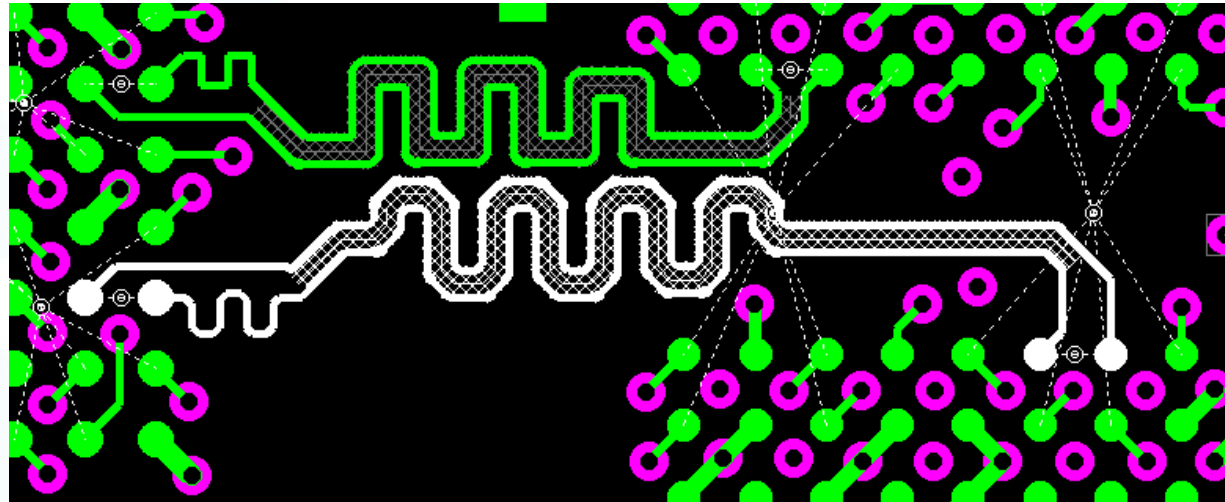
Constraint – Assigning Values

- > Topology
- > Impedance Profile
- > Skew Groups
 - > Simple
 - > Relative
- > Intra-Net Skew
 - > Virtual Branch Point
- > Length v. Delay Mode



Constraint Implementation

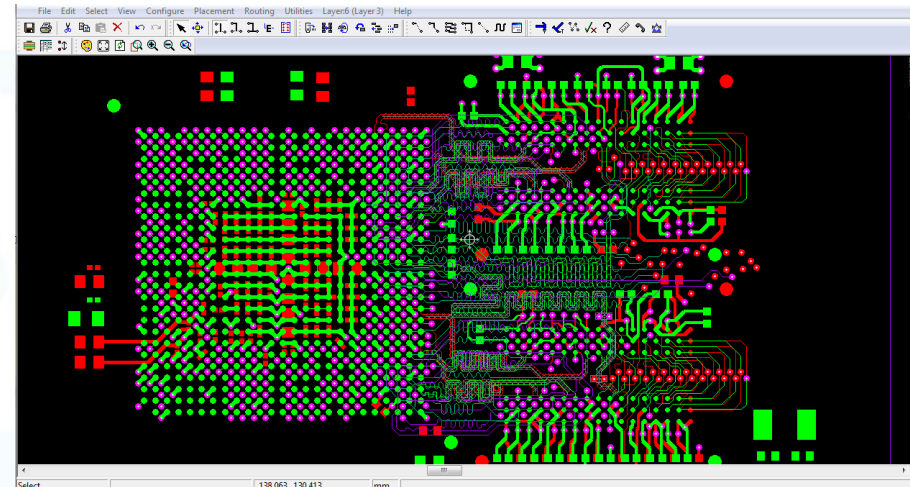
- > Place and Route
 - > Dynamic DRC
 - > Clearance
 - > Length
 - > Delay



Start>

Constraint Verification

- > Dynamic
 - > Length / Delay markers
 - > Pop-up
- > Signal Integrity
- > Power Integrity
 - > EMC
 - > Power distribution
 - > Decoupling

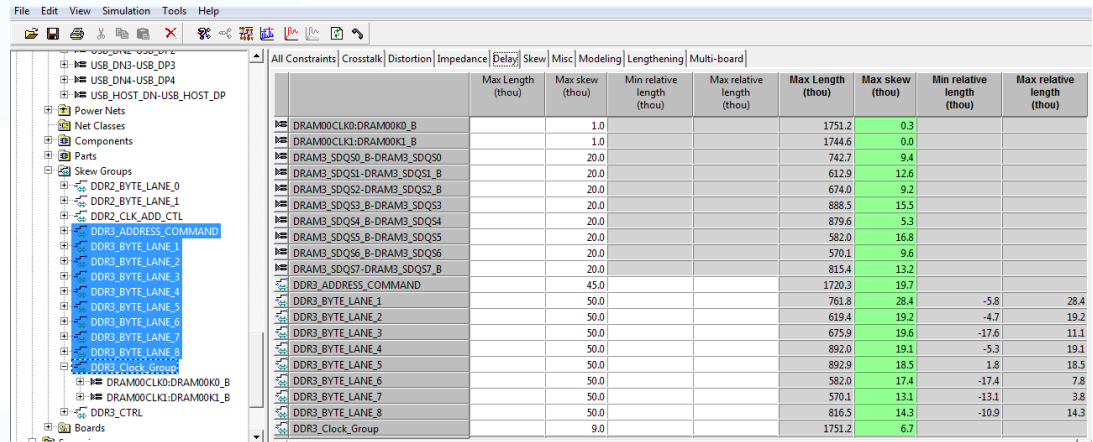


Start>

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Constraint Documentation

- > Spreadsheet
- > Reports
 - > DRC
 - > Skew
 - > Length
 - > Delay
- > Embed links in Schematic and PCB

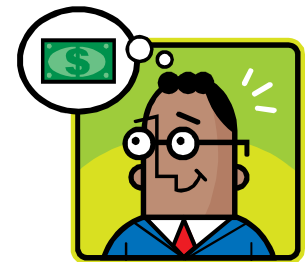


The screenshot shows a software window with a tree view on the left and a table of constraints on the right. The tree view includes categories like USB, Power Nets, Net Classes, Components, Parts, Skew Groups, and Boards. The table on the right is titled 'All Constraints' and has columns for various constraint metrics. The data is as follows:

	Max Length (thou)	Max skew (thou)	Min relative length (thou)	Max relative length (thou)	Max Length (thou)	Max skew (thou)	Min relative length (thou)	Max relative length (thou)
DRAM0CLK0-DRAM0K0_8		1.0			1751.2	0.3		
DRAM0CLK1-DRAM0K1_8		1.0			1744.6	0.0		
DRAM3_SQSQ0_8-DRAM3_SQSQ0_8	20.0				742.7	9.4		
DRAM3_SQSQ1-DRAM3_SQSQ1_8	20.0				612.9	12.6		
DRAM3_SQSQ2-DRAM3_SQSQ2_8	20.0				674.0	9.2		
DRAM3_SQSQ3_8-DRAM3_SQSQ3_8	20.0				888.5	15.5		
DRAM3_SQSQ4_8-DRAM3_SQSQ4_8	20.0				879.6	5.3		
DRAM3_SQSQ5_8-DRAM3_SQSQ5_8	20.0				582.0	16.8		
DRAM3_SQSQ6_8-DRAM3_SQSQ6_8	20.0				570.1	9.6		
DRAM3_SQSQ7-DRAM3_SQSQ7_8	20.0				815.4	13.2		
DDR3_ADDRESS_COMMAND	45.0				1720.3	19.7		
DDR3_BYTE_LANE_1	50.0				761.8	28.4	-5.8	28.4
DDR3_BYTE_LANE_2	50.0				619.4	19.2	-4.7	19.2
DDR3_BYTE_LANE_3	50.0				675.9	19.6	-17.6	11.1
DDR3_BYTE_LANE_4	50.0				892.0	19.1	-5.3	19.1
DDR3_BYTE_LANE_5	50.0				892.9	18.5	1.8	18.5
DDR3_BYTE_LANE_6	50.0				582.0	17.4	-17.4	7.8
DDR3_BYTE_LANE_7	50.0				570.1	13.1	-13.1	3.8
DDR3_BYTE_LANE_8	50.0				816.5	14.3	-10.9	14.3
DDR3_Clock_Group	9.0				1751.2	6.7		

Benefits of Integration - summary

- > For you and your colleagues
 - > Design, Layout, Production, Test
 - > Fast, Accurate, Secure, Repeatable
- > For your partners
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