sintecs
Excellence in Electronic Development

High-performance embedded systems

Presenter Hans Klos

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AGENDA

- Introduction Sintecs
- Trends that make Electronic designs complex
- Electronic Design Challenges
- High-Speed Board Analysis

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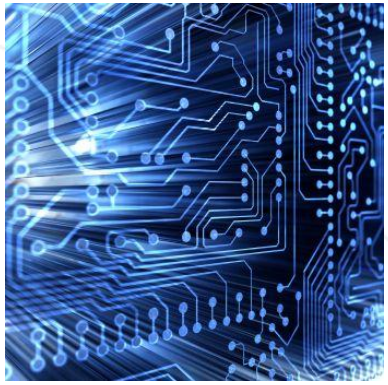
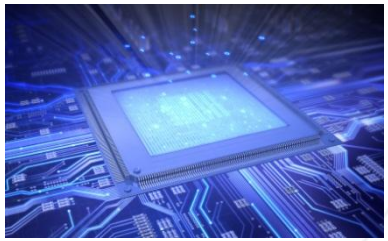
The Company Sintecs





- Started in 2000
- System design and services partner
- Core competences in electronic development, (embedded) software development and design analysis & verification
- System-On- Module supplier

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Freescale Proven Partner

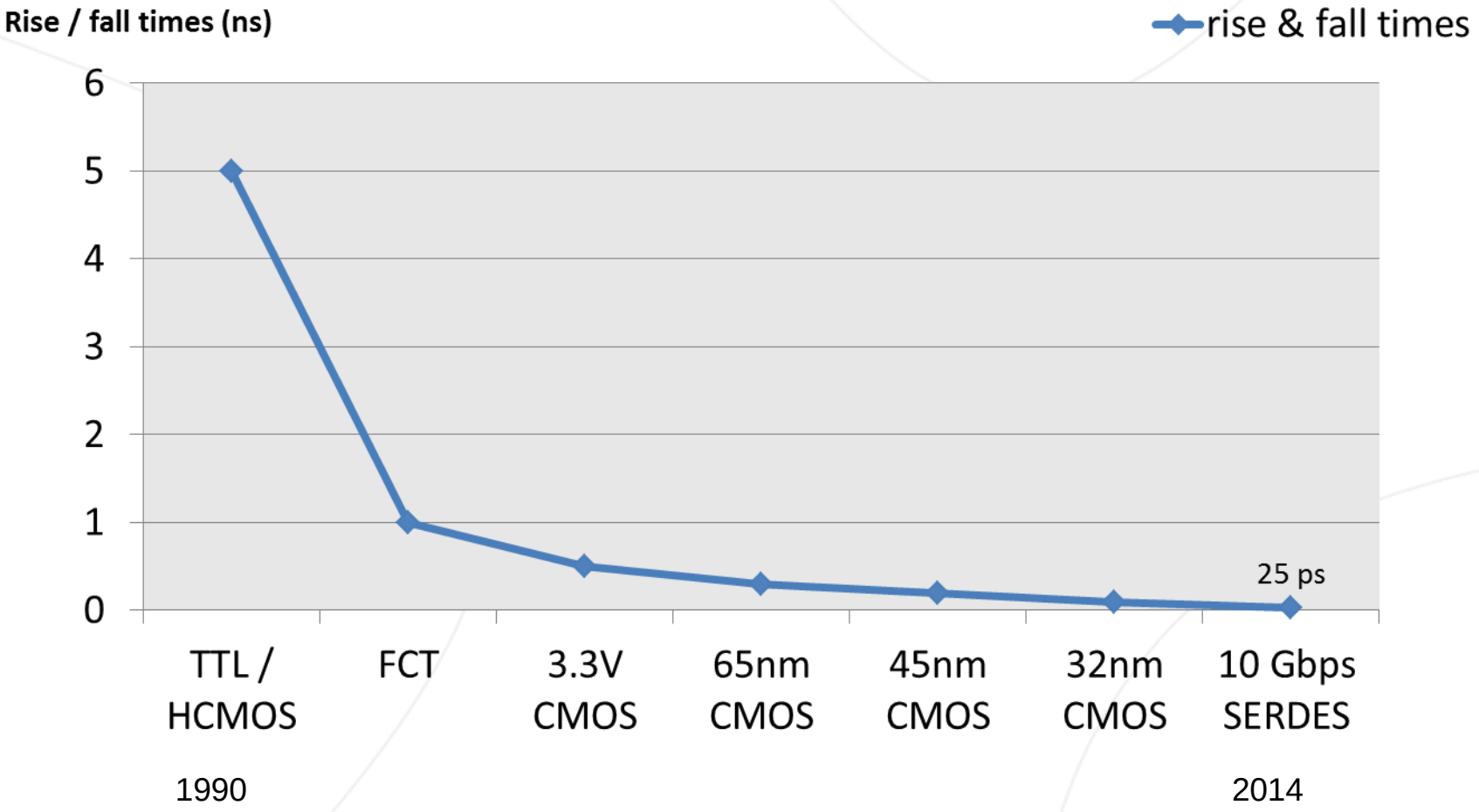
- System on Module development
  - Freescale i.MX processor family
  - Freescale QorIQ processor family
- Custom electronic development
  - Integrate module in customer design

Trends that make Electronic designs complex

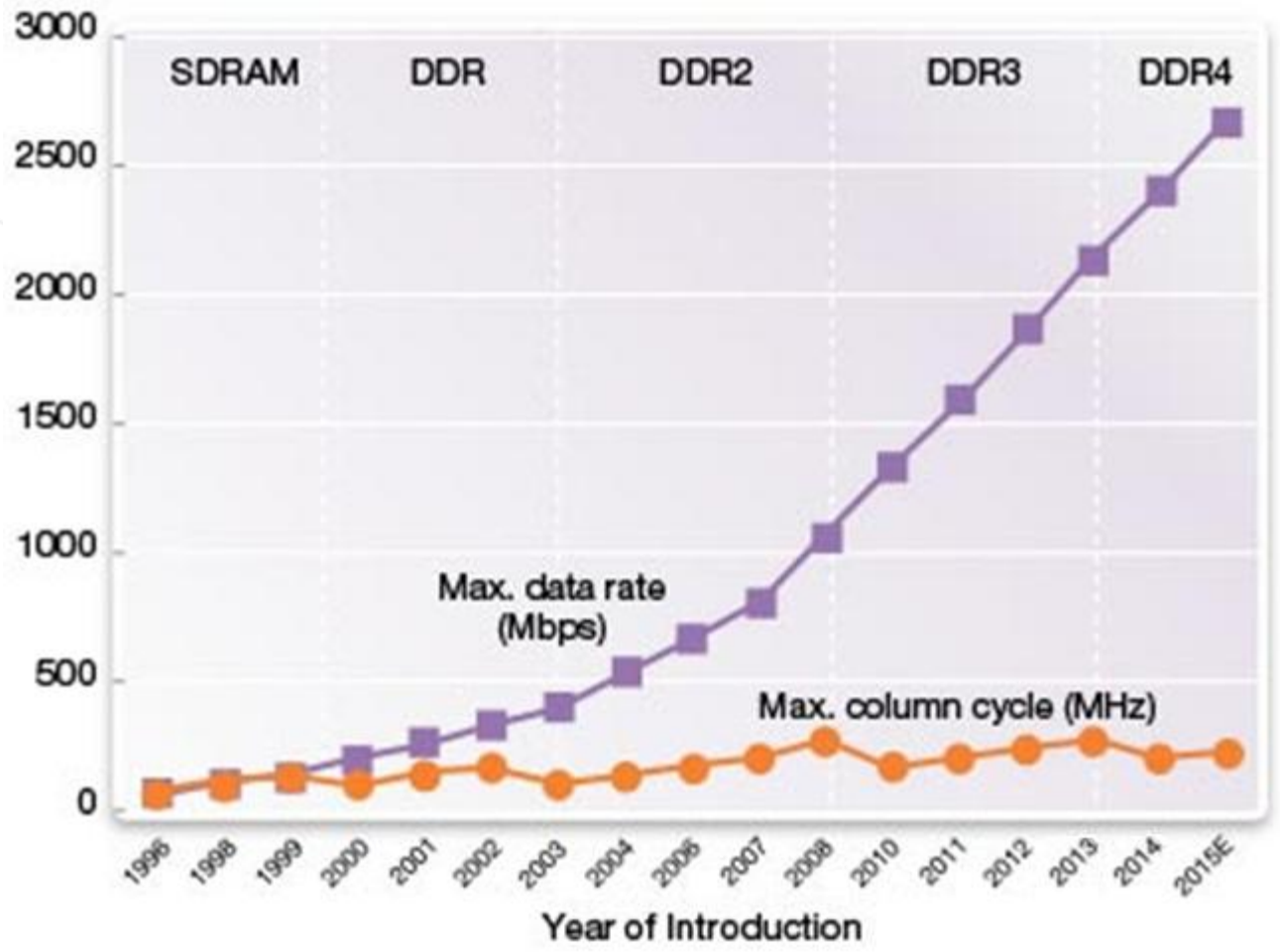
Trends

- Shorter Rise & fall time
- Increasing Data Rate & Bandwidth
- Lower power supply voltage
- Higher currents
- Dense & larger pin count devices / smaller pitch

Rise & Fall times



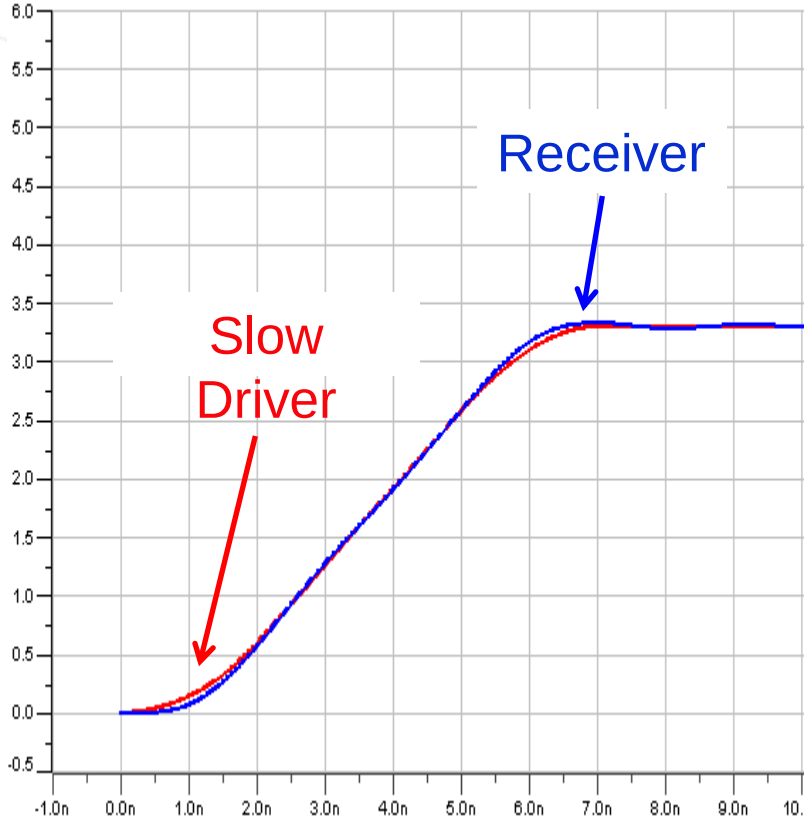
Increasing Data Rate

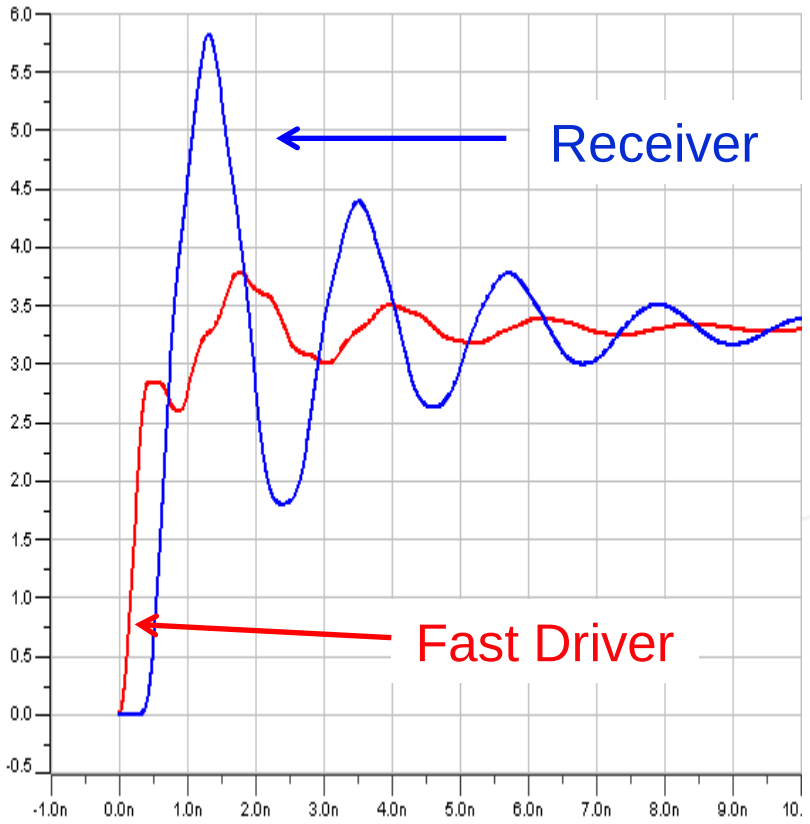


Challenges

- Fast switching devices
- Packages
- Device loading
- Number of power rails
- Multi Gigabit signaling

Rise & Fall times





Both are the same trace

Routing challenges

DDR3 routing guidelines for a Xilinx Kintex 7

Match within a byte lane all the DQ, DM and DQS within 5ps → within less than 1 mm

- The maximum electrical delay between any DQ and its associated DQS/DQS# should be ±5 ps.
- The maximum electrical delay between any address and control signals and the corresponding CK/CK# should be ±25 ps.
- The maximum electrical delay of any DQS/DQS# should be less than that of CK/CK#.

DDRx timing simulation needed!

Packages

Example from the Xilinx Kintex 7 datasheet

Table 50: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC7K70T	FBG484	108	ps
			FBG676	135	ps
		XC7K160T	FBG484	118	ps
			FBG676	136	ps
			FFG676	161	ps
		XC7K325T	FBG676	146	ps
			FFG676	154	ps
			FBG900	163	ps
			FFG900	161	ps
		XC7K355T	FFG901	149	ps
		XC7K410T	FBG676	165	ps
			FFG676	168	ps
			FBG900	151	ps
			FFG900	146	ps
		XC7K420T	FFG901	149	ps
			FFG1156	145	ps
		XC7K480T	FFG901	149	ps
			FFG1156	145	ps

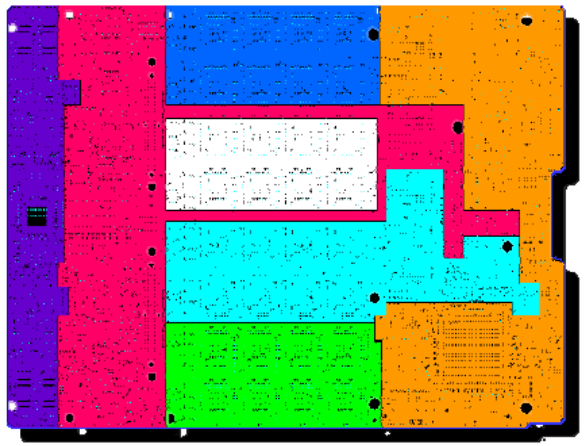
168ps worst case package skew ~ 20 mm

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Number of Power Rails / Area fills

- Number of Power Rails / Area fills
- Small pitch BGA’s
- Planes are not low impedance any more



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High-speed board analysis

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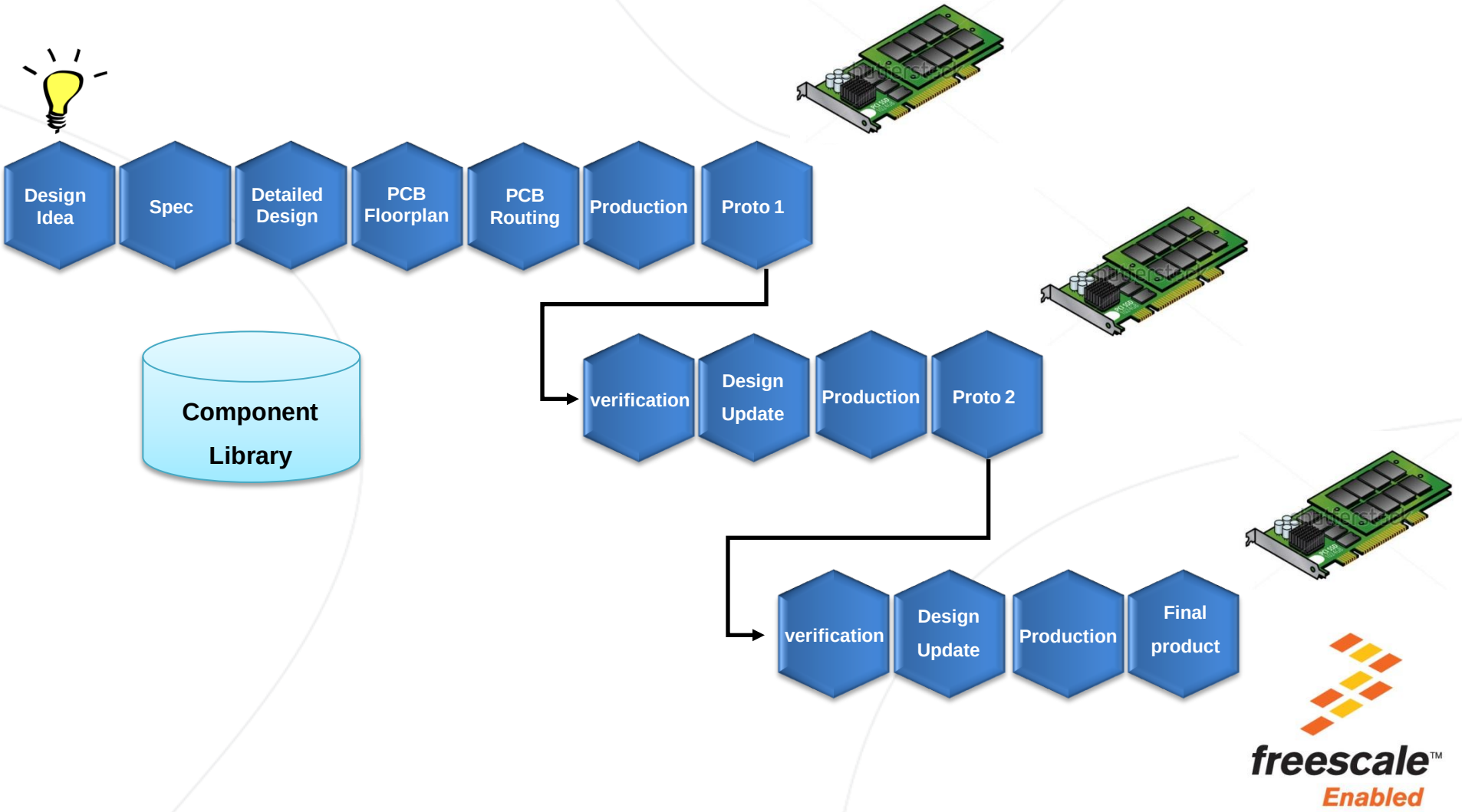
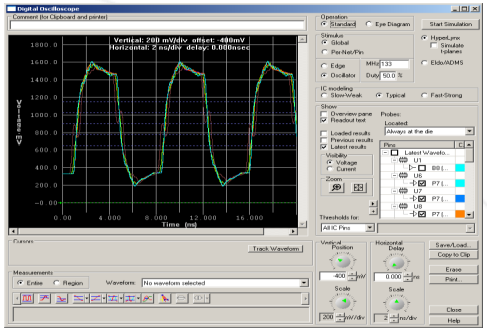
Traditional electronic design flow

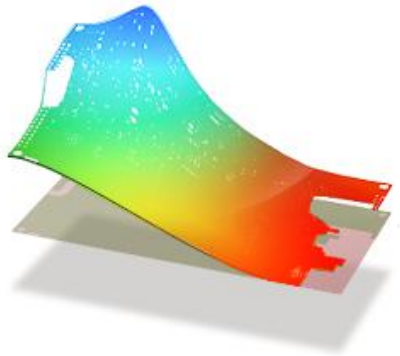


High-speed board analysis

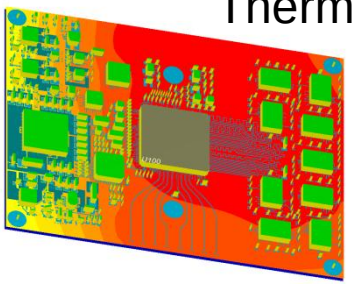
Signal Integrity



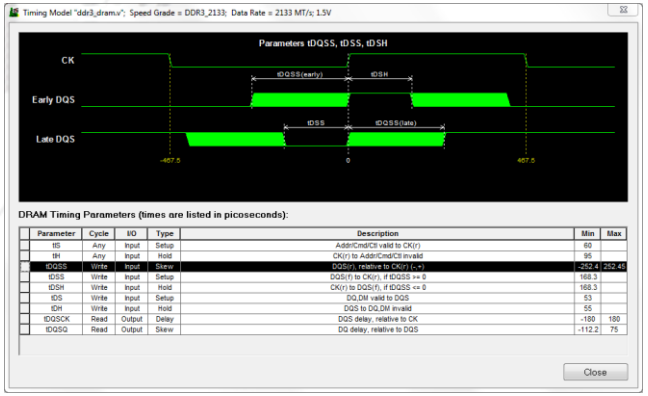
Power Integrity



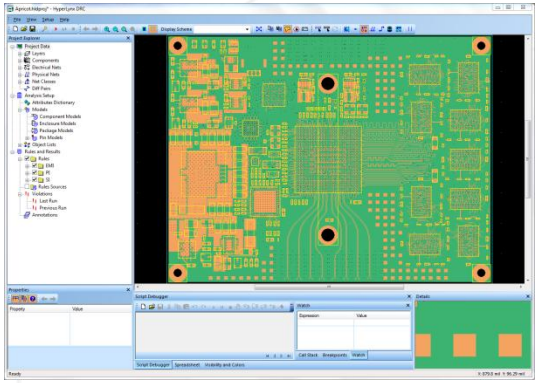
Thermal



DDRx timing analysis



DRC



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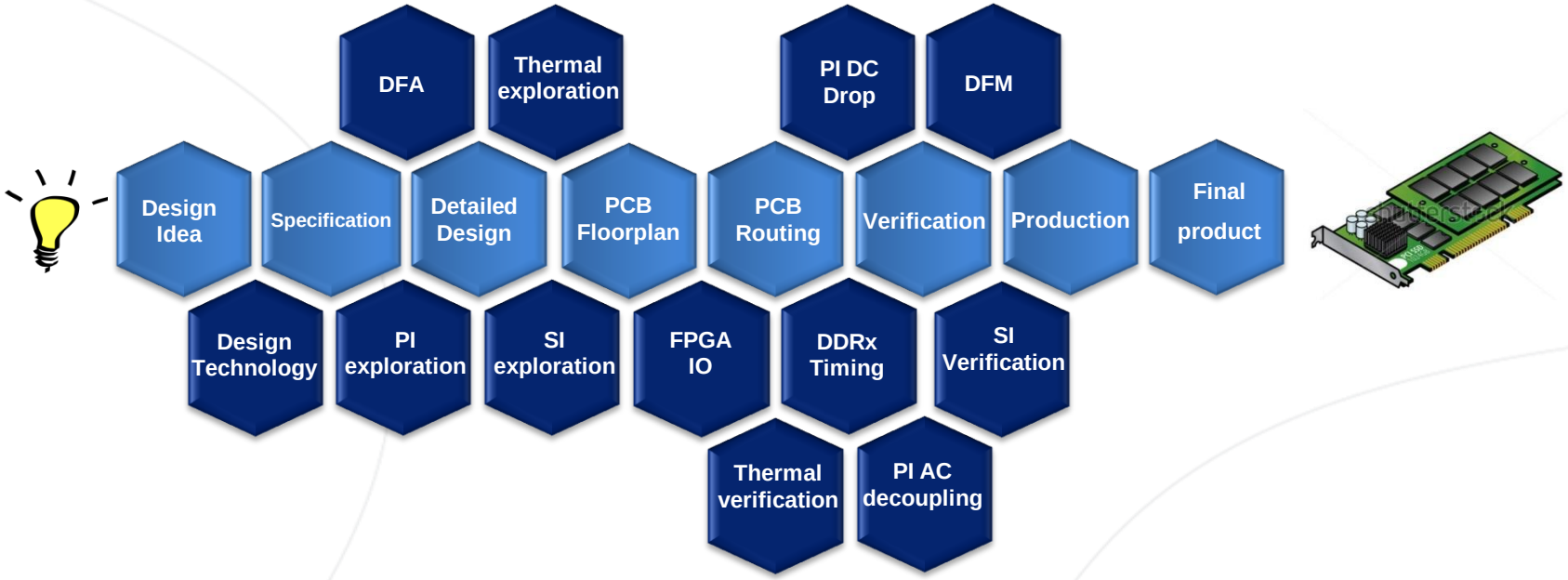
High-speed design flow

Component database:

Schematic symbols | Footprints | Simulation models (SI /PI / Thermal / Timing)



Design Constraints

PCB Technology | Electrical constraints | Physical constraints

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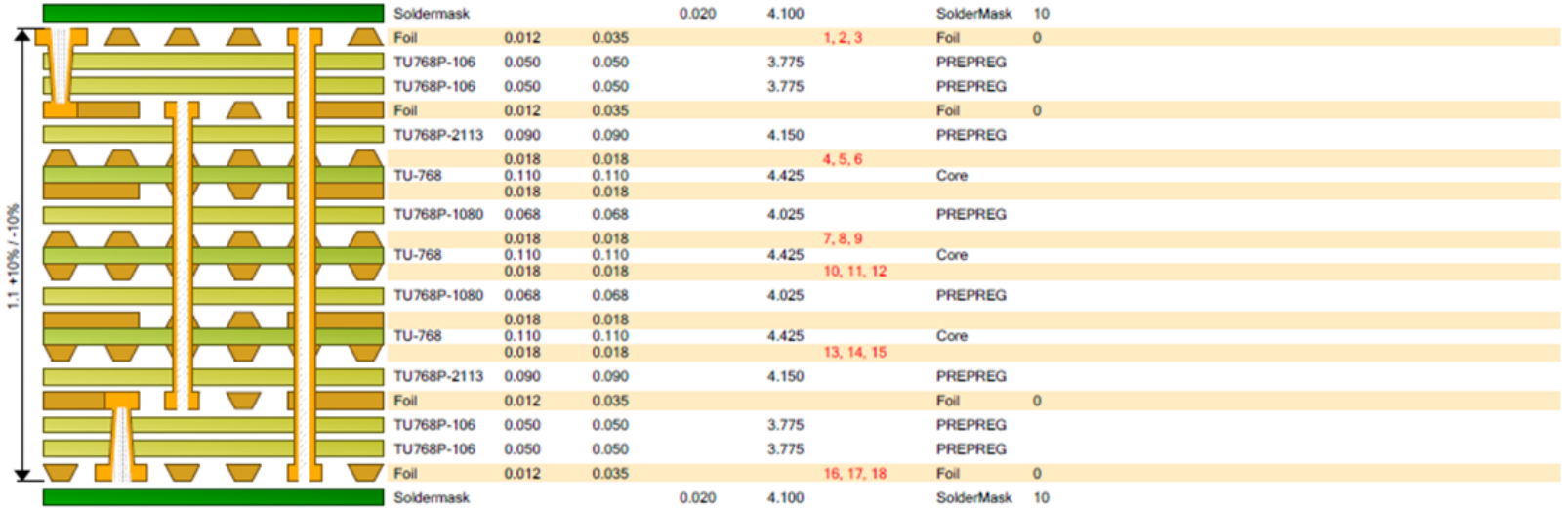
Design technology setup

- Explore which impedances are needed on the board
- How many signal and power planes are needed
  - What is smallest pitch of BGA's
  - How many power rails?



Layer	Stack up	Description	Base Thickness	Finish Thickness	Mask Thickness	er	Impedance ID	Type	Notes-1
		Soldermask			0.020	4.100		SolderMask	10
1		Foil	0.012	0.035			1, 2, 3	Foil	0
		TU768P-106	0.050	0.050		3.775		PREPREG	
		TU768P-106	0.050	0.050		3.775		PREPREG	
2		Foil	0.012	0.035				Foil	0
		TU768P-2113	0.090	0.090		4.150		PREPREG	
3			0.018	0.018			4, 5, 6		
		TU-768	0.110	0.110		4.425		Core	
4			0.018	0.018					
		TU768P-1080	0.068	0.068		4.025		PREPREG	
5			0.018	0.018			7, 8, 9		
		TU-768	0.110	0.110		4.425		Core	
6			0.018	0.018			10, 11, 12		
		TU768P-1080	0.068	0.068		4.025		PREPREG	
7			0.018	0.018					
		TU-768	0.110	0.110		4.425		Core	
8			0.018	0.018			13, 14, 15		
		TU768P-2113	0.090	0.090		4.150		PREPREG	
9		Foil	0.012	0.035				Foil	0
		TU768P-106	0.050	0.050		3.775		PREPREG	
		TU768P-106	0.050	0.050		3.775		PREPREG	
10		Foil	0.012	0.035			16, 17, 18	Foil	0
		Soldermask			0.020	4.100		SolderMask	10

Copper Thickness = 0.247 | Dielectric Thickness = 0.846 | Solder Mask Thickness = 0.040 | Stack Up Thickness = 1.093 | Stack Up Thickness with Solder Mask = 1.133 |

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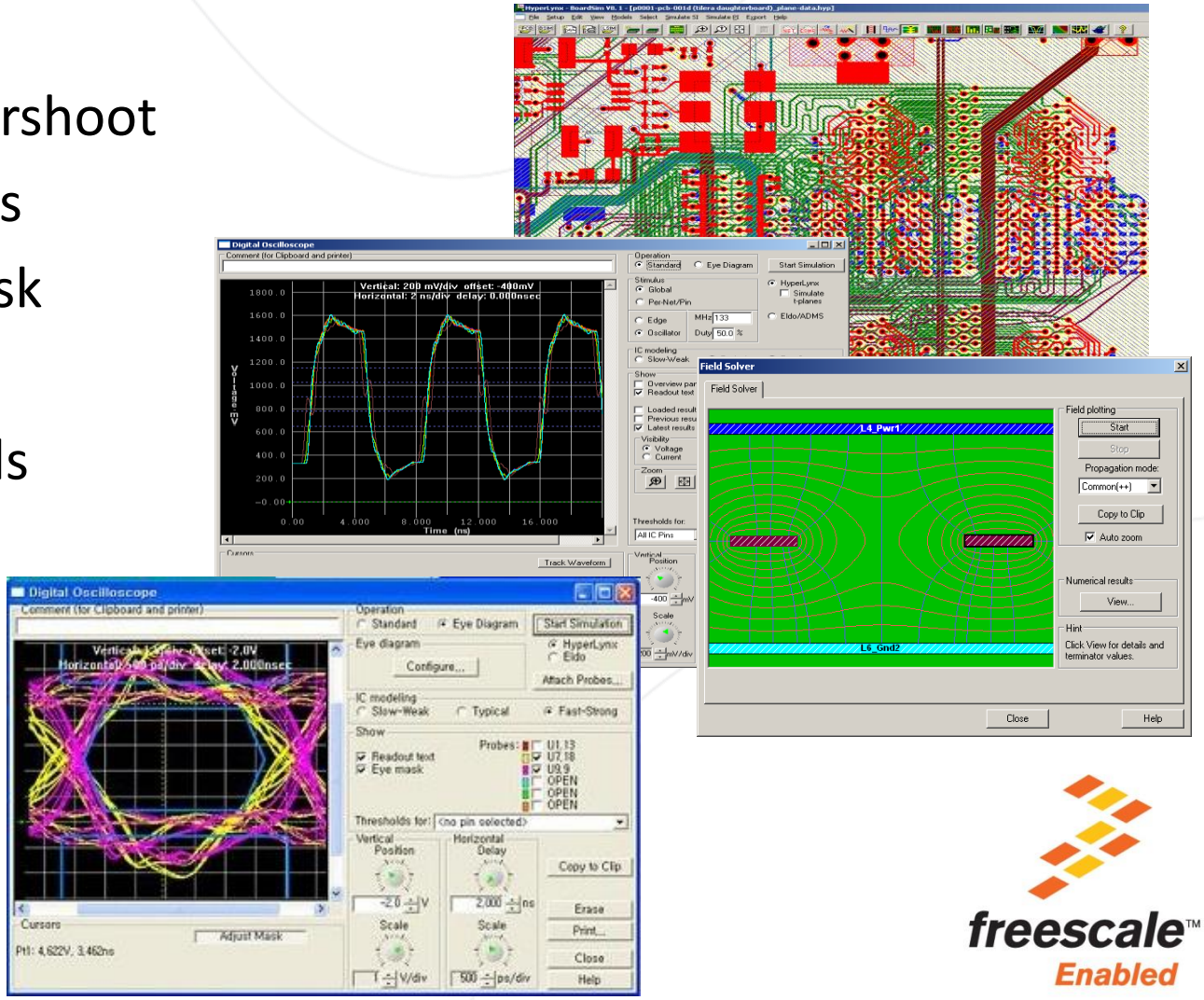
Signal Integrity

- Signal over/undershoot
- Trace impedances
- Eye Pattern / Mask
- Crosstalk
- Monotonic signals



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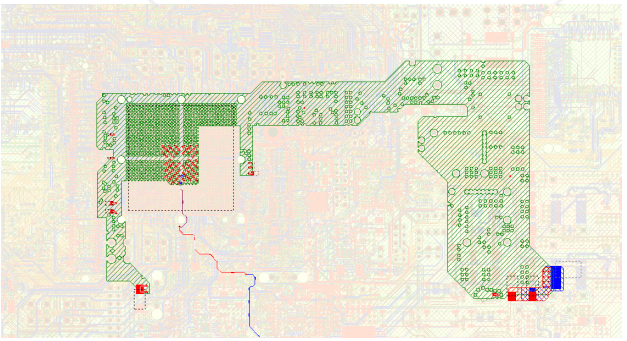
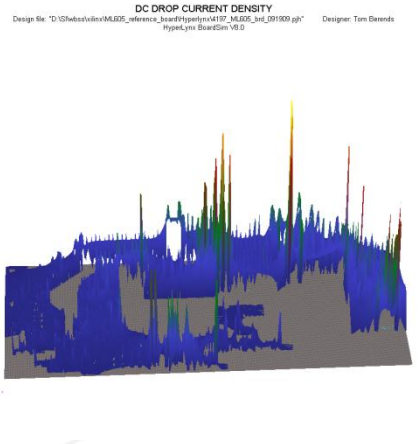
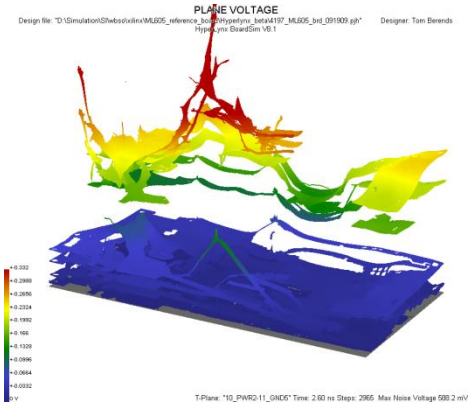
Power Integrity

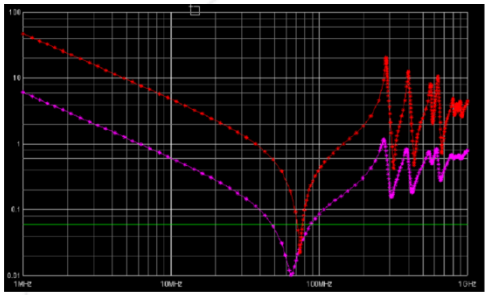
- **DC analysis**
  - Voltage drop
  - Current densities





- **AC analysis**
  - decoupling / Target impedance
  - Plane noise





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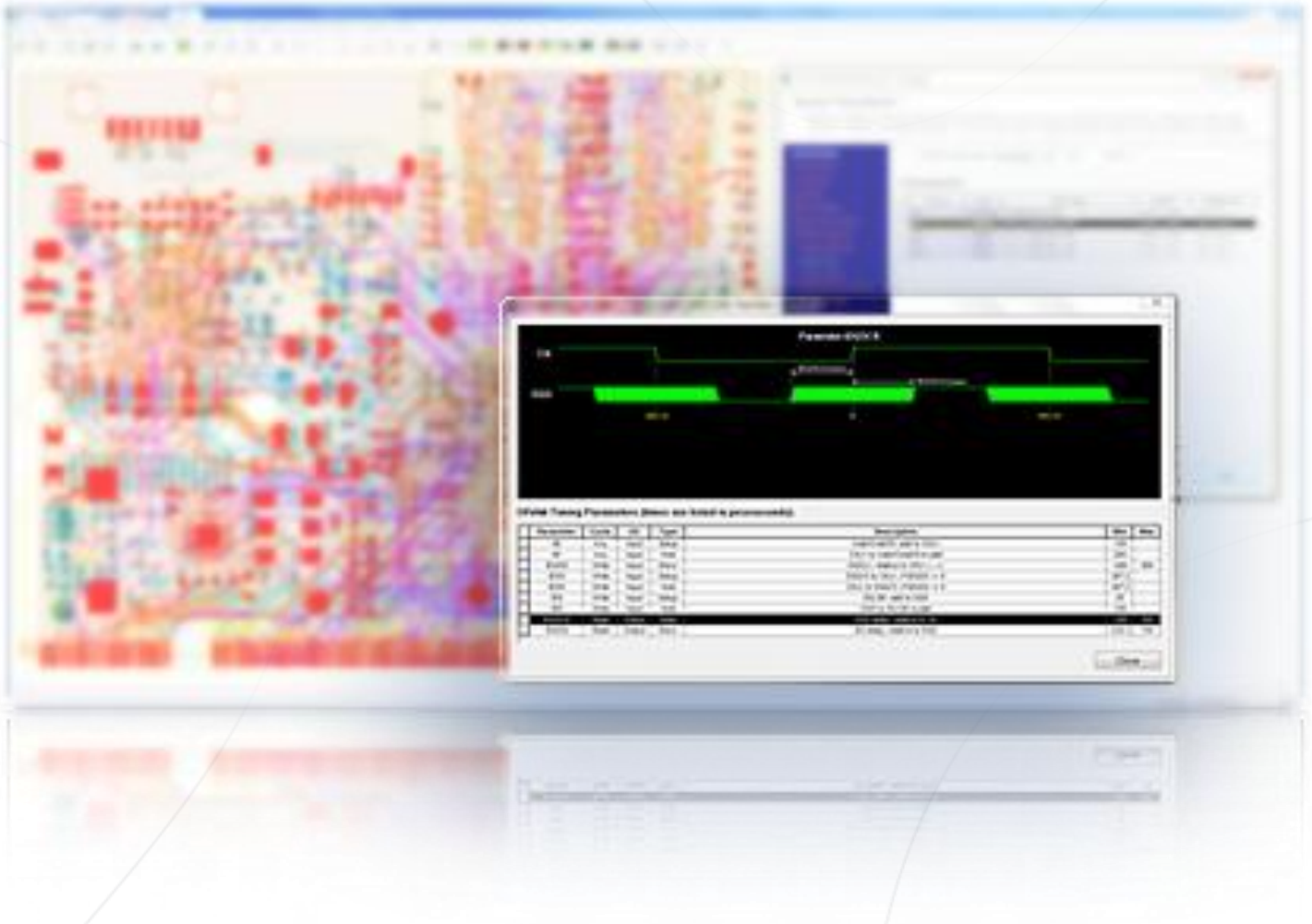
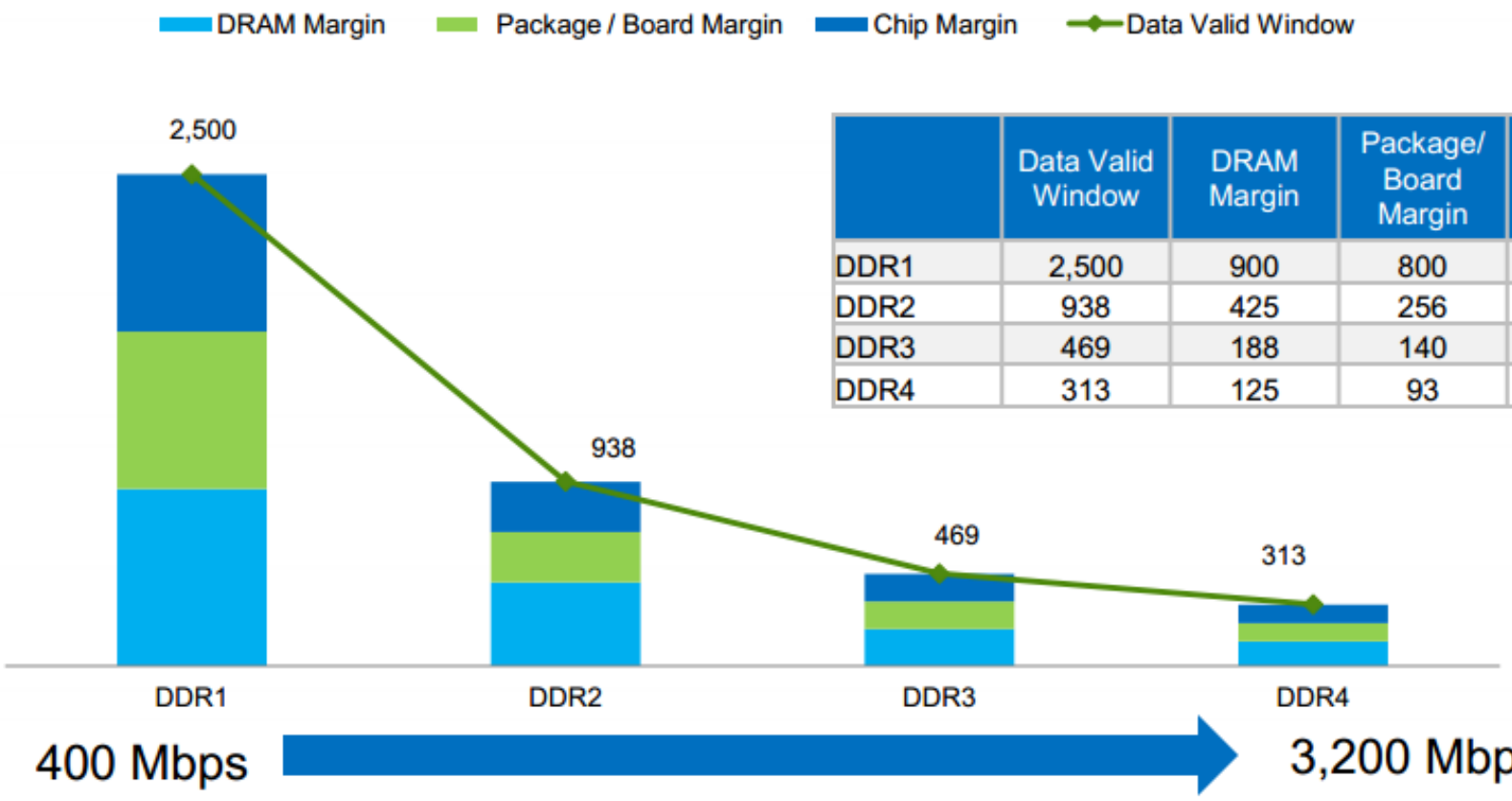
DDRx timing



DDRx timing margins

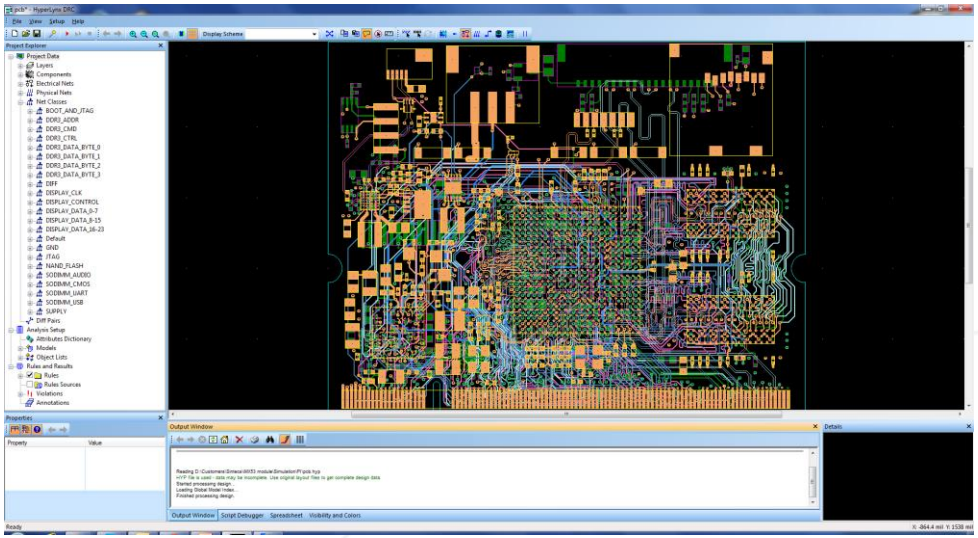


	Data Valid Window	DRAM Margin	Package/ Board Margin	Chip Margin
DDR1	2,500	900	800	800
DDR2	938	425	256	256
DDR3	469	188	140	140
DDR4	313	125	93	93

Only 93ps board/package margin ~10mm

Design Rule Checks

- Use Design Rules checker for e.g. following check:
  - Trace crossing gaps
  - IO coupling
  - Reference plane change
  - IC's over split
  - Traces near plane edge
  - Decoupling placement
  - Power/Ground width
  - Long nets
  - …..



Summary

- A good high-speed design starts with understanding of different hiigh-speed effects which can have impact on your design
- Try to develop first-time right
  - When you plan 2 proto types, you will get 2 proto types
- Make use of high-speed board analysis tools

Thank you!

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