Plessey GaN-on-Silicon LED

The Impact of GaN-on-Silicon on SSL

2nd December 2014

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Plessey: An innovative technology design and manufacturing company

1917 — Plessey founded as a mechanical engineering company

1957 — Plessey Electronics and Equipment Group set up and Plessey Semiconductors founded; first Integrated Circuit model produced

2010 — Plessey re-launched from the Swindon and Plymouth facilities

2011 — Market-leading sensor technology developed alongside legacy product sales

2012 — Acquisition of CamGaN provides access to ground-breaking LED technology

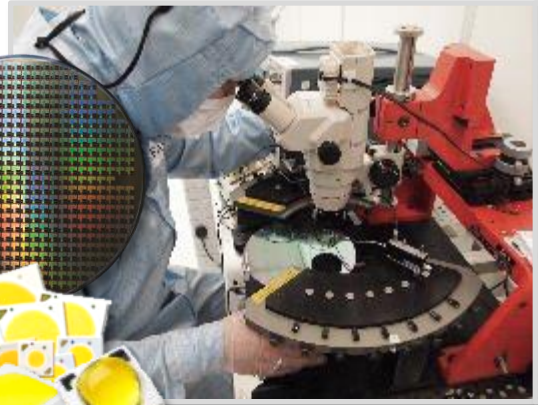
Transfer of experimental recipe onto production tool completed

2013

- Plessey doubles efficacy within the year, from 32 to 64lm/W
- Plessey produces world's first commercial LEDs manufactured on 6" (150mm) diameter silicon substrates

2014 AND ONWARDS

- Mainstream GaN-on-Si production
- 10 reactors installed at Plymouth facility
- Expanded product range
- Efficacy at 100lm/W, and higher



Plessey's LED Fab In Plymouth

- Plessey-owned land and buildings: ~53,000m^2. operational plus an additional ~60,000 m^2 of property for expansion
- Manufacturing standards ISO9001, TS16949 (automotive), ISO14001, OHSAS 18001

Two wafer manufacturing lines

- 8-inch (200mm) wafer manufacturing facility: 1,550sqm, Class 1000, with better than Class 1 SMIF mini environment
- 6-inch (150mm) wafer manufacturing line: 1,200sqm, Class 10: GaN-on-Si for LED and power devices




LED Technology

MaGIC™ — Manufactured on GaN-on-Si I/C

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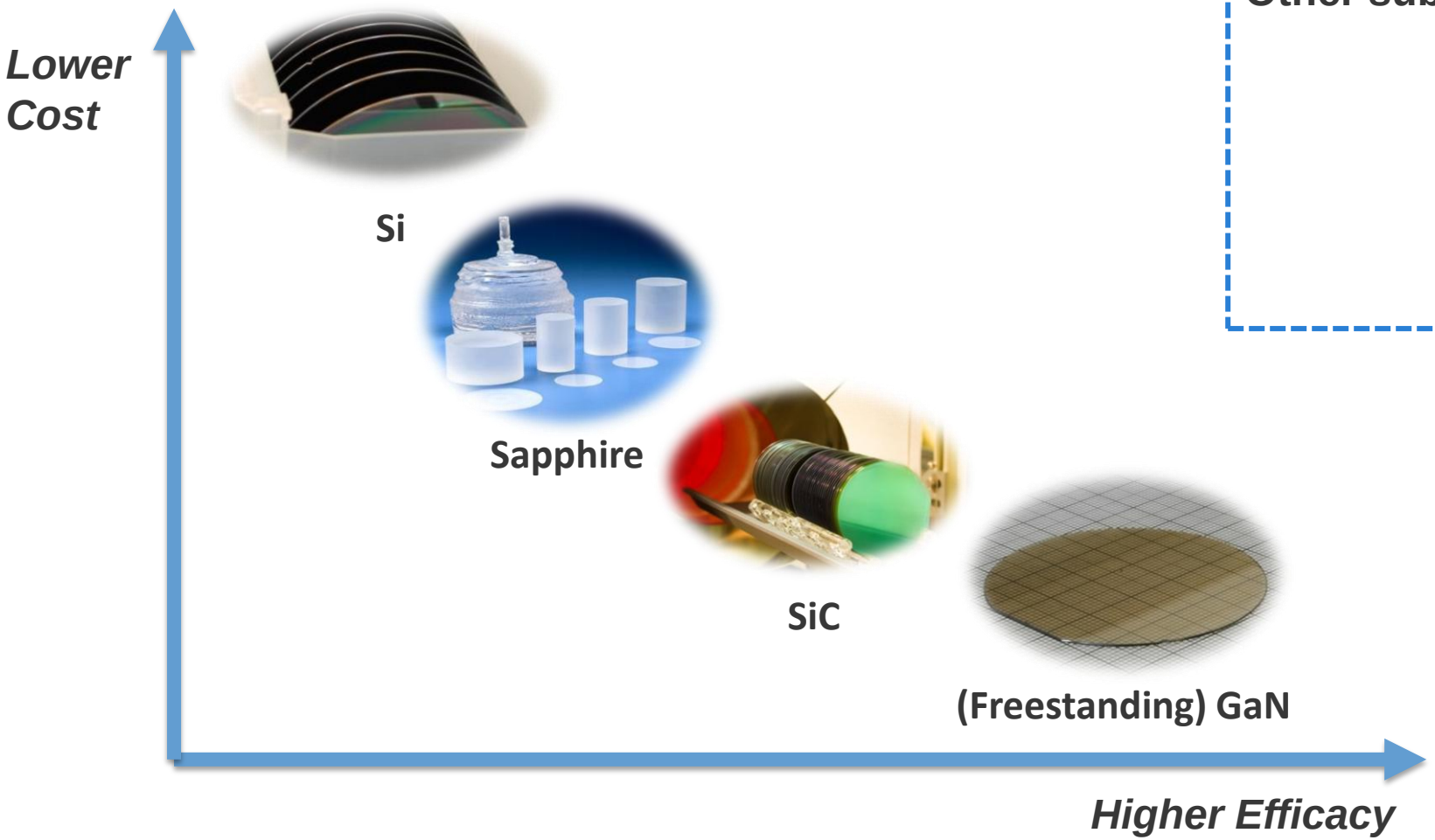
Substrates for Gallium Nitride growth



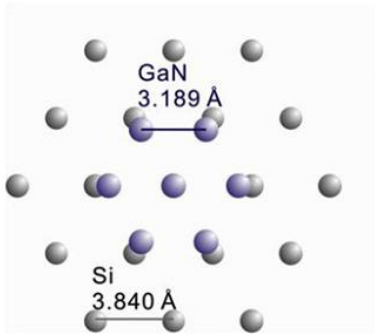
Other substrates:

$LiAlO_2$
$MgAlO_2$
ZnO
Glass
…

Courtesy:
led-professional.com
compoundsemiconductor.net
lux123.ezweb1-2.35.com

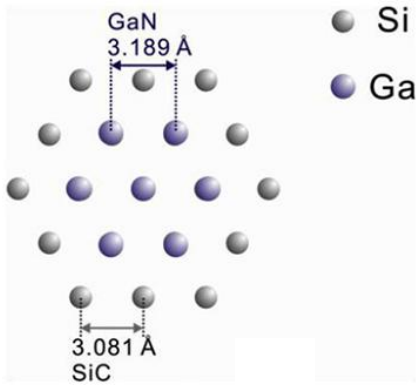
What makes GaN-on-Si growth difficult?

1) 17% Lattice mismatch between GaN and Si → High defect density
2) 54% Thermal mismatch (CTE) → Material cracks upon cooling
3) Meltback etching → 3D defects causing poor yield



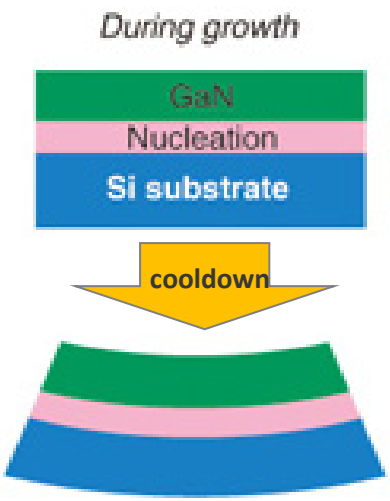
$$\frac{\left|a_{GaN} - \sqrt{2}\, a_{Si}/2\right|}{\sqrt{2}\, a_{Si}/2} = 17\%$$

Si



$$\frac{\left|a_{GaN} - a_{SiC}\right|}{a_{SiC}} = 3.5\%$$

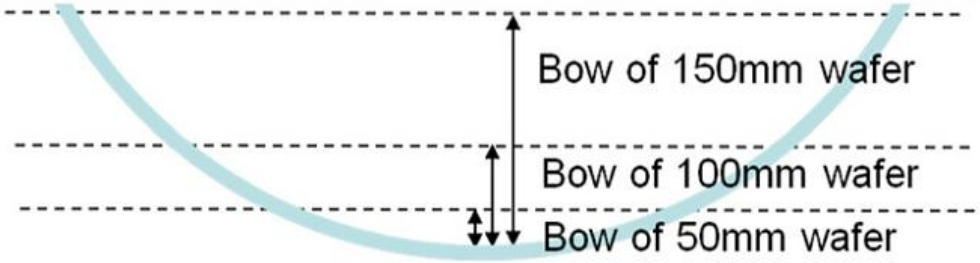
SiC

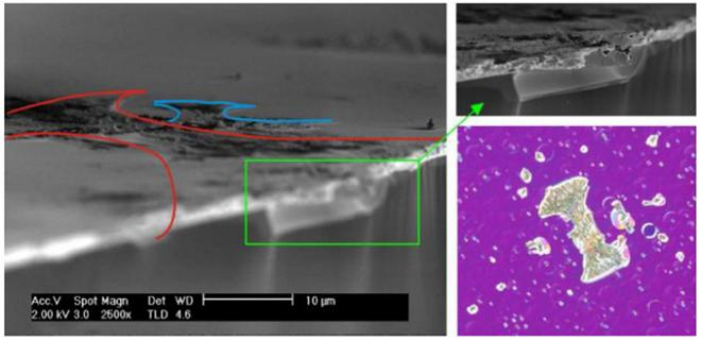


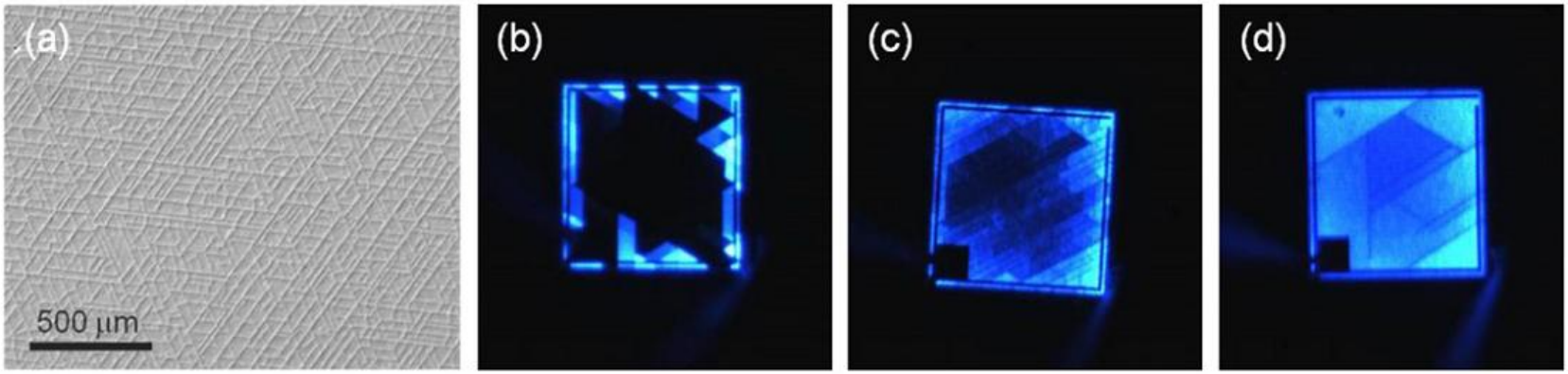
GaN under tensile stress after cooldown

1 2 3

What makes GaN-on-Si growth difficult?







Courtesy:
Rep. Prog. Phys. ***76*** *(2013) 106501*

How Does Plessey tackle the issues?

- **Thermal mismatch**

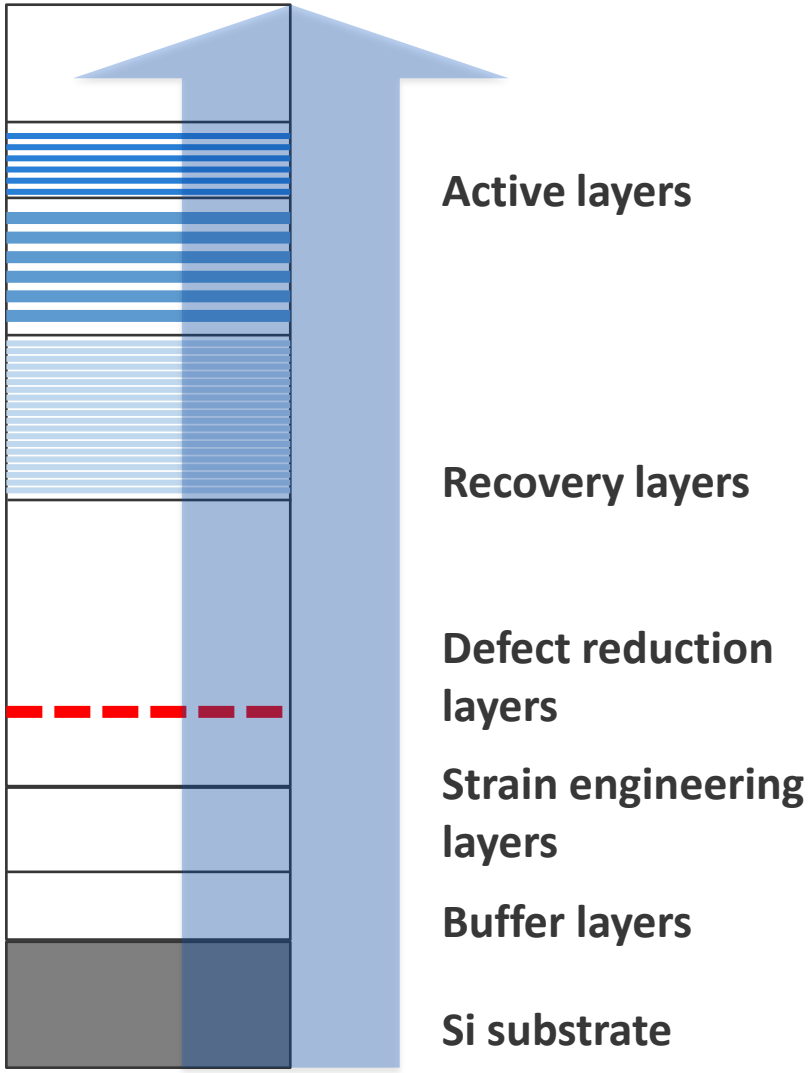
Strain engineering layers enables (0±10)um bow upon cool down

- **Lattice mismatch**

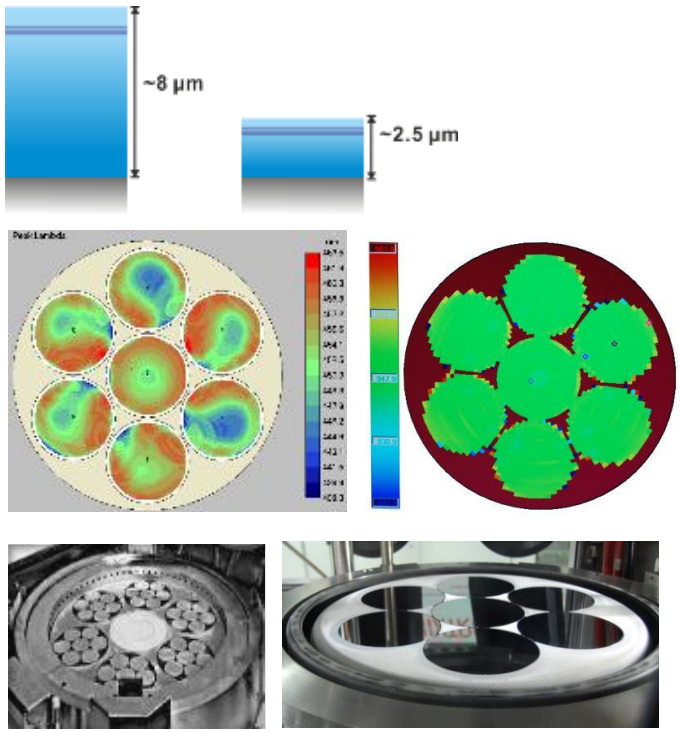
Recovery layers, defect reduction layers as well as strain engineering layers enable good material quality

- **Melt-back**

Special treatment of the substrate surface as well as buffer layers eliminate the melt-back effect



Plessey's GaN-On-Si Technology Benefits



42x2" sapphire V.S. 7x6" silicon

Features	lead to	Benefits
Si		Lower unit substrate costs
6"		Lower epitaxy costs
Thin-GaN		Lower processing costs
Automated processing		Higher throughput
		Higher yield

Other benefits include good wavelength uniformity and high binning yield; Increasing popularity with wafer scale packaging bodes well with GaN on Silicon

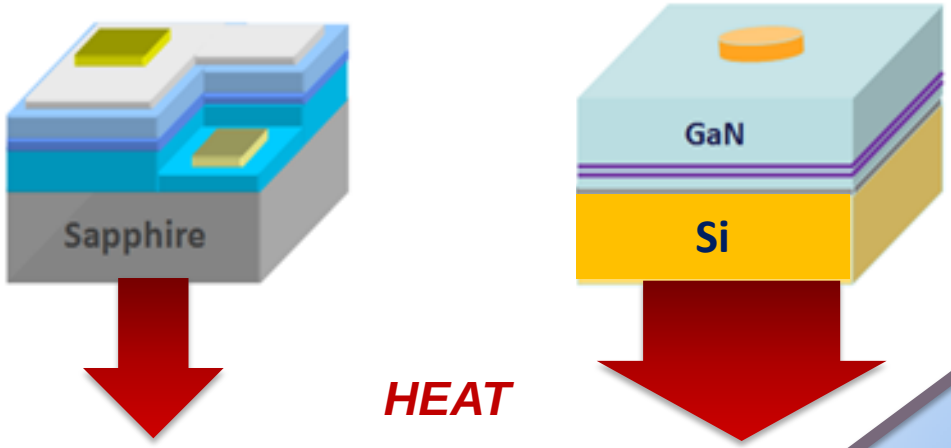
The Technical Advantages of our Technology (GaN on silicon)

Technical Features	*Technical USP's*
Material: Silicon	Better thermal performance
Chip Architecture: Surface emitting	A very focused light emitting area
	Less efficiency loss in big die
Process: Growth Process Control	Better on-wafer uniformity

Better thermal performance

Si 149 W/m·K

Sapphire 27 W/m·K



Three dimensions to leverage the better thermal performance

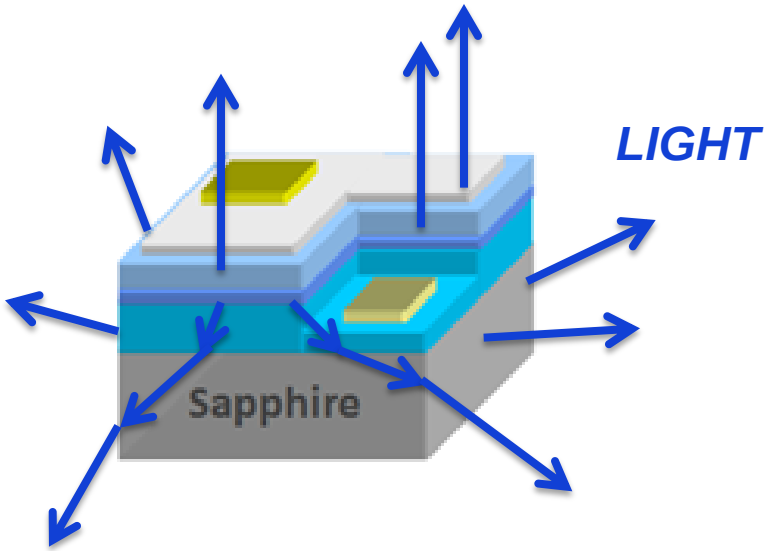
Lower LED operating temperature
Higher reliability

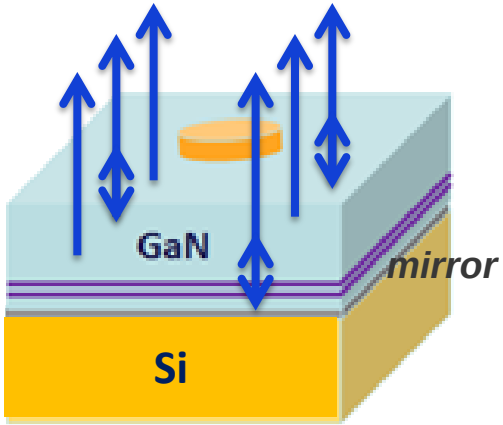
Higher driving current
More lm per die area

Simpler heat sink
Lower system cost

Focused light emitting surface - smaller Etendue

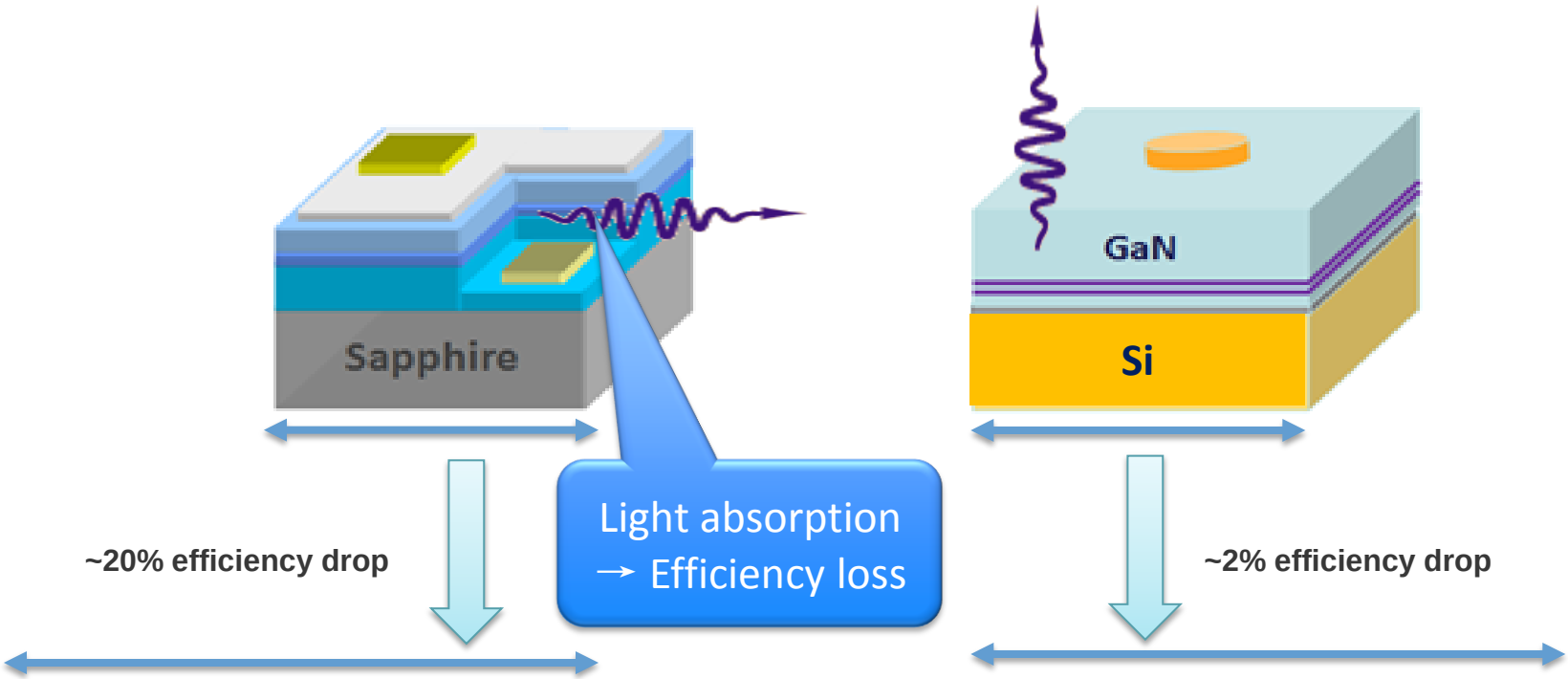
- Surface emitter V.S. volume emitter: How “spread out” the light is
- Simpler and lower cost optical system





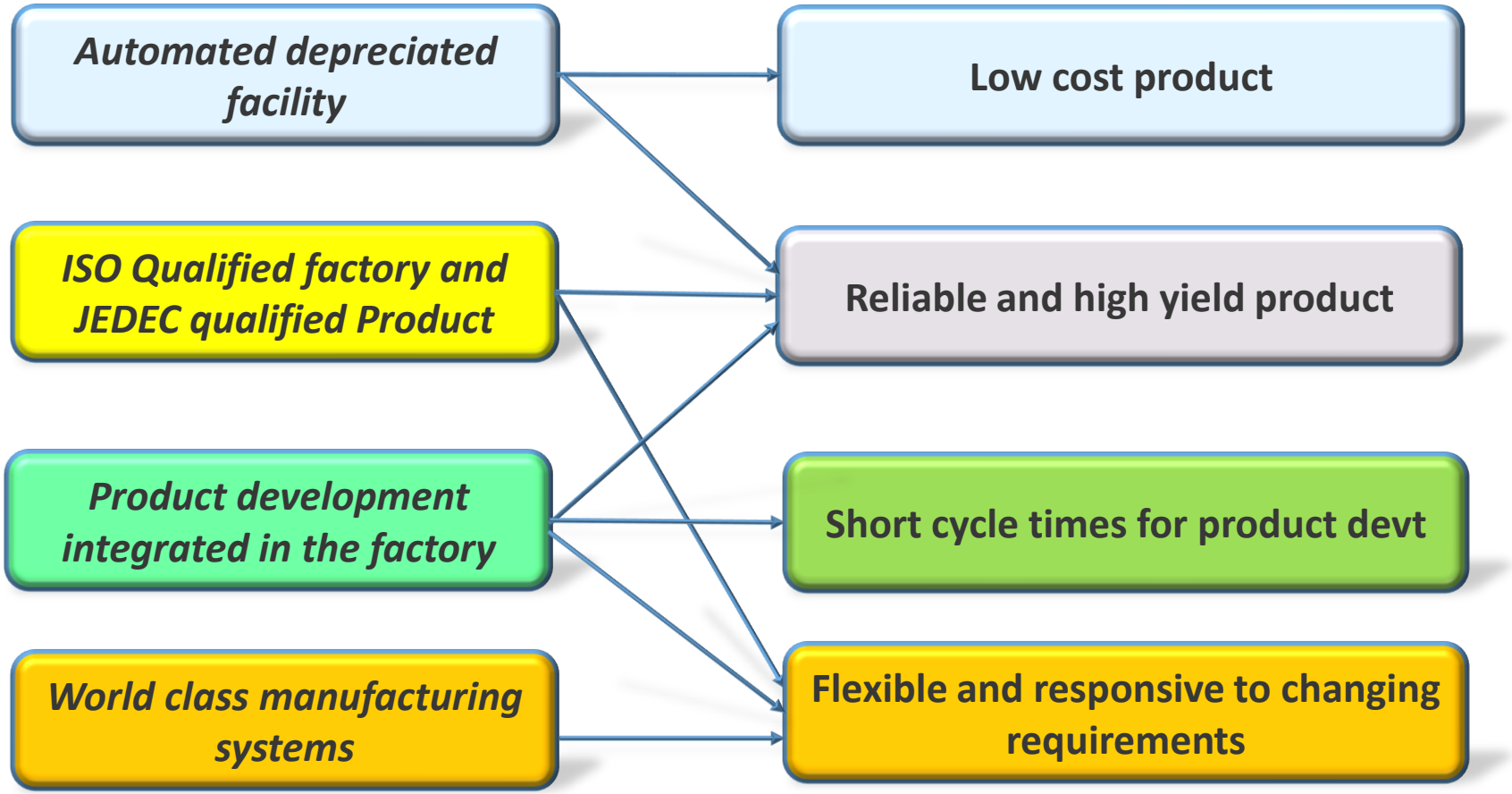
Less efficiency loss in big die

- Better lm/W maintenance when scaling up die size



Scaling up the chip size from 500um to 1500um

The Manufacturing Advantages



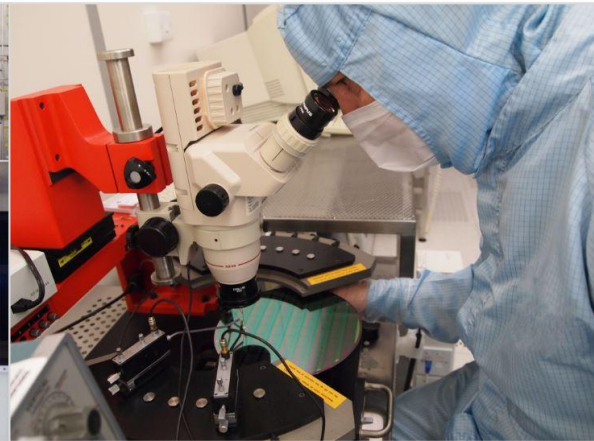
World-class Manufacturing Control System

World class IT Infrastructure enables maximum yield and minimal costs for LED manufacturing.

System integrates

- Real time MOCVD growth in situ measurements of temperature, wafer reflectance and curvature
- Post growth measurements of x-ray diffraction, photoluminescence and wafer bow
- In line defectivity data
- Wafer probe data

This allows manufacturing engineers to continuously optimise the process for optimum results.



Wafer-to-Package Assembly Line Flow

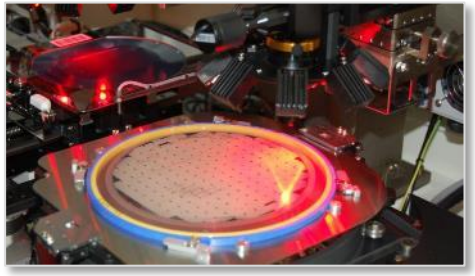
Assembly Wafer Preparation

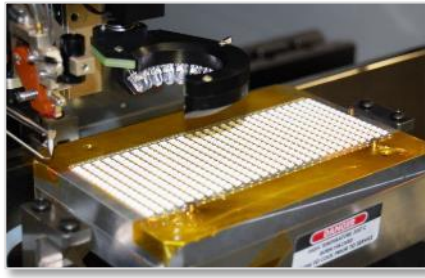
Wafer Probe → Wafer Tape Machine → Laser Scriber → Wafer Expander → Die Sorter

Die Assembly

Die Attach & Bonder → Curing Oven → Wire Bonder → Wire Bond Pull → Encapsulation → Singulation

Die Tester → Package sorter → Tape & Reel Packager





- Production process for probe, saw, sort and supply of die on membrane
- Facilitates Plessey to rapidly prototype and evaluate new chip designs
- Capability to produce engineering samples in 3535, 3020, 5630 package
- Capability to produce development samples of COB modules

Product Portfolio & Roadmap

MaGIC™ — Manufactured on GaN-On-Si I/C

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Technology Roadmap

To be added in the slide set but not published

Summary

MaGIC™ – Manufactured on GaN-On-Silicon

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Summary

- World's leading proprietary GaN-on-Si LED technology
- State-of-the-art in-house manufacturing capability from a European LED supplier
- Disruptive product portfolio addressing the massive and fast-growing SSL market
- Strong heritage and international brand recognition
- Blue-chip international partners
- R&D "engine room" for new technology