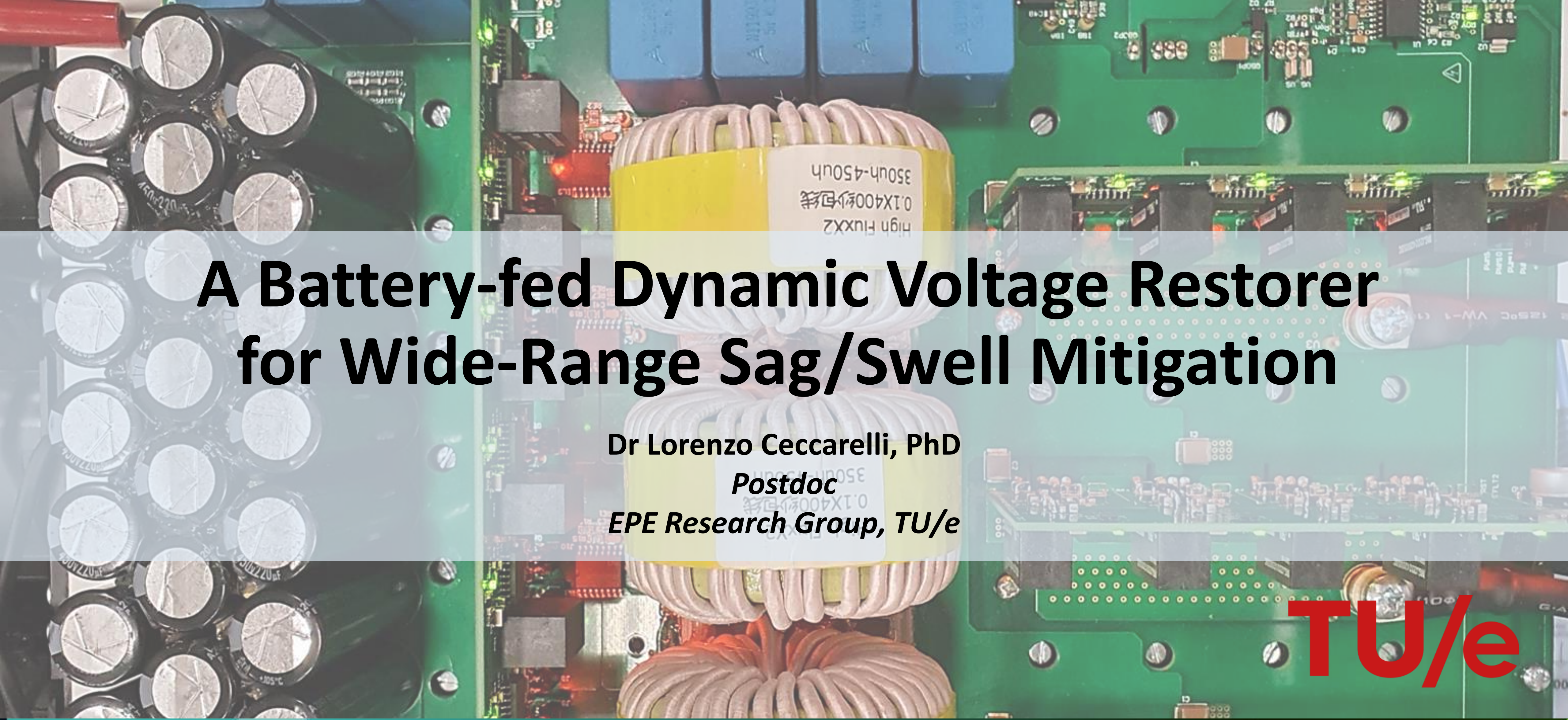

A Battery-fed Dynamic Voltage Restorer for Wide-Range Sag/Swell Mitigation

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EPE Research Group, TU/e

TU/e

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Outline

- **Introduction**
- Proposed DVR Layout
- Modeling and Simulation
- Experimental Setup
- Conclusion

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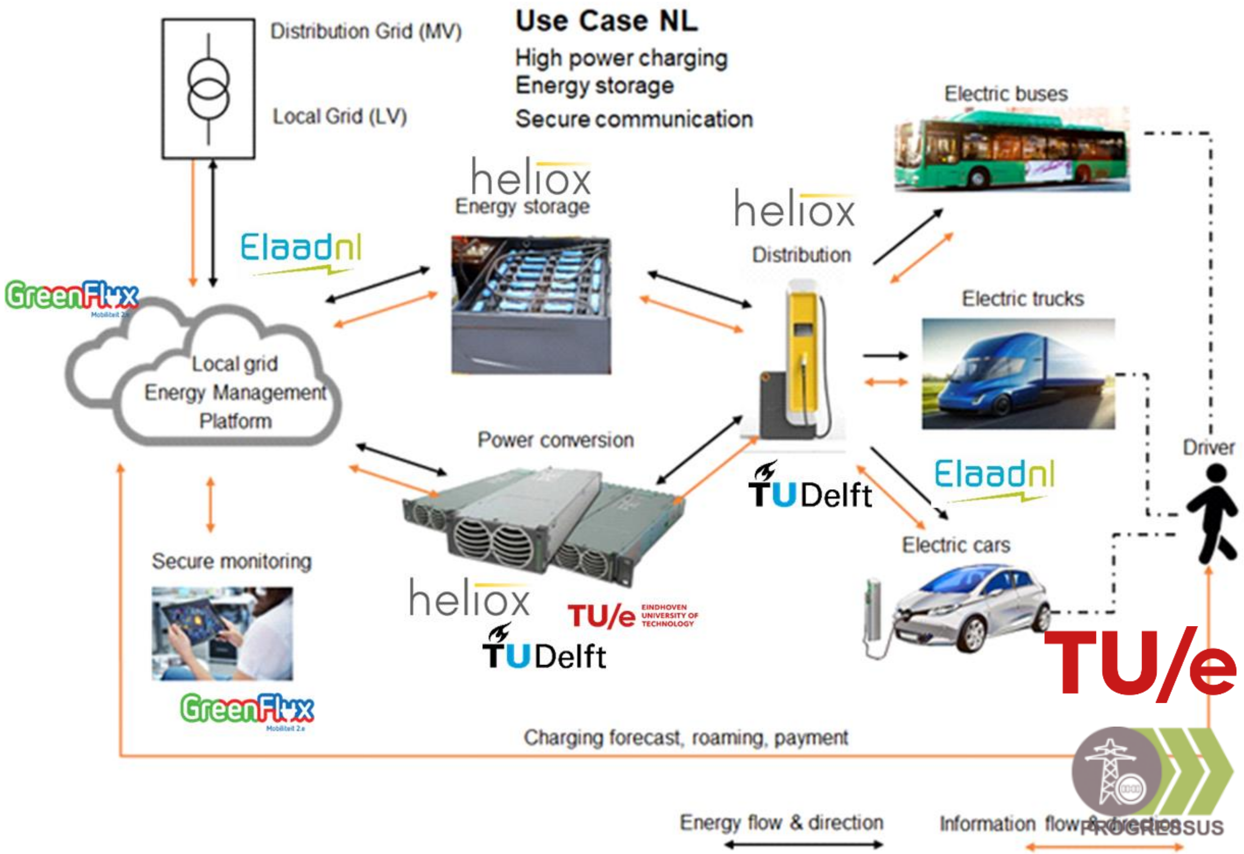
EV Charging Infrastructure

ECSEL PROGRESSUS
Use Case 2

- 65% reduction of peak power
- 20% lower cost
- 20% smaller volume
- 30% lower losses (WBG)
- Need for a protective interface with the grid (PQ)

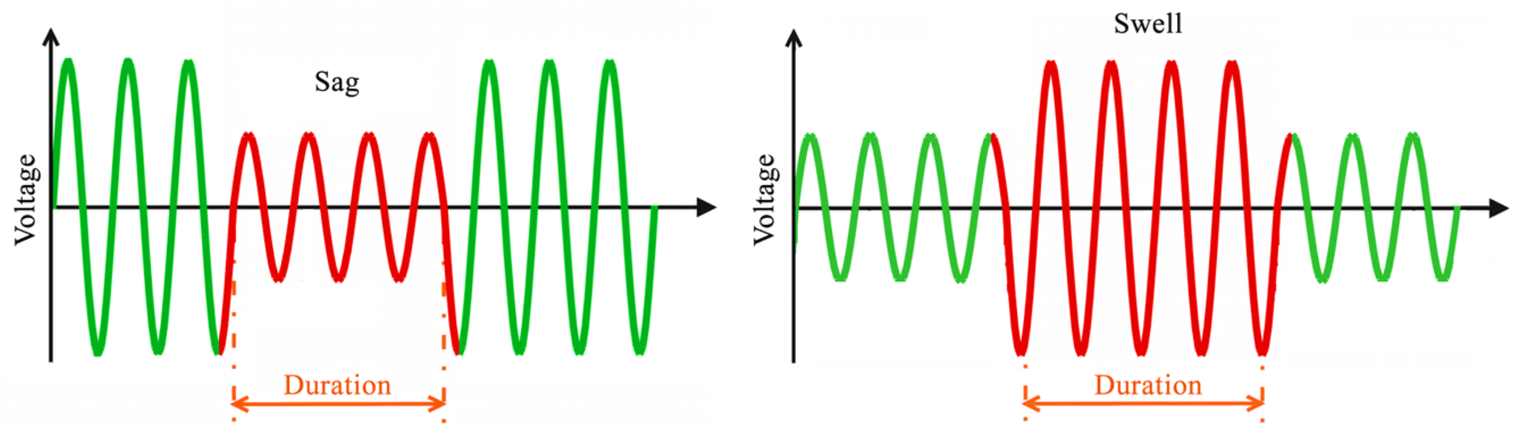


https://www.ecsel.eu/projects/progressus

Voltage Disturbances on the LV Grid

- Voltage *sags* and *swells* are among the most common **PQ** issues
- Mostly due to remote faults on the MV side
- Can cause **interruptions** and **malfunctioning**

Sags and Swells



Occurs when the rms voltage decreases between 10% and 90%
for a duration of a half-cycle to one minute.

Occurs when the rms voltage increases to over 110%
for a duration of a half-cycle to one minute.

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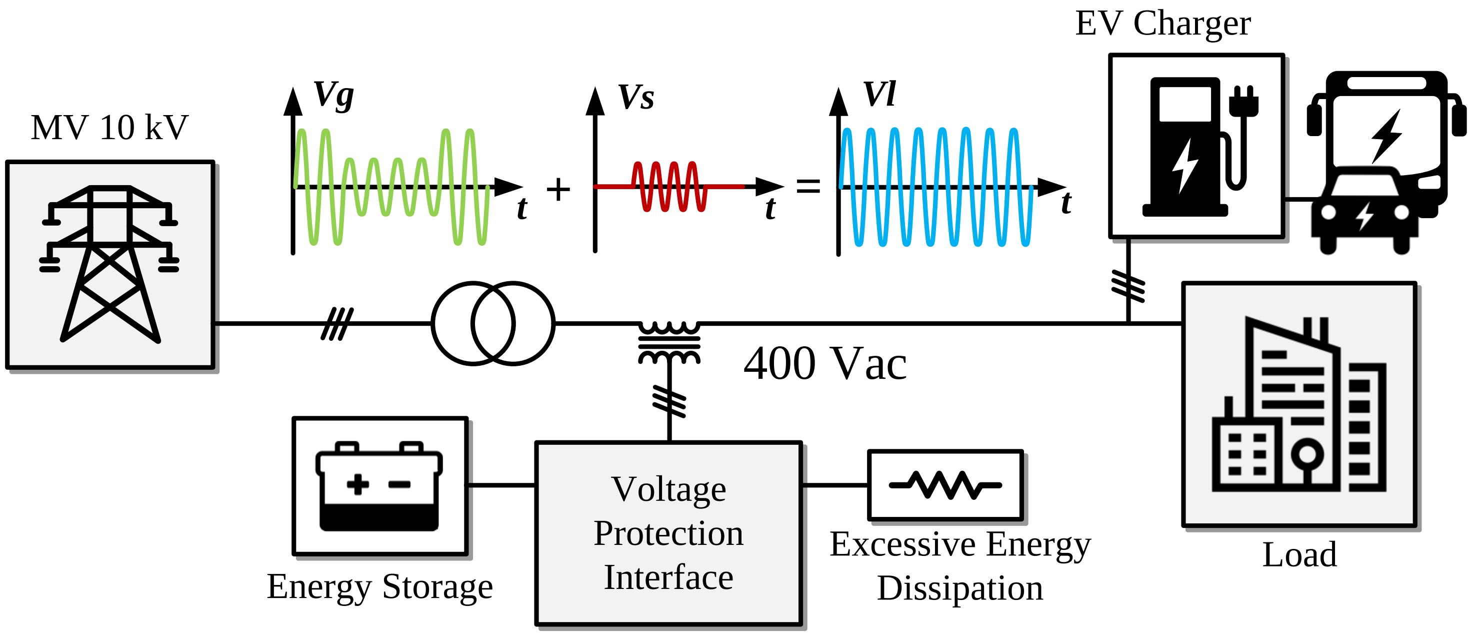
Dynamic Voltage Restorer (1/2)

- An established and cost-effective way to mitigate voltage disturbance on the load side
- **Dynamic voltage restorers** (DVRs) inject voltage in series with the source to compensate for voltage sags/swells

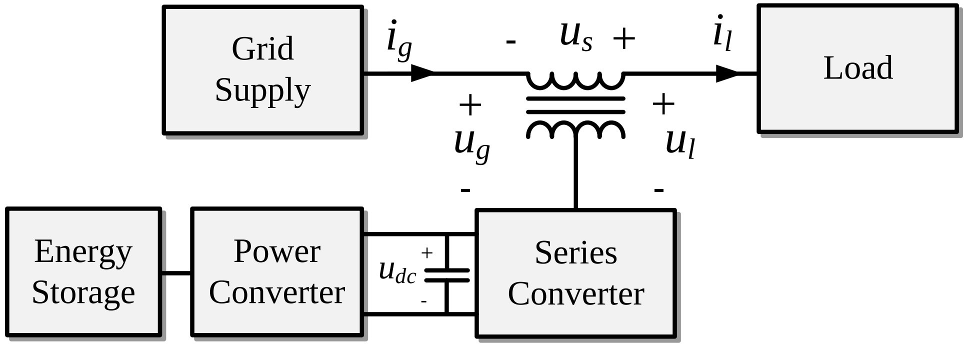


- Our requirement: **0.2 to 2 p.u.** for **5 ms to 60 s** (wide range)

Dynamic Voltage Restorer (2/2)

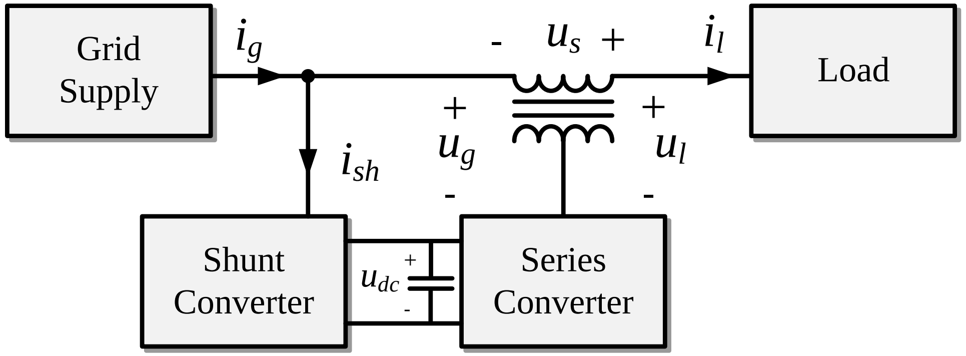
With energy storage

- Works independently from the grid ☺
- Wider compensation range/time ☺
- Mainly active power
- Relatively expensive ☹



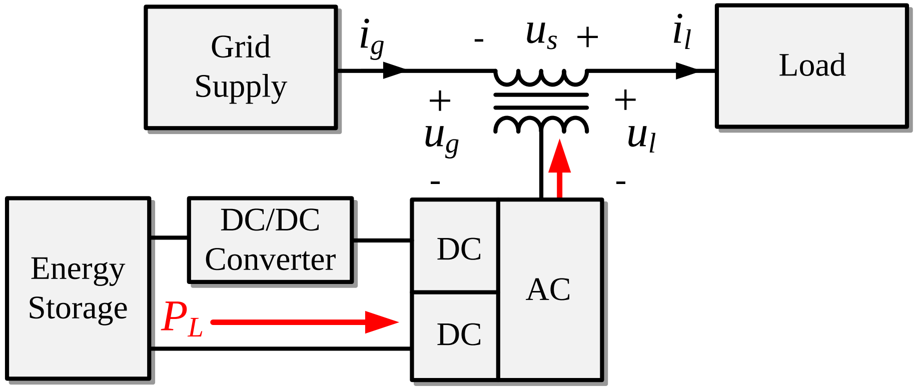
Without energy storage

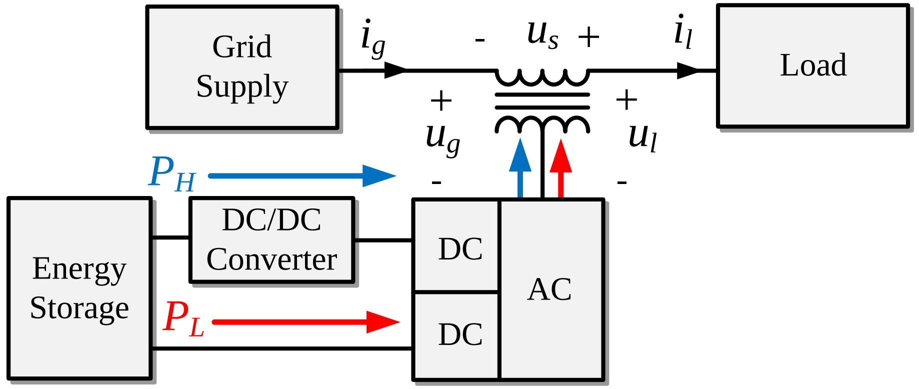
- Taps energy from the grid
- Lower compensation range/time ☹
- Mainly reactive power
- Relatively cheap ☺

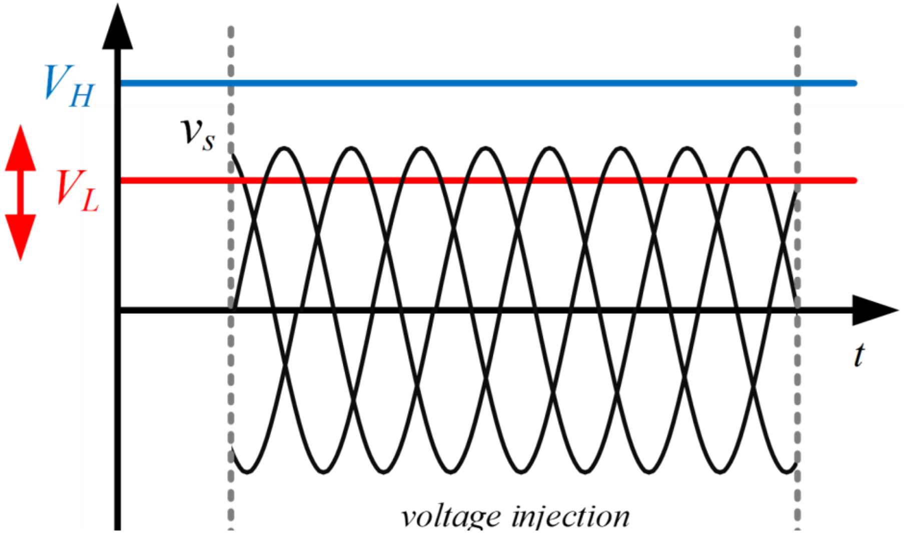


J. G. Nielsen and F. Blaabjerg, "A detailed comparison of system topologies for dynamic voltage restorers," IEEE Transactions on Industry Applications, vol. 41, no. 5, pp. 1272–1280, Sep. 2005.

Dynamic Voltage Restorer (2/2)







- Can tap power directly from the battery (2L) ☺
- Reduced power rating of dc-stage ☺
- Power consumption in standby mode ☹
- Efficiency can be further improved

J. Wang, Y. Xing, H. Wu, and T. Yang, “A Novel Dual-DC-Port Dynamic Voltage Restorer With Reduced-Rating Integrated DC–DC Converter for Wide-Range Voltage Sag Compensation,” IEEE Trans. Power Electron., vol. 34, no. 8, pp. 7437–7449, Aug. 2019.

Possible DVR Improvements

- Main drawback: power consumption in idle mode (series-connected converter)
- Efficient design with wide-bandgap power switches
- Further improve DC-stage design
- Power density (relevant to our case study)
- Multi-functional PQ converter

➢ **Computer-aided design workflow based on modeling and simulation**

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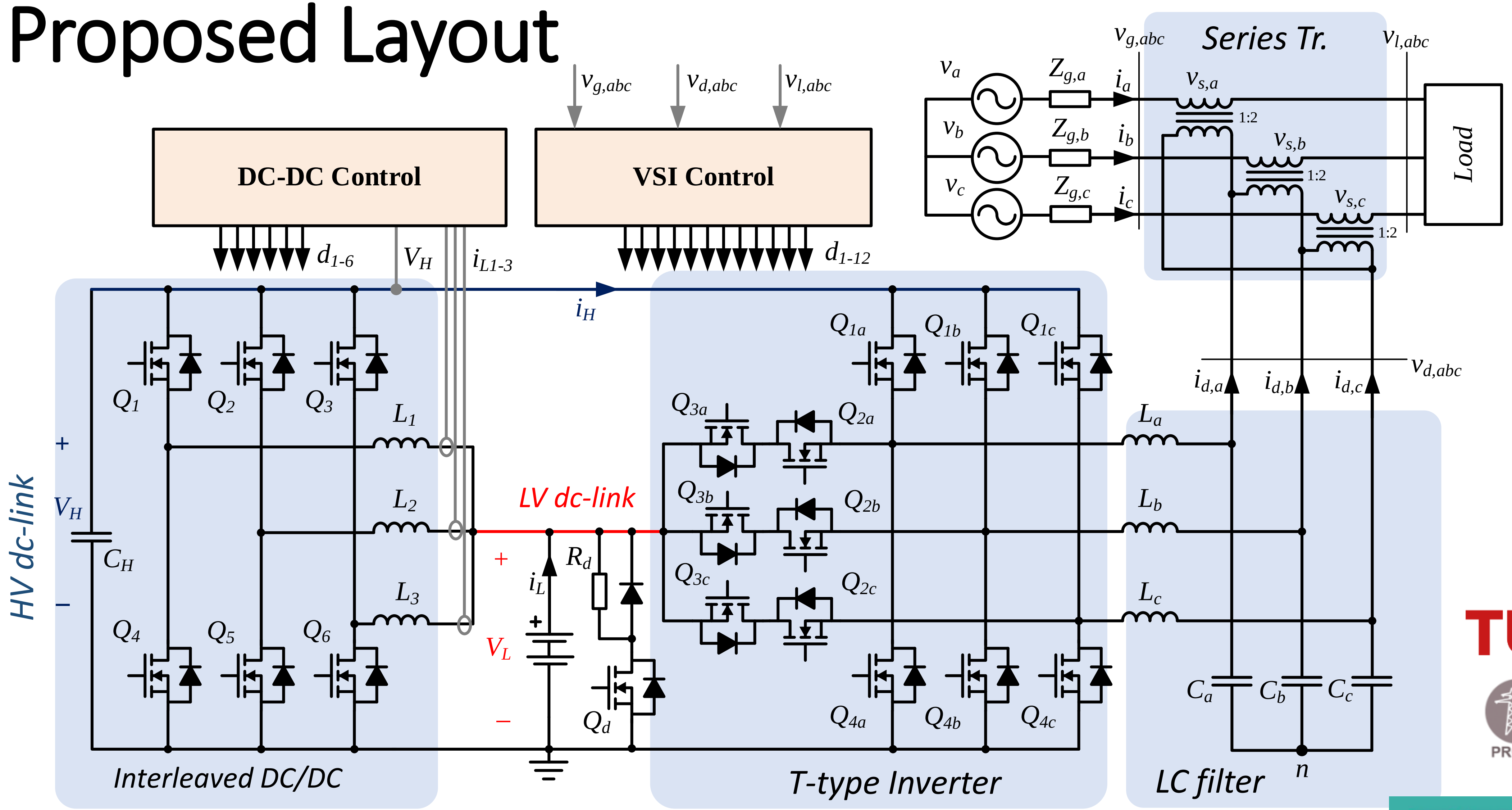
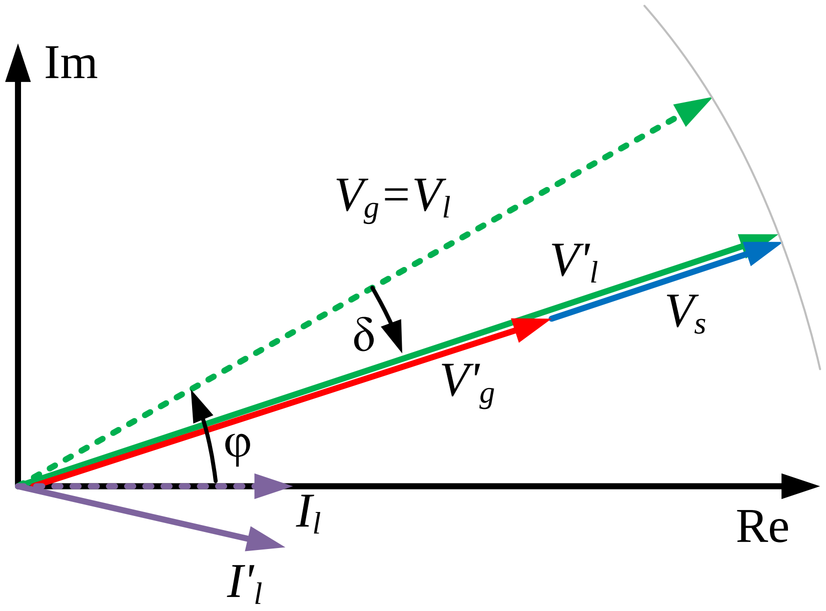
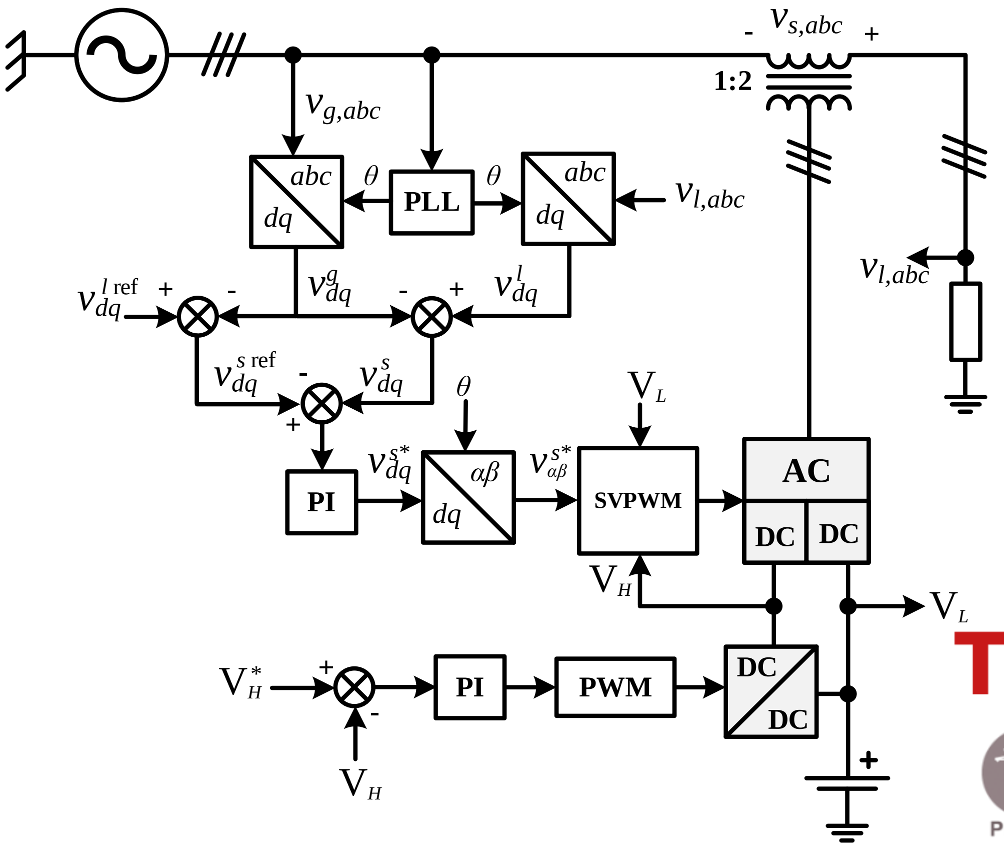
Proposed Layout



Control Technique (1/2)

- *In-phase* compensation technique





- Minimized injected voltage amplitude
- Phase jump is not compensated

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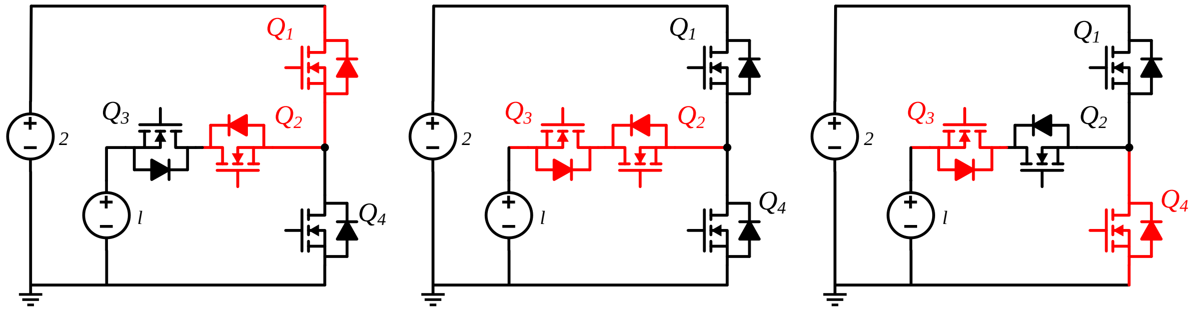
Control Technique (2/2)

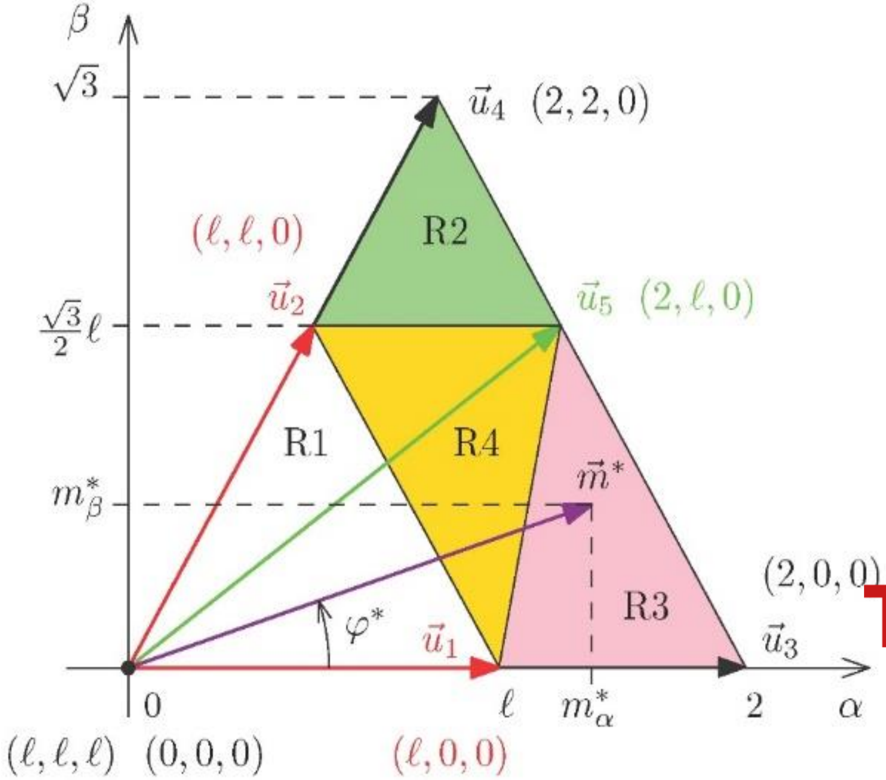
- Asymmetrical SVPWM

$0 \leq l \leq 2$

$$S_{Qi} = \begin{cases} 2 \; (Q_{1i}, Q_{2i}, Q_{3i}, Q_{4i}) = (1,1,0,0) \\ l \; \; (Q_{1i}, Q_{2i}, Q_{3i}, Q_{4i}) = (0,1,1,0) \\ 0 \; (Q_{1i}, Q_{2i}, Q_{3i}, Q_{4i}) = (0,0,1,1) \end{cases}$$



$$\vec{m}^* = (1 - d_1 - d_2) \; \vec{e}_0 + d_1\vec{e}_1 + d_2\vec{e}_2$$



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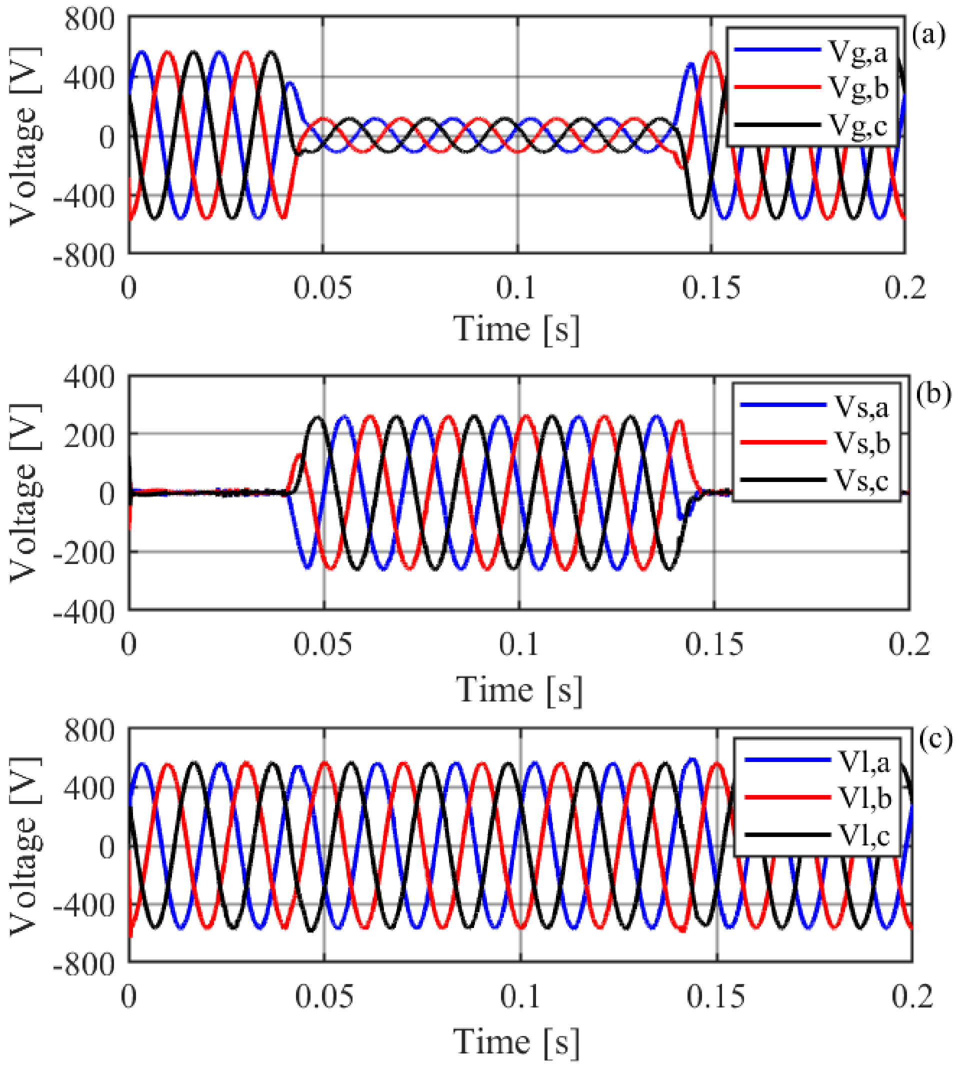
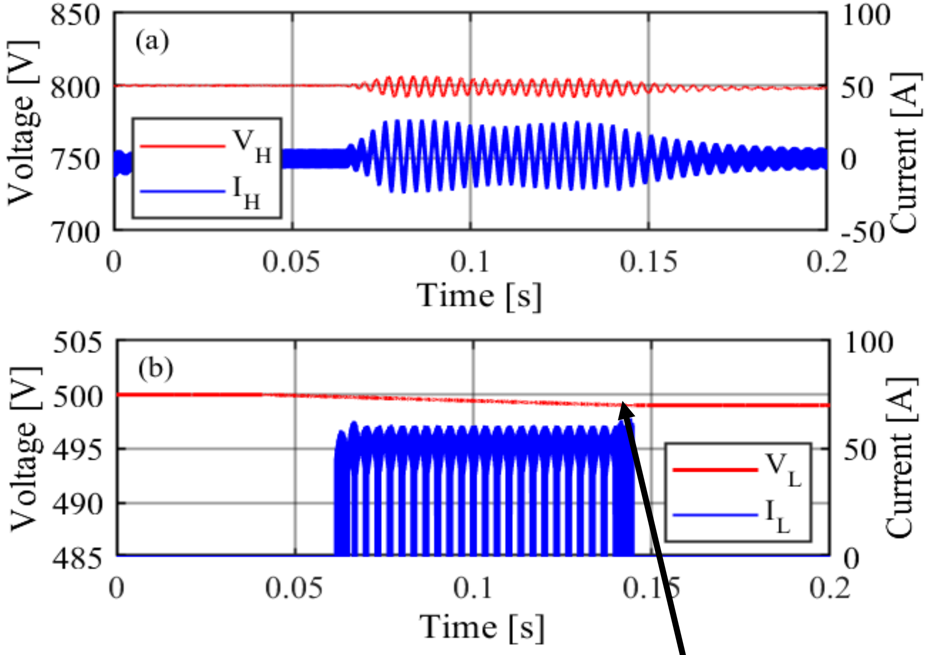
Voltage Sag Simulation – 0.2 p.u. / VL= 500 V

Grid Voltage

DVR Voltage

Load Voltage





HV dc-port

LV dc-port

battery discharging

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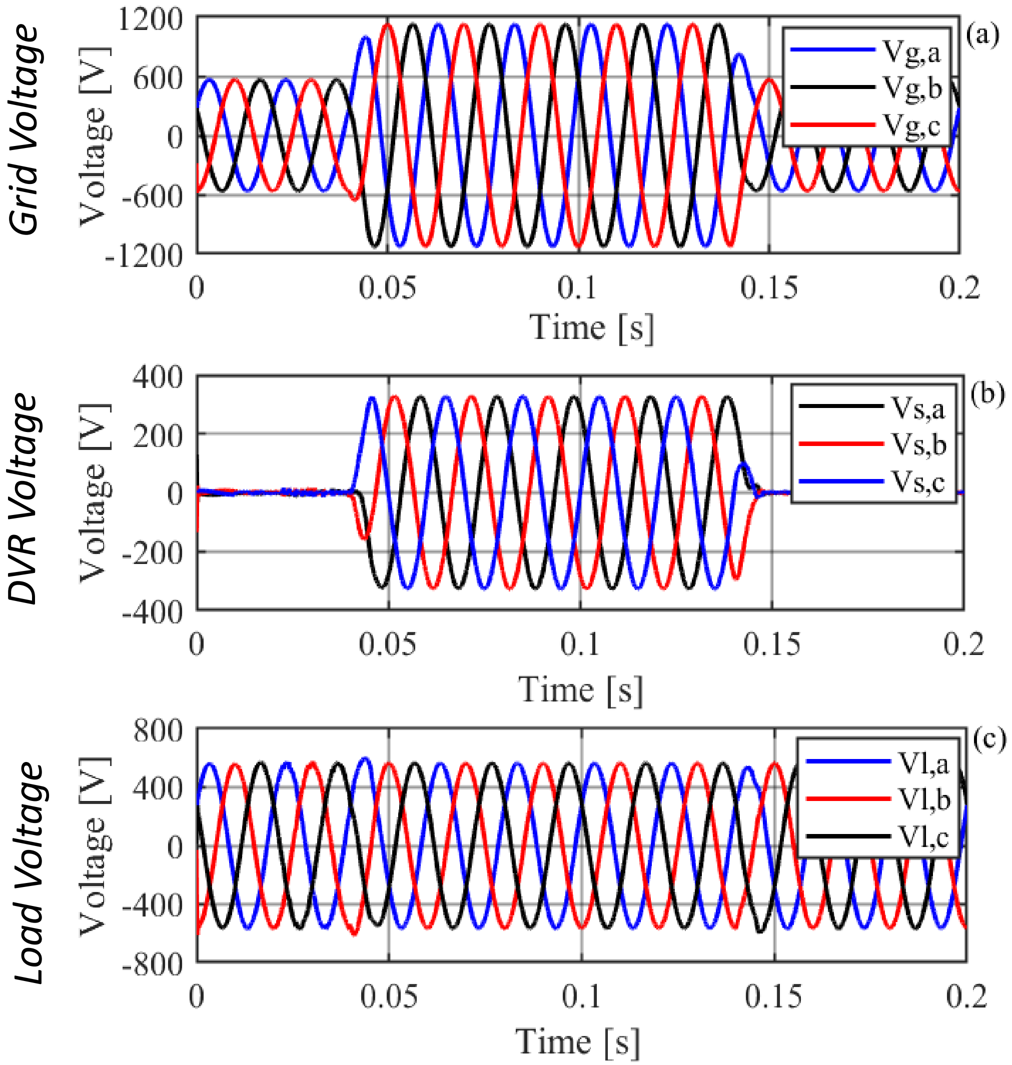
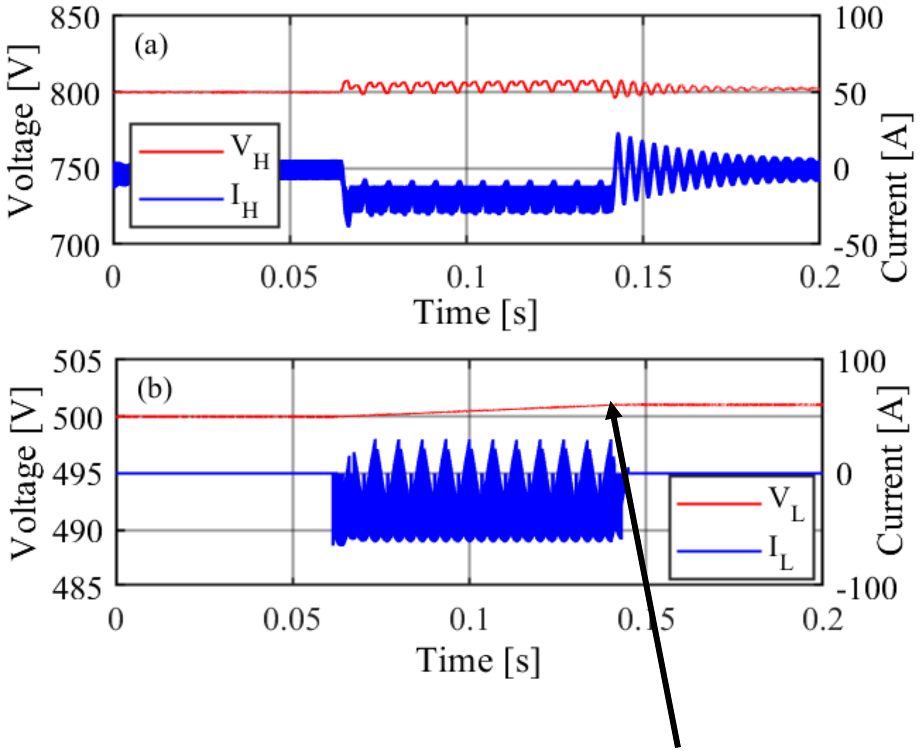
Voltage Swell Simulation – 2 p.u. / VL= 500 V





HV dc-port

LV dc-port

battery charging

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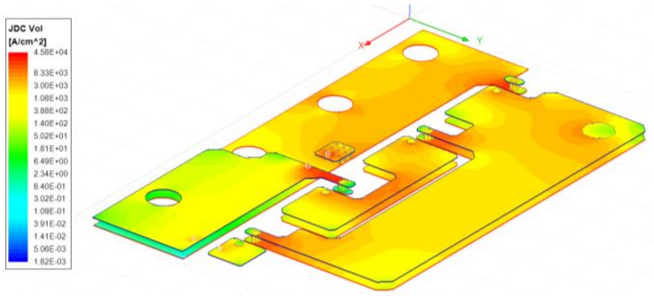
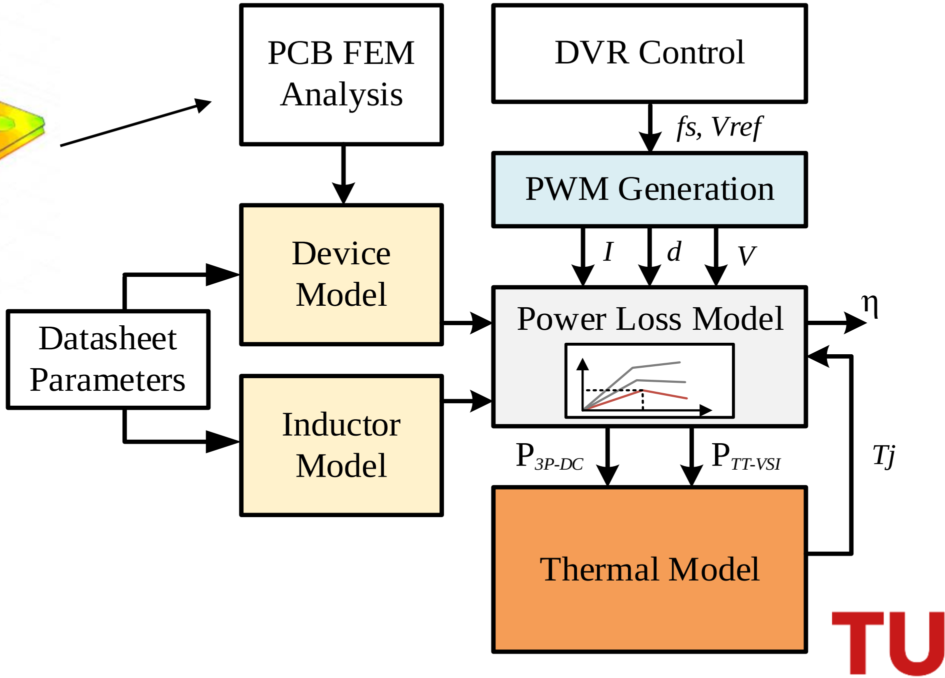
Power Loss Modeling





PCB FEM Analysis

DVR Control

fs, Vref

PWM Generation

I *d* *V*

Datasheet Parameters

Device Model

Inductor Model

Power Loss Model

η

$P_{3P\text{-}DC}$ $P_{TT\text{-}VSI}$

Tj

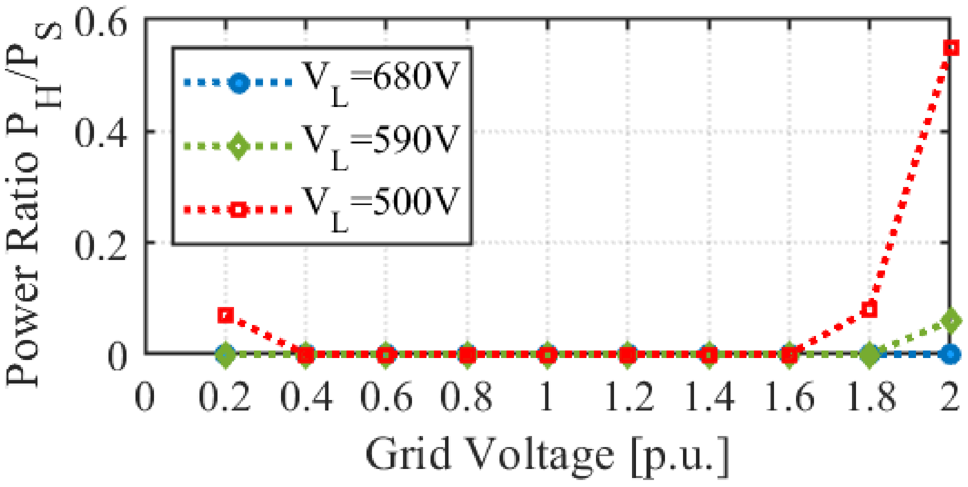
Thermal Model

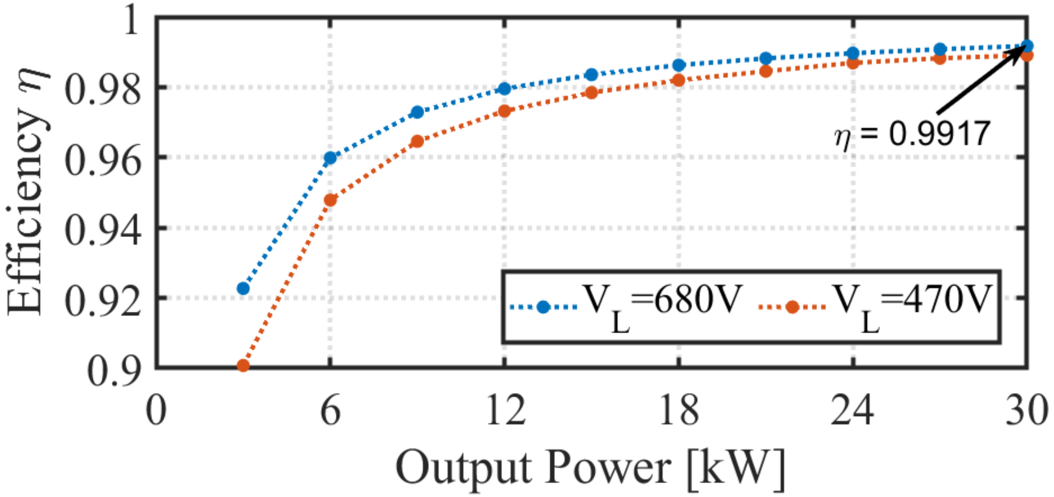
- Power loss model of switch and inductor
- PCB parasitics extracted via FEM simulation
- Thermal model obtained by heatsink geometry

Simulation Results

- DC stage only operates when >60% power is required at low battery charge
- 45% lower power rating for DC stage

- Simulated peak efficiency at 99.17% (semiconductor + inductor losses)
- Efficiency drops as battery charge reduces





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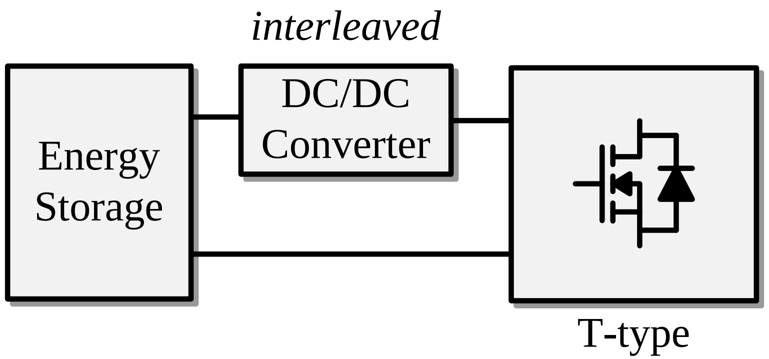
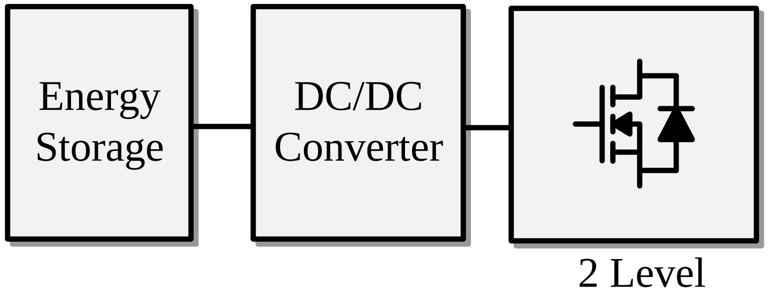
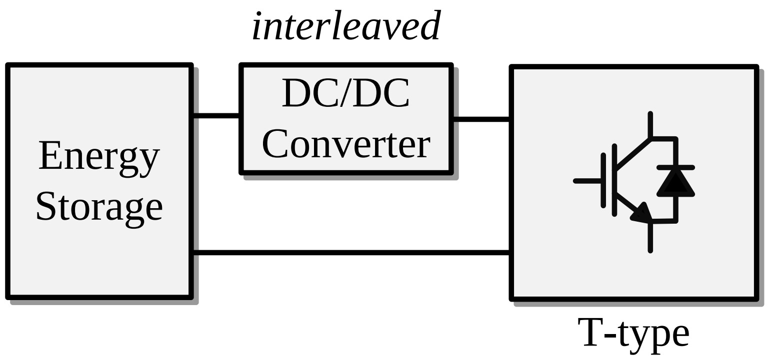
Comparative Analysis

Proposed Layout (SiC MOSFETs)

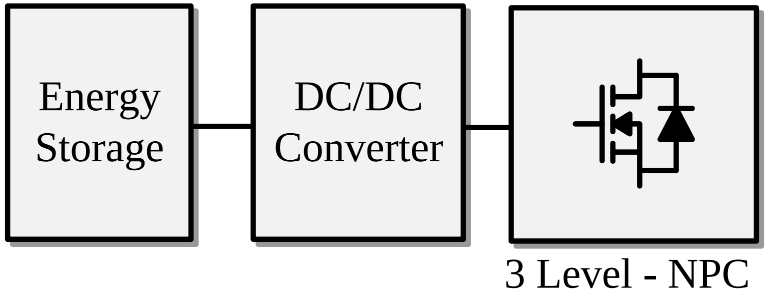


DC/DC + 2 level (SiC MOSFETs)





Proposed Layout (Si IGBT)



DC/DC + 3 level (SiC MOSFETs)

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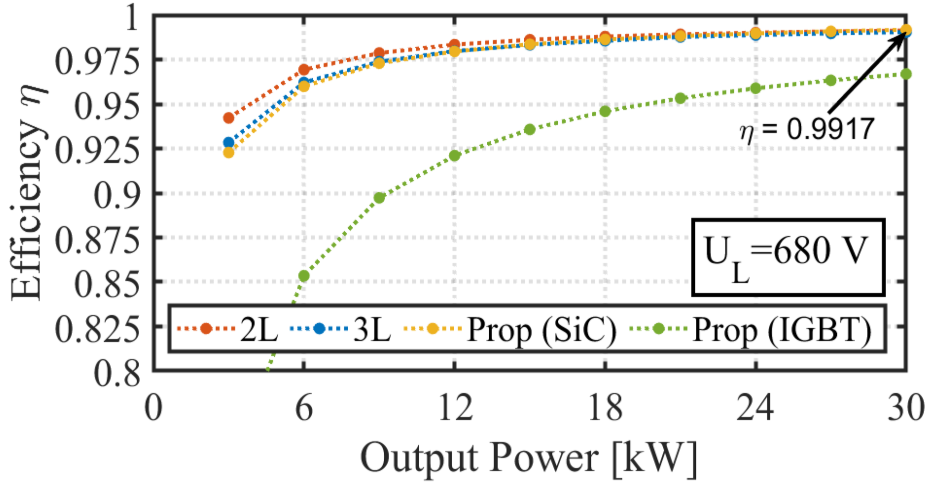
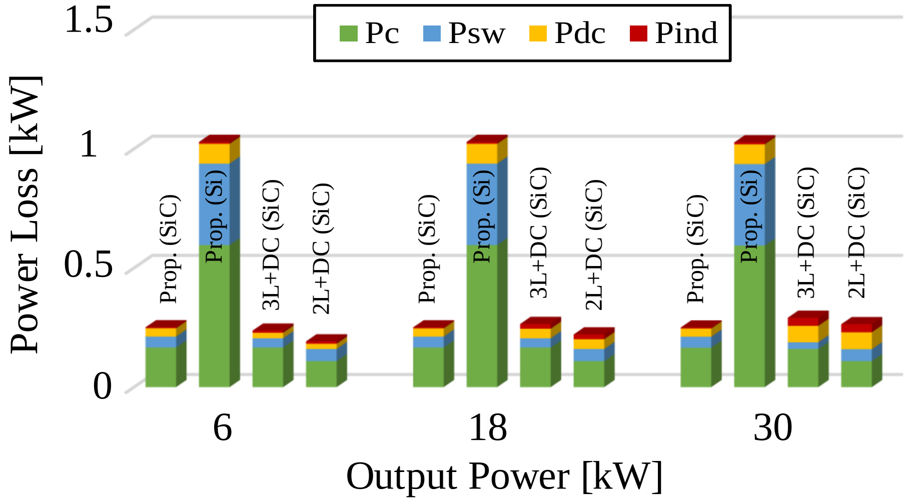
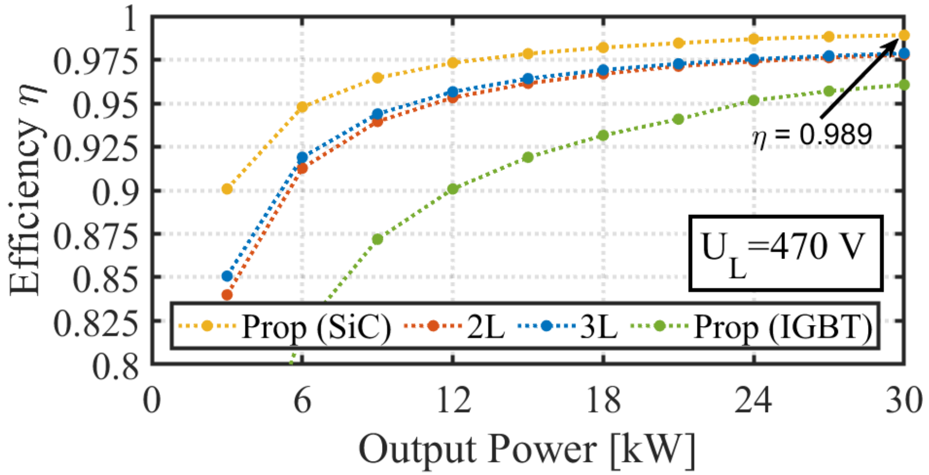
Comparative Analysis - U_L=680V

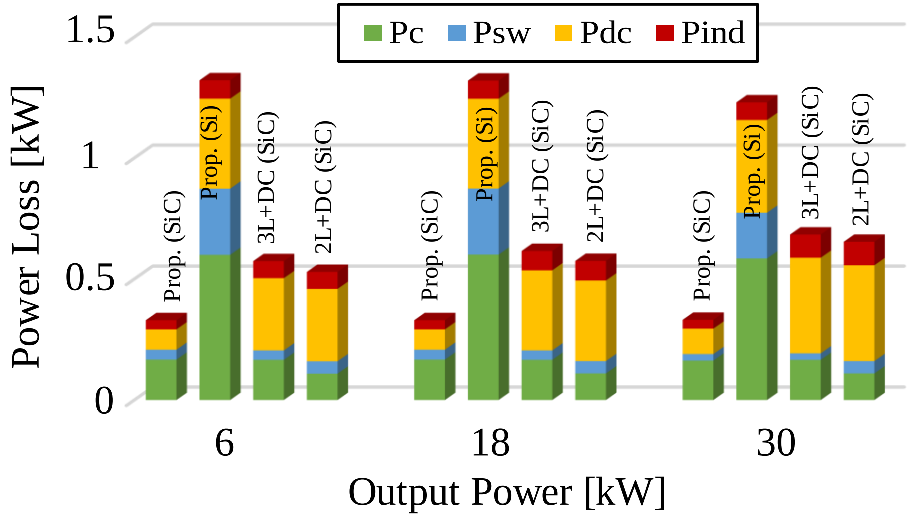




- No significant difference between SiC topologies
- IGBT shows worse performance
- DC-stage losses are minimum

Comparative Analysis - U_L=470V





- Proposed topology has better performance if battery SOC is lower
- DC-stage losses are higher in all the other designs
- Interleaved dc-stage performs better

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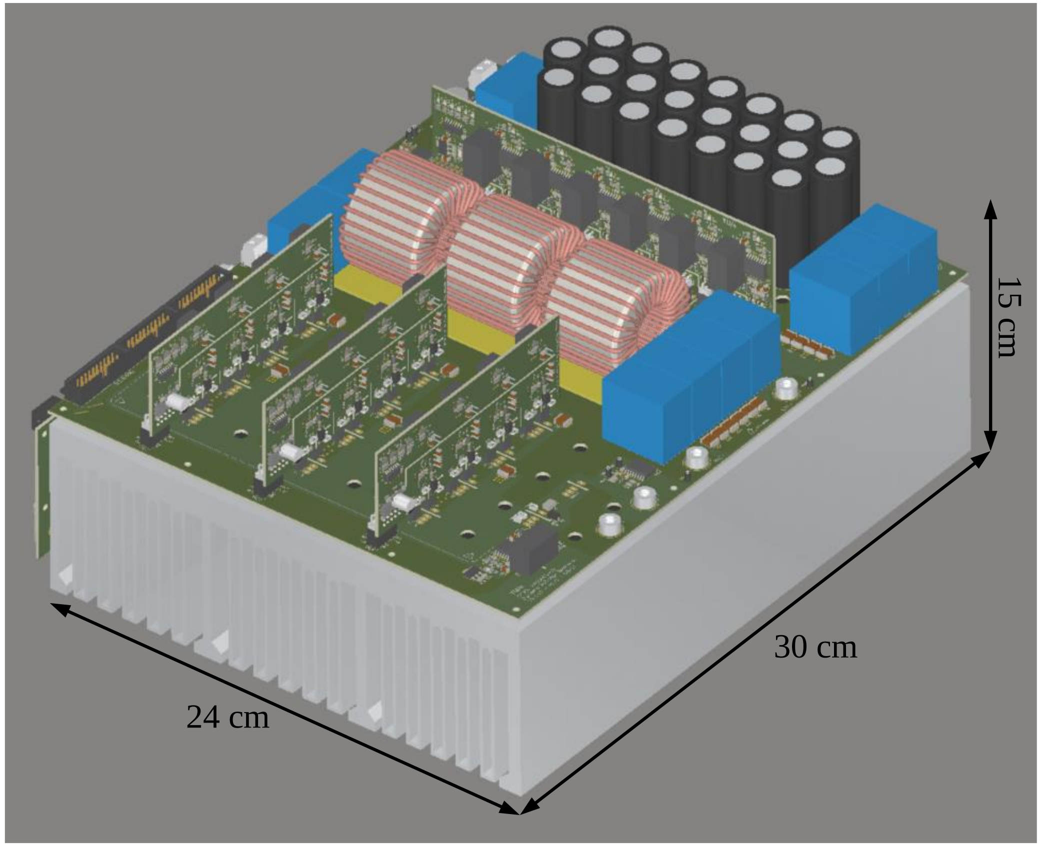
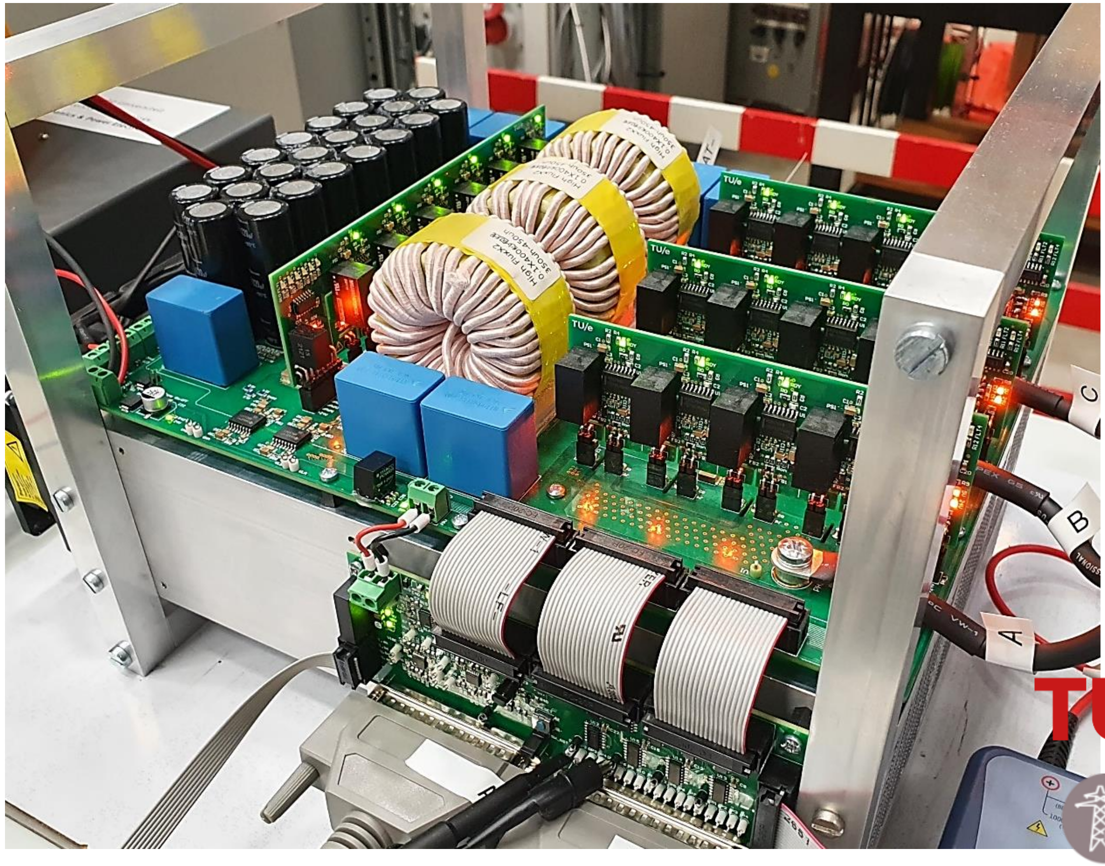
30 kVA DVR Prototype





- Power density ~3.3 kW/dm^3

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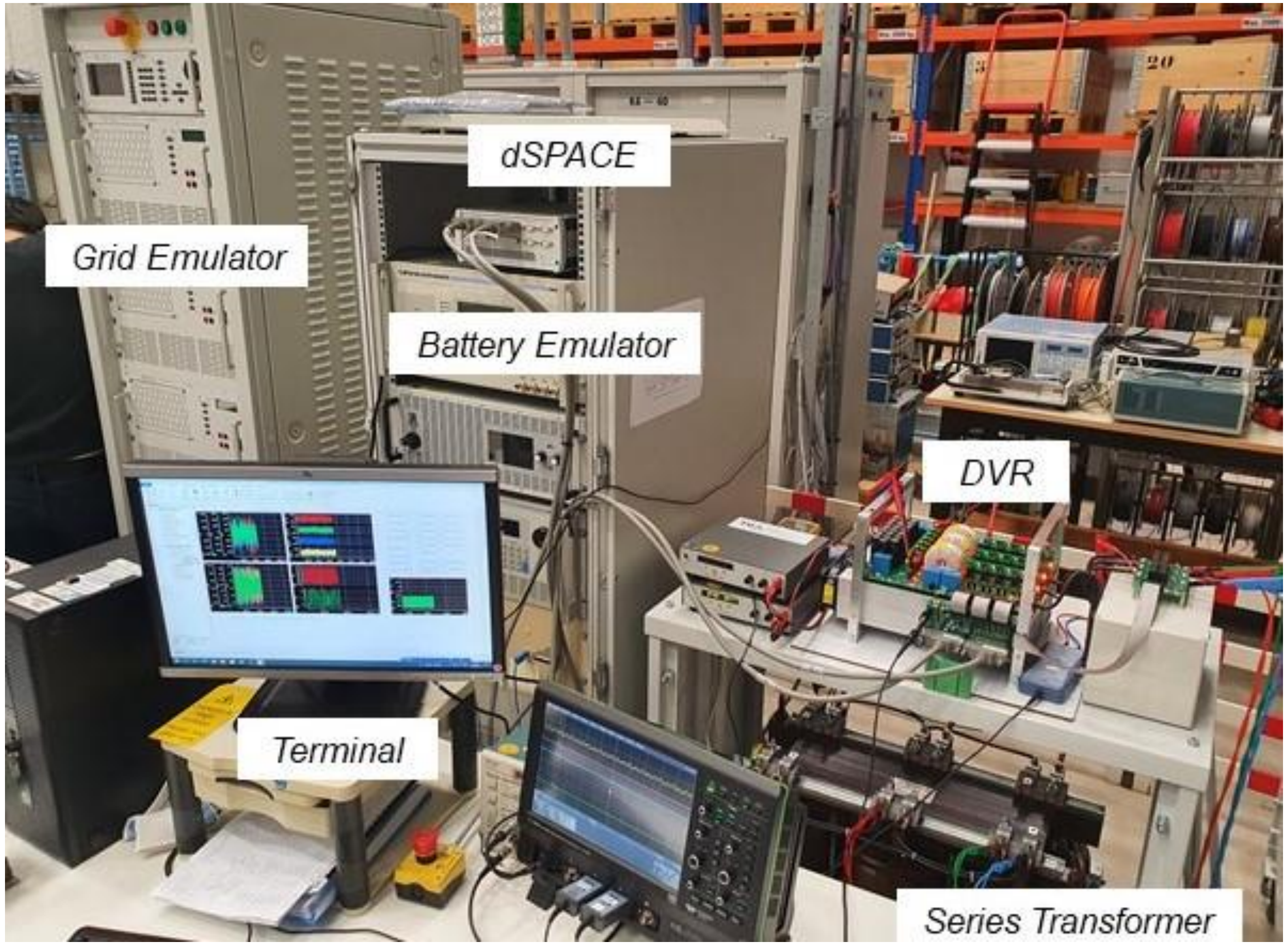
Test Setup

- 15 kVA grid emulator
- 30 kVA series transformer
- 30 kW DC source / battery emulator
- dSPACE control interface



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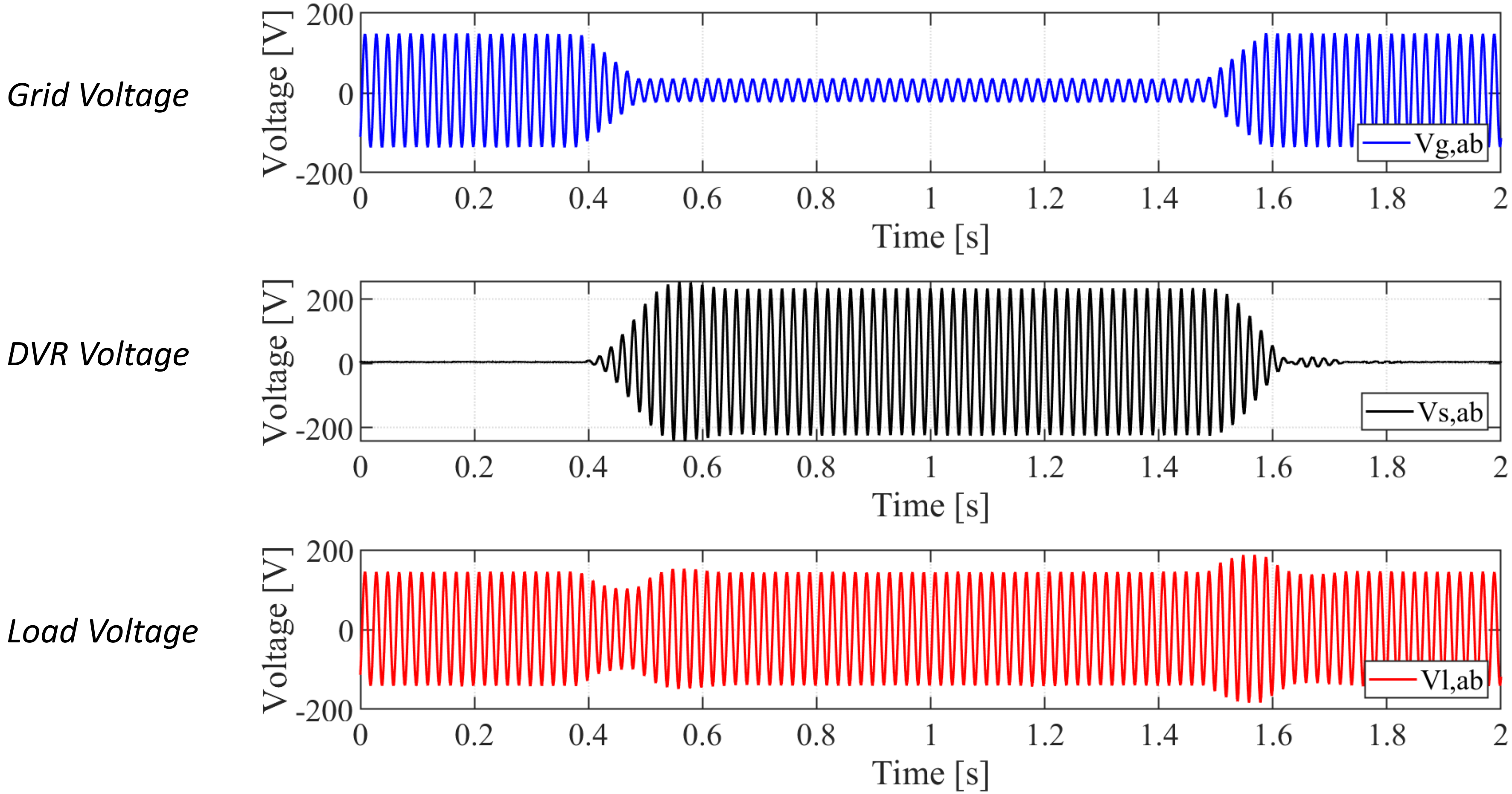
Experimental Results (1/3)

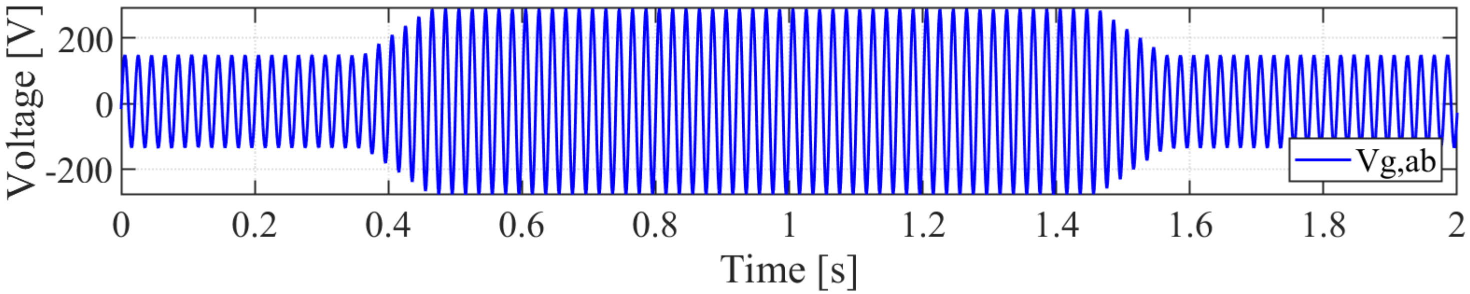
Voltage Sag – 0.2 p.u. / VH= 300 V



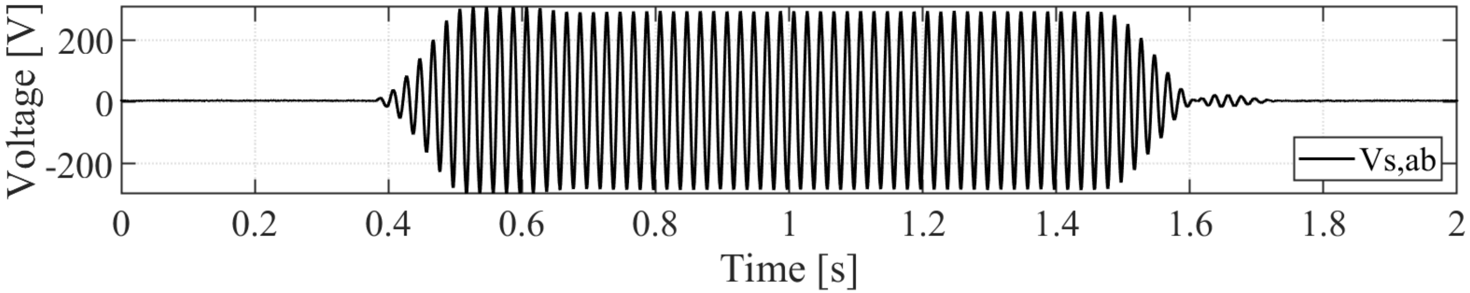
Experimental Results (2/3)

Voltage Swells – 2 p.u. / VH= 300 V

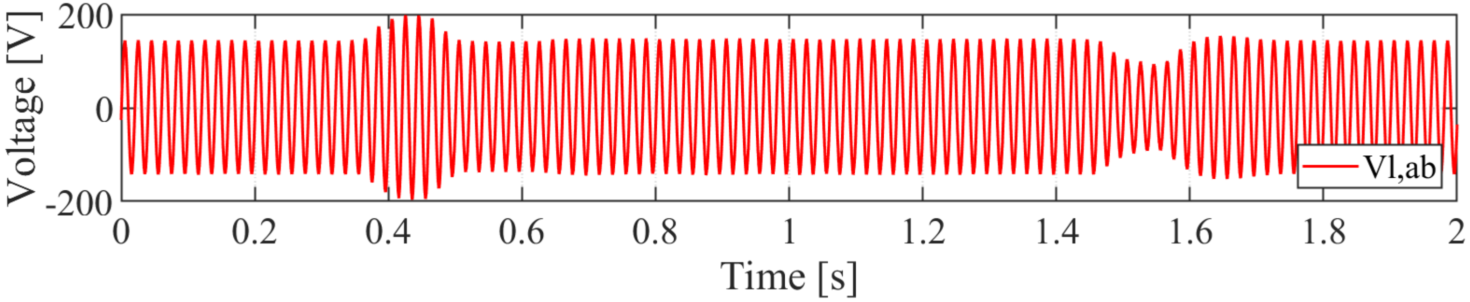
Grid Voltage



DVR Voltage



Load Voltage



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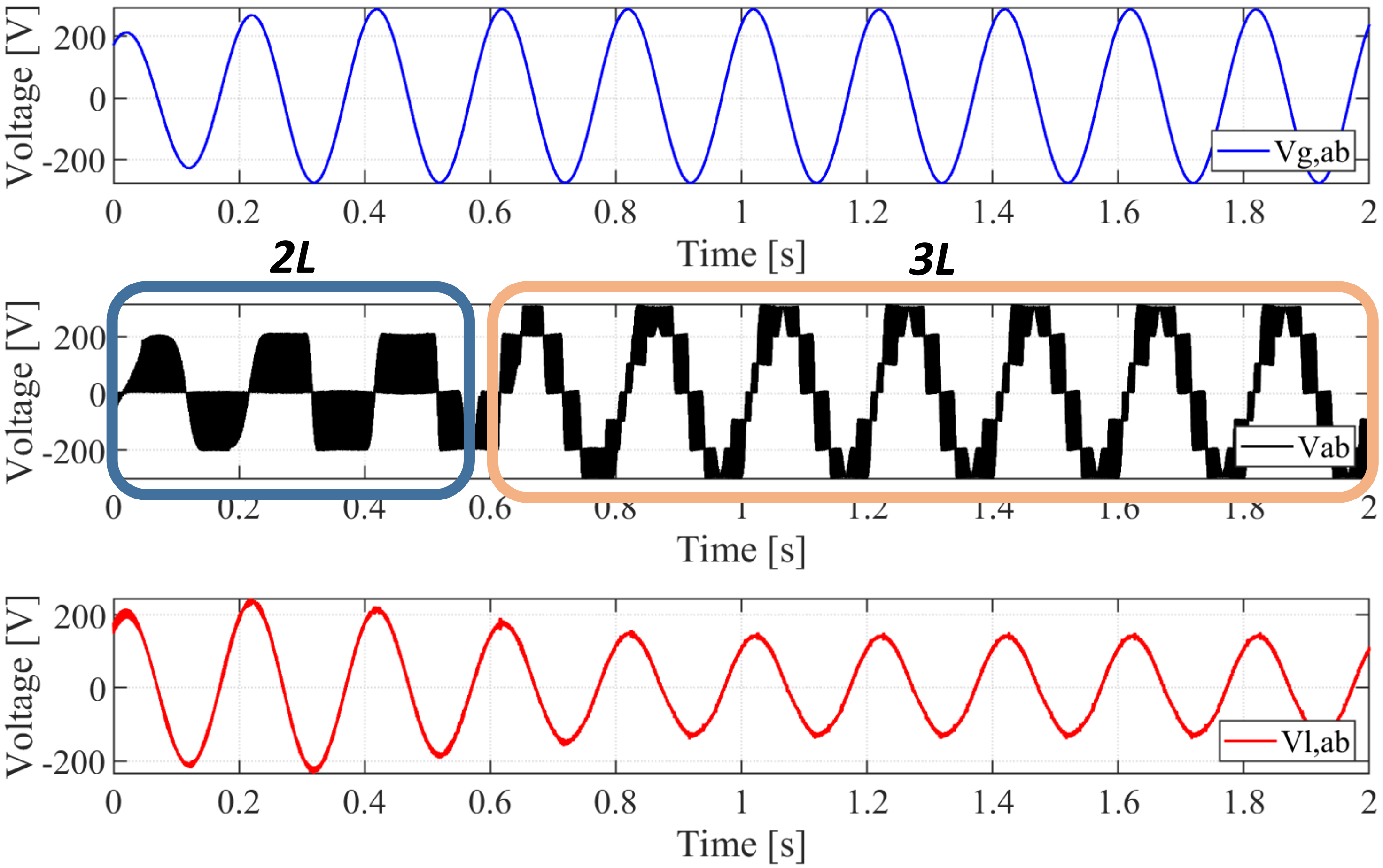
Experimental Results (3/3)

Voltage Swells – 2 p.u. / VH= 300 V

Grid Voltage

DVR Voltage

Load Voltage



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Conclusion

- Concept and implementation of an all-SiC DVR for wide-range sag/ swell compensation
- Improved layout
- Simulation-driven design procedure
- Simulation and early test results shows promising performance

Future Work

- Full validation of converter performance
- Additional PQ features (harmonic mitigation)

Thank you for your attention!

Questions?

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Postdoc

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