# Schakelen van 650V GaN halfgeleiders op ultra-hoge schakel frequenties

Bart Bokmans

# Introduction

- PhD candidate in EPE group
- Started in January 2020
- Focus on Gallium Nitride (GaN) based power converters
- Towards multi-MHz switching frequencies

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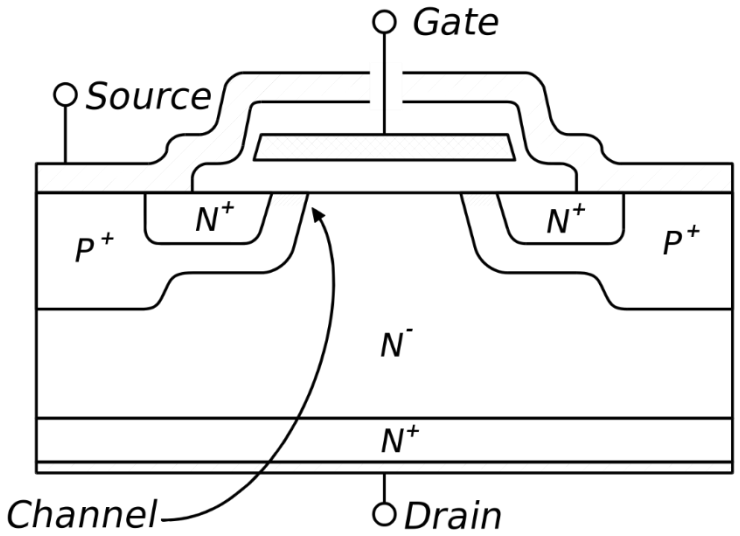
# Agenda

- Advantages of Gallium Nitride (GaN) semiconductors
- Design considerations
- TU/e prototype



# Power Semiconductors

- Power MOSFET available since the 1960s




- Multi-billion market with expected CAGR of 5% till 2030

- Modern wide-bandgap semiconductors

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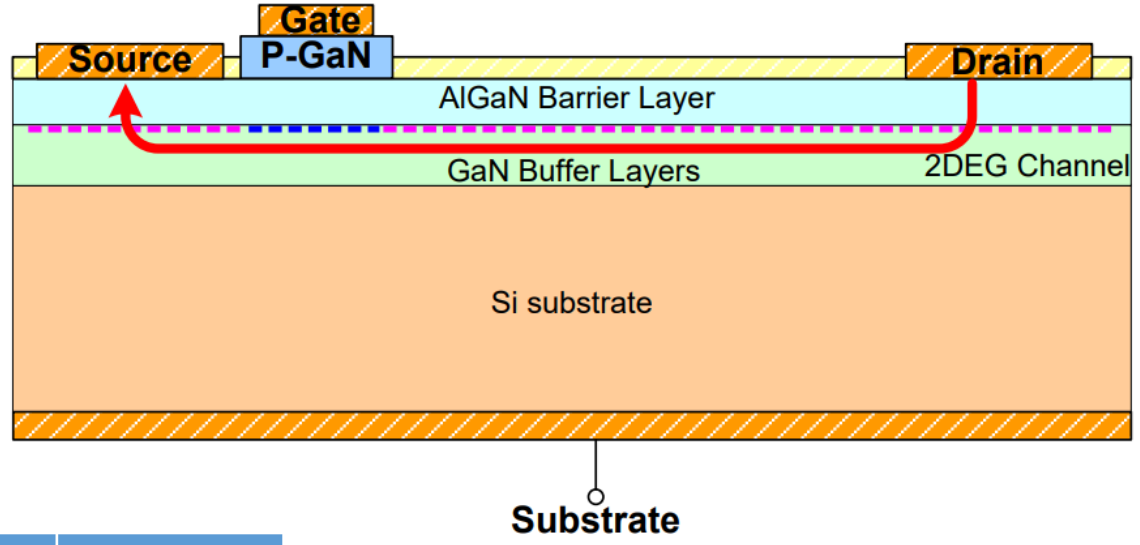
# GaN Semiconductors

- Normally-off HEMT

High Electron-Mobility Transistor



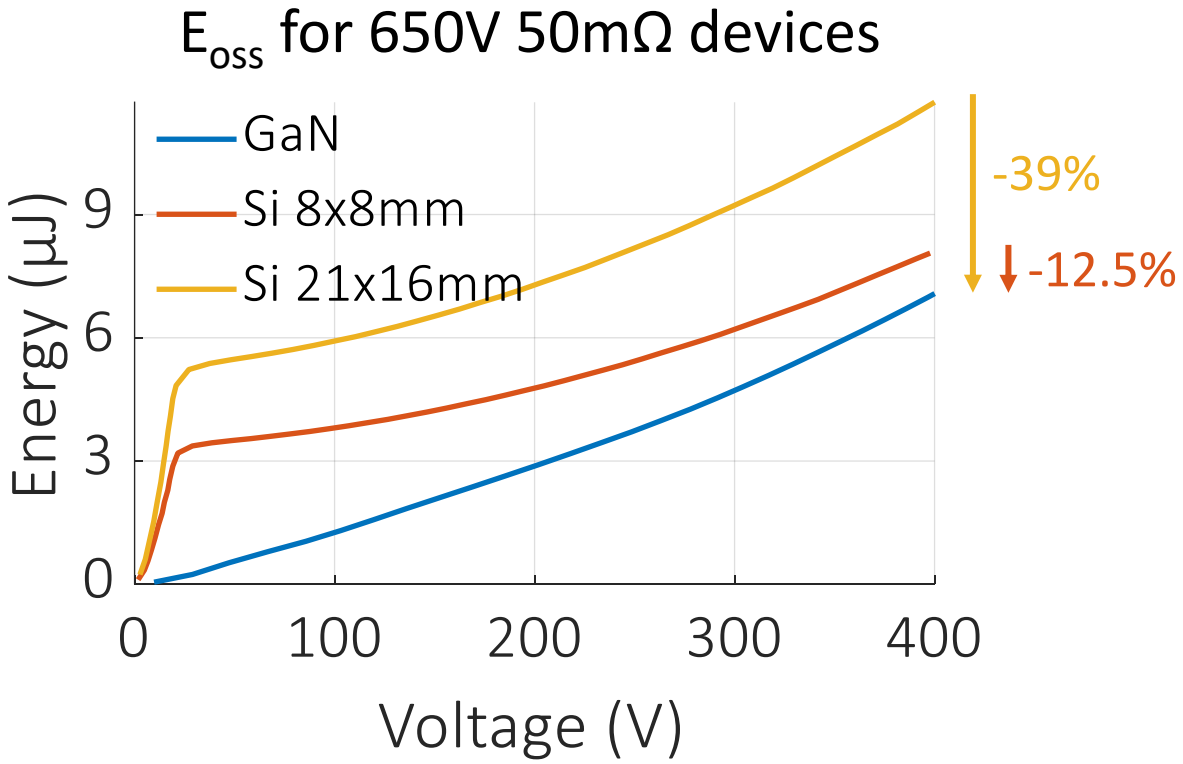

- Material properties

| Material | Si | GaN | SiC-4H |
|---|---|---|---|
| Bandgap Energy (eV) | 1,1 | 3,4 | 3,3 |
| Breakdown Field (V/µm) | 25 | 400 | 300 |
| Electron Mobility ($cm^2/V{\cdot}s$) | 1350 | 1300 | 800 |
| Thermal Conductivity (W/cm·K) | 1,5 | 1,3 | 4,9 |

*Roccaforte, F et al. An Overview of Normally-Off GaN-Based High Electron Mobility Transistors*

# GaN Semiconductors

- Electrical Performance




7 x 4,5 mm


8 x 8 mm


21 x 16 mm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# GaN Semiconductors

- Electrical Performance

  - Smaller $C_{iss}$, $C_{oss}$ and $C_{rss}$
  - Faster switching speed
  - No reverse recovery loss
  - No avalanche breakdown

7 x 4,5 mm


8 x 8 mm


21 x 16 mm



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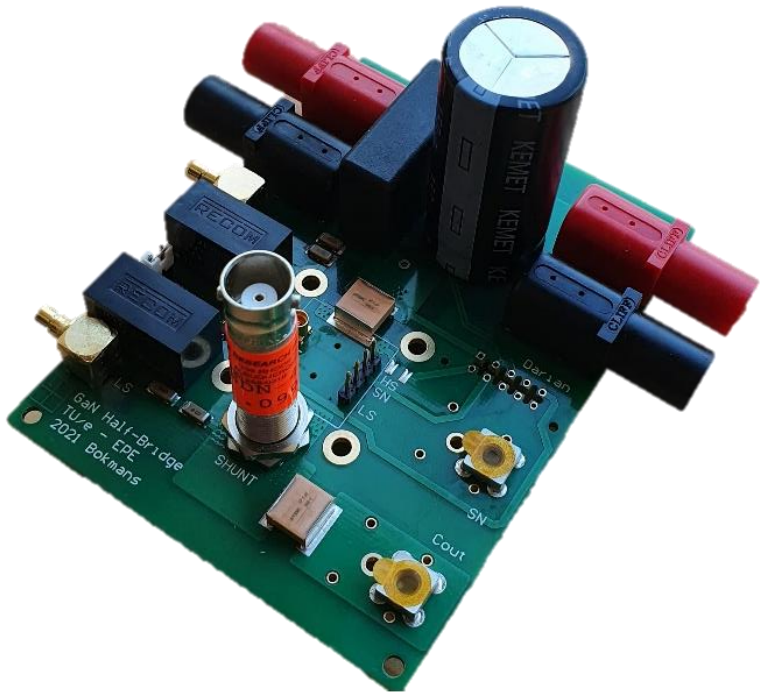
# GaN Semiconductors

- Advantages
  - ➢ Higher efficiency
  - ➢ More compact design
  - ➢ Reduced weight
  - ➢ More development effort

GaN 350W micro PV inverter

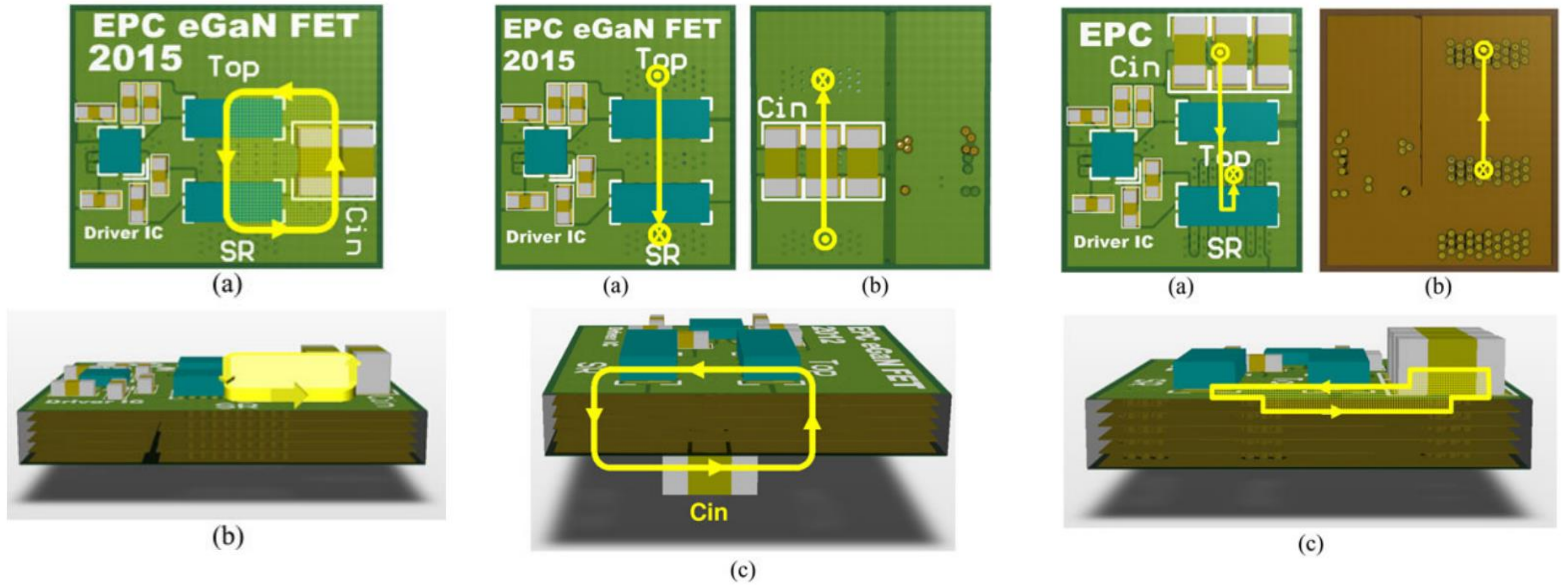

USB-C PD 140W

# Design Considerations



# Design Considerations

- Powerloop PCB layout

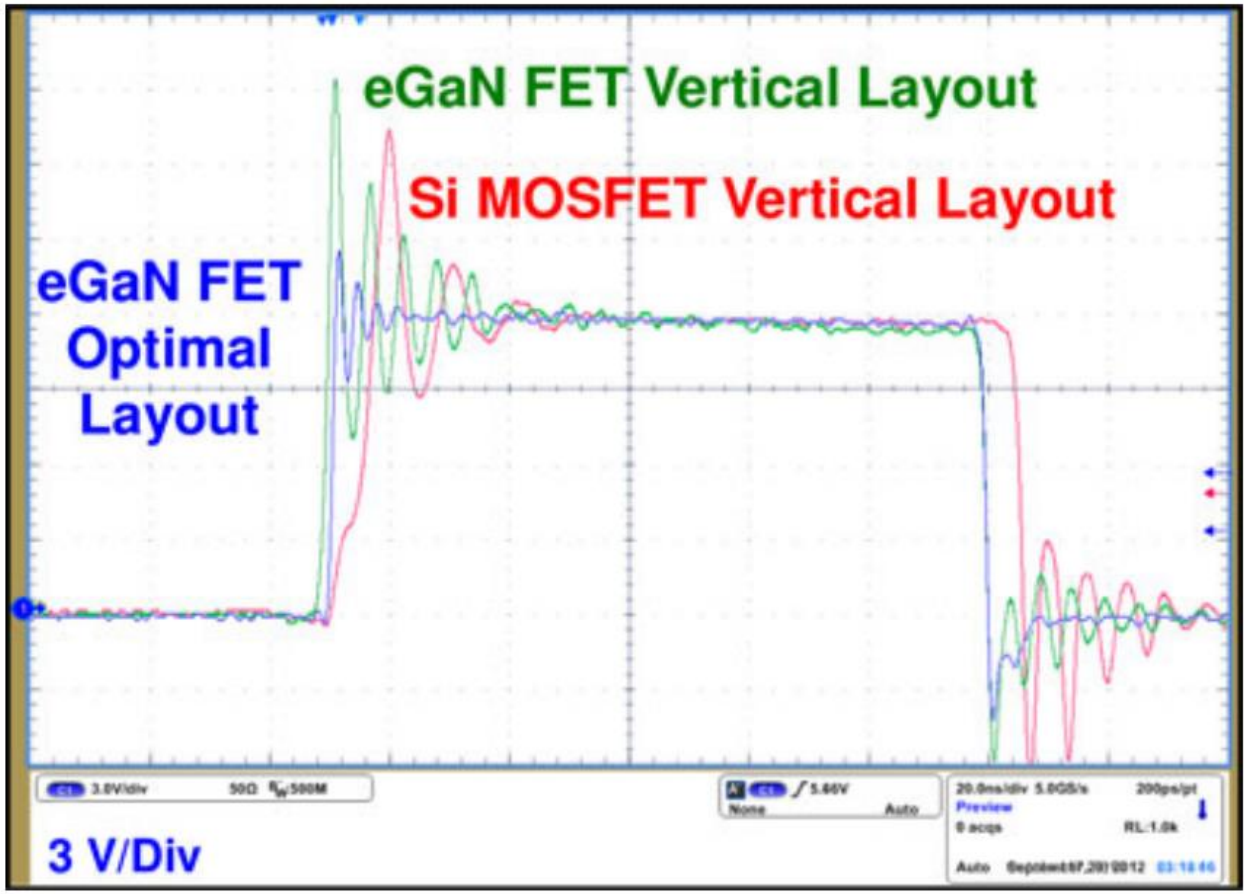


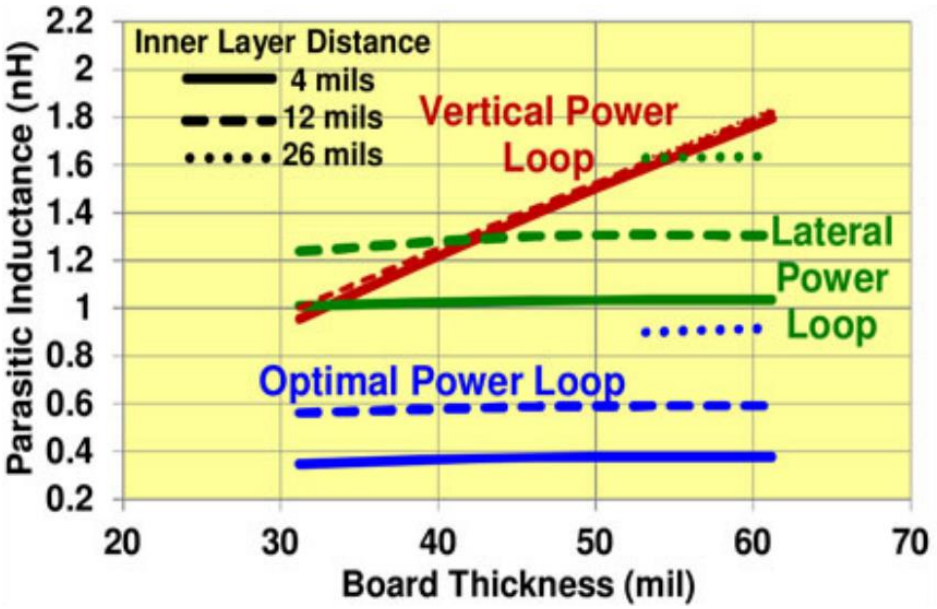

Lateral Vertical Optimal

*Reusch, D and Strydom, J. Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter*

# Design Considerations

- Effect of PCB layout on switching performance

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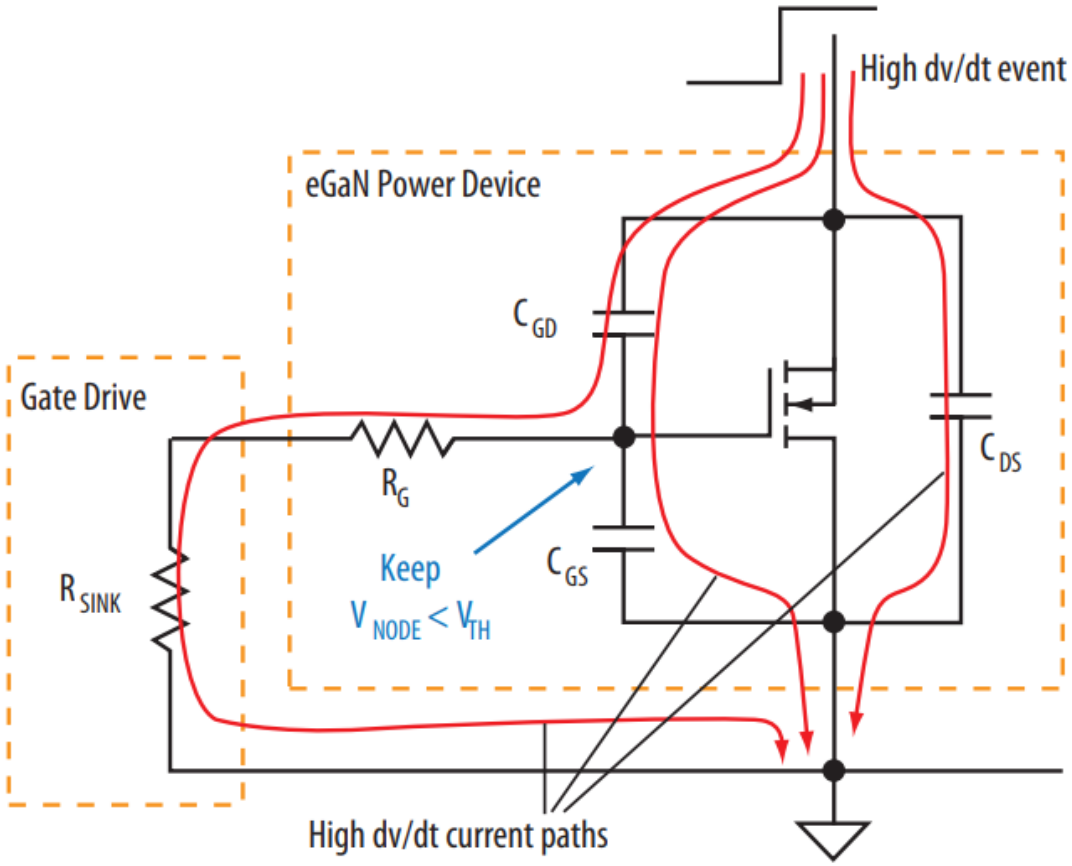
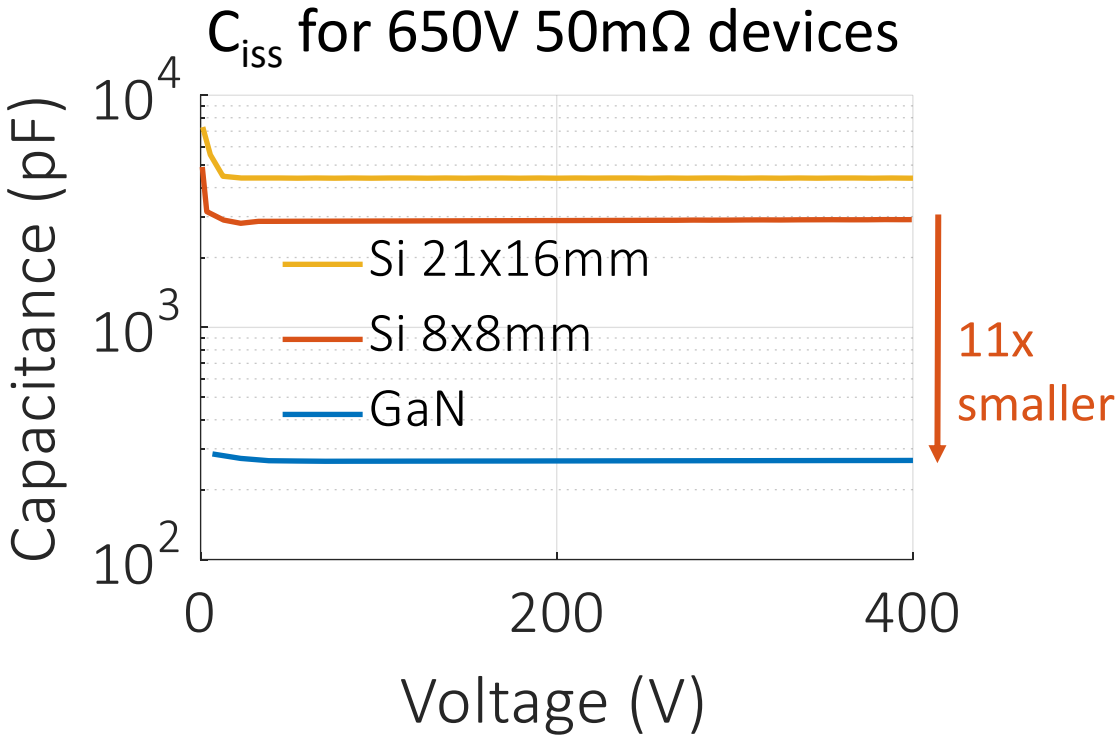
# Design Considerations

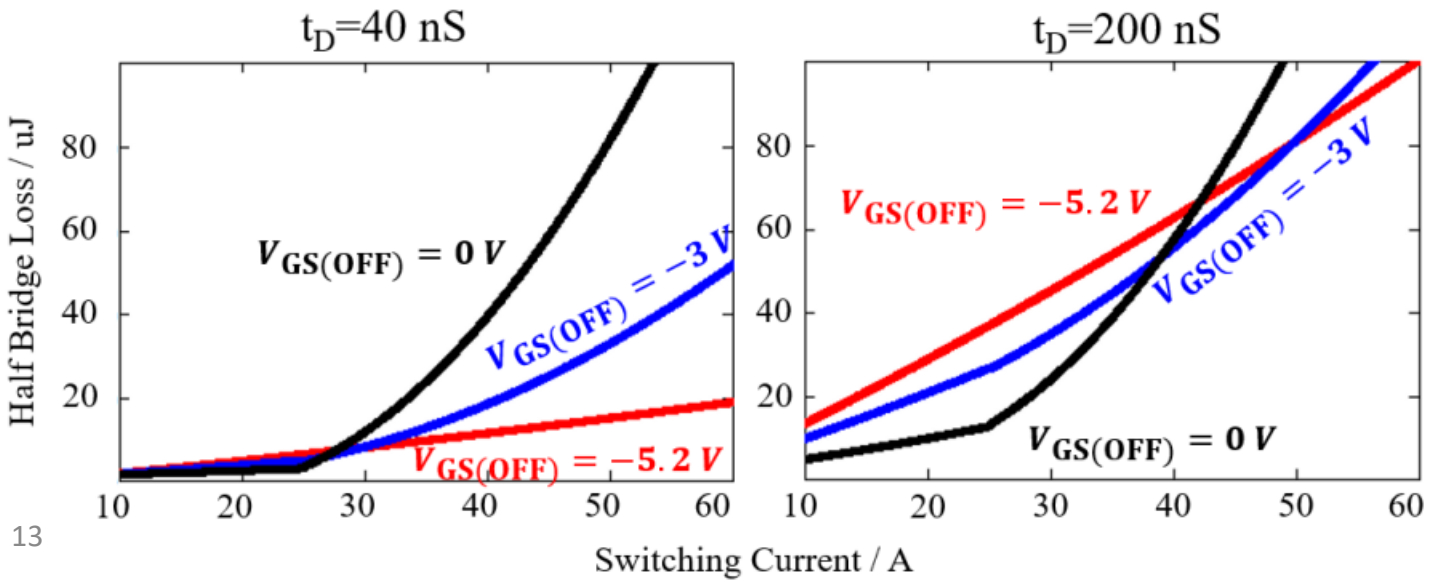
- Gate driving



# Design Considerations

- Gate driving
  - Minimize gate loop inductance
  - Slowing down switching speed
  - Using negative turn-off voltage

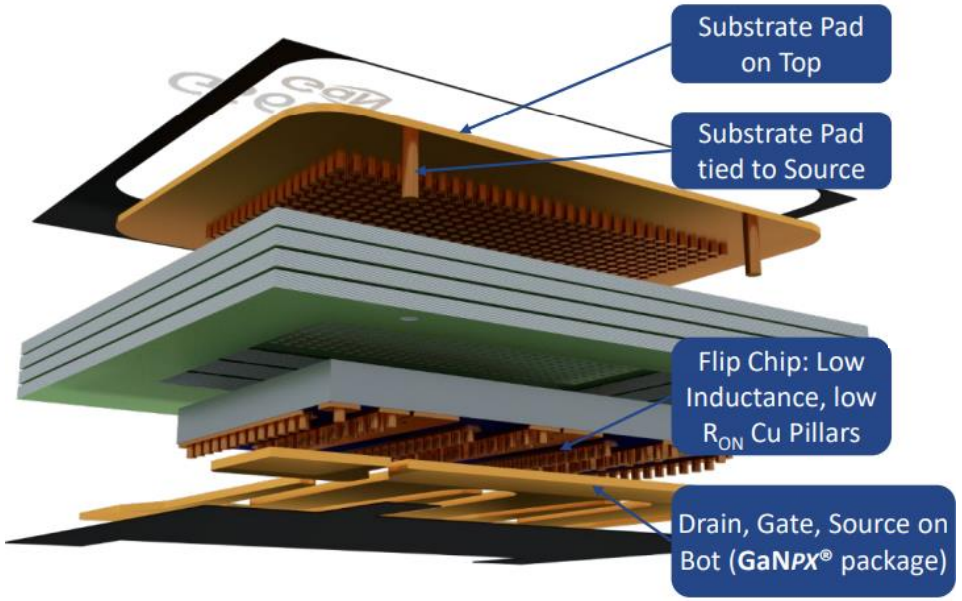


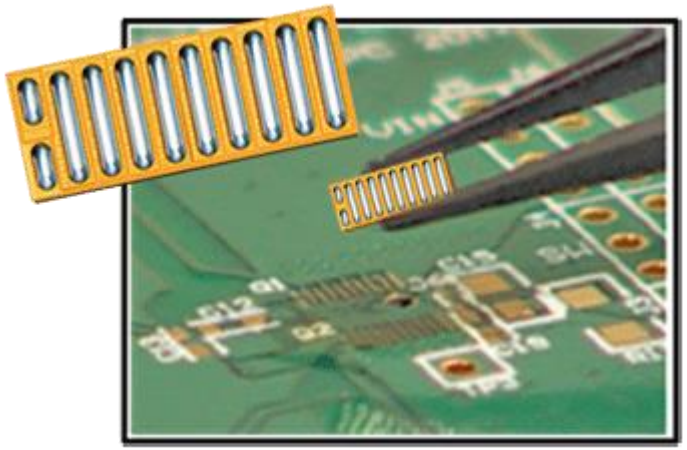

*GaNSystems: half-bridge loss vs switching currents under varying turn-off voltages for 40ns and 200ns dead-time*

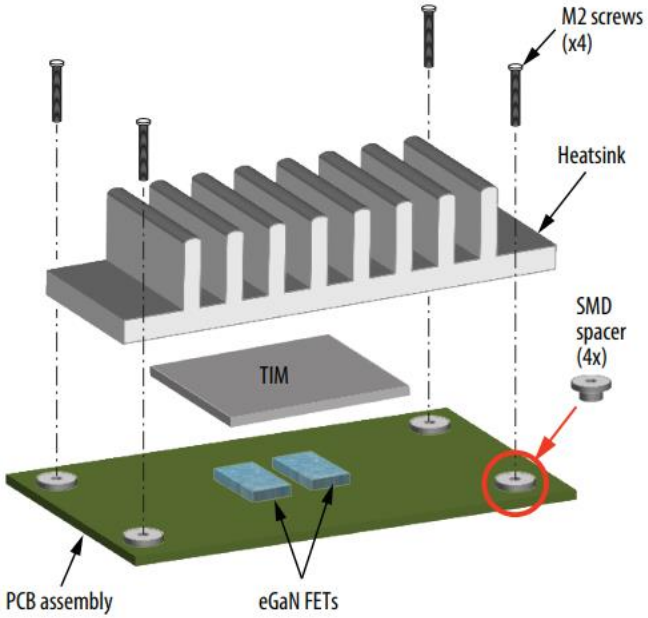
# Design Considerations

- Cooling

Extracting heat from 2 … 100 mm2 chip area





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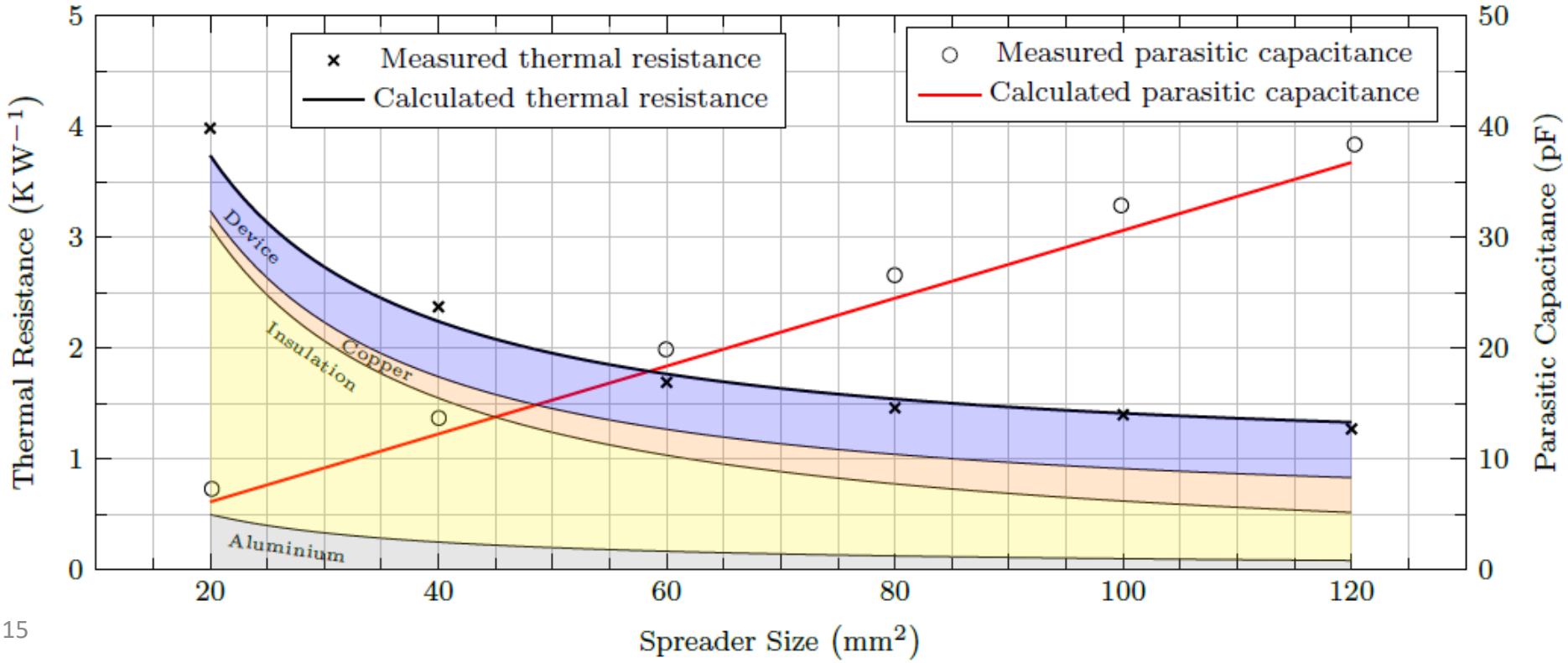
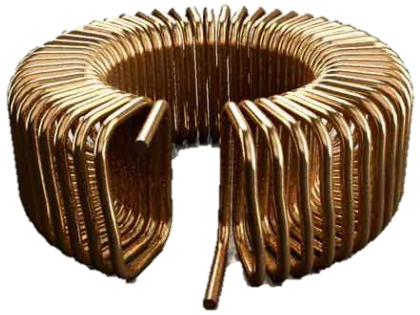
# Design Considerations

- Heat spreaders

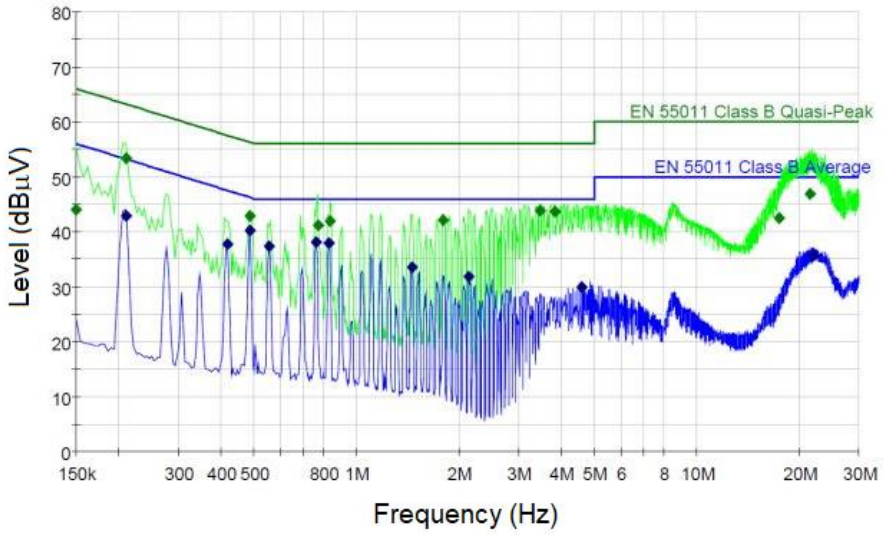


# Design Considerations

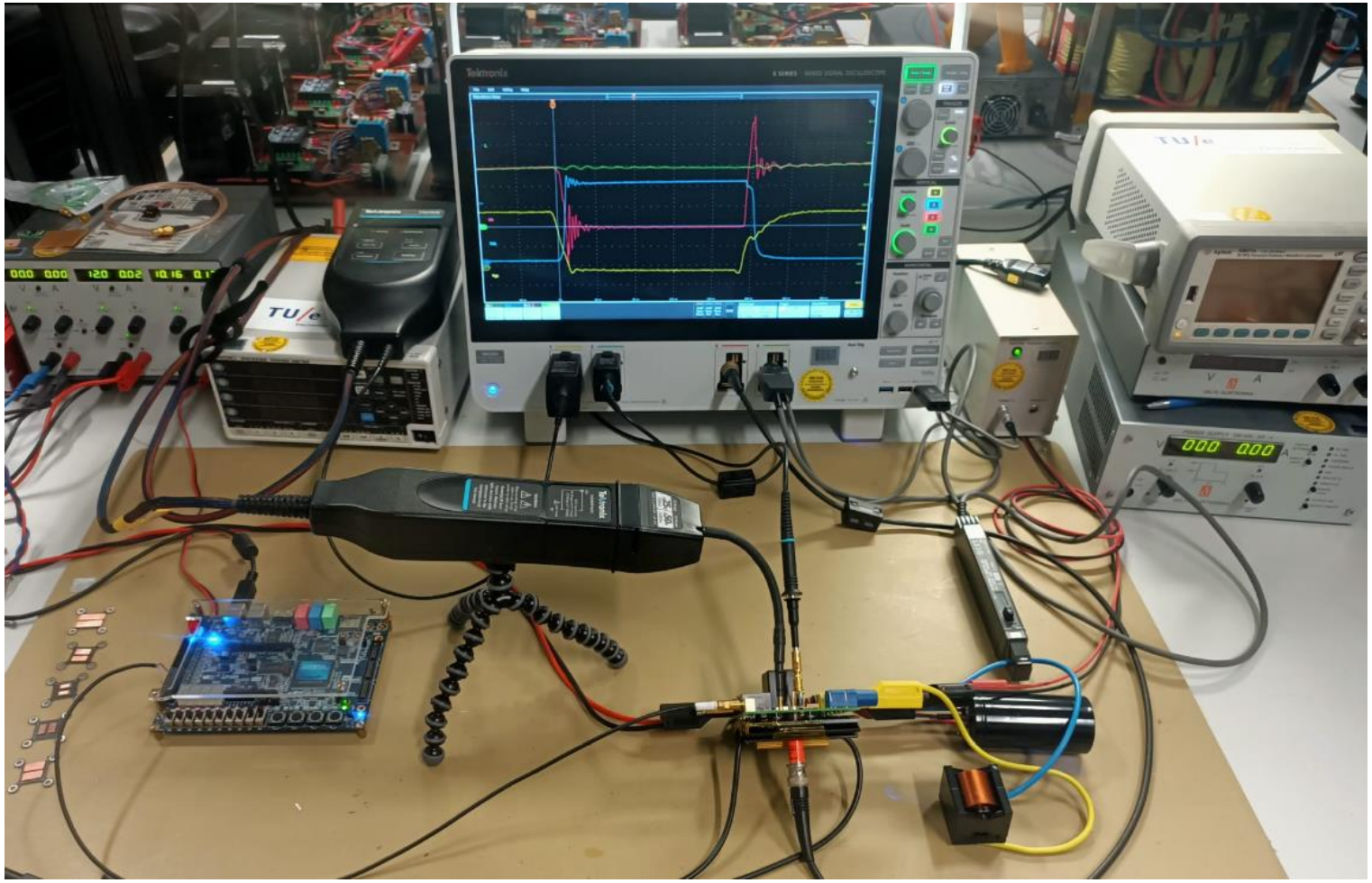
- And many more…
  - Magnetics
  - Measurements
  - Control and modulation
  - EMI
  - Reliability



$$\hat{\boldsymbol{x}}[n+1] = \Phi\,\hat{\boldsymbol{x}}[n] + \Gamma\,\boldsymbol{u}[n] + \boldsymbol{L}\boldsymbol{e}[n]$$

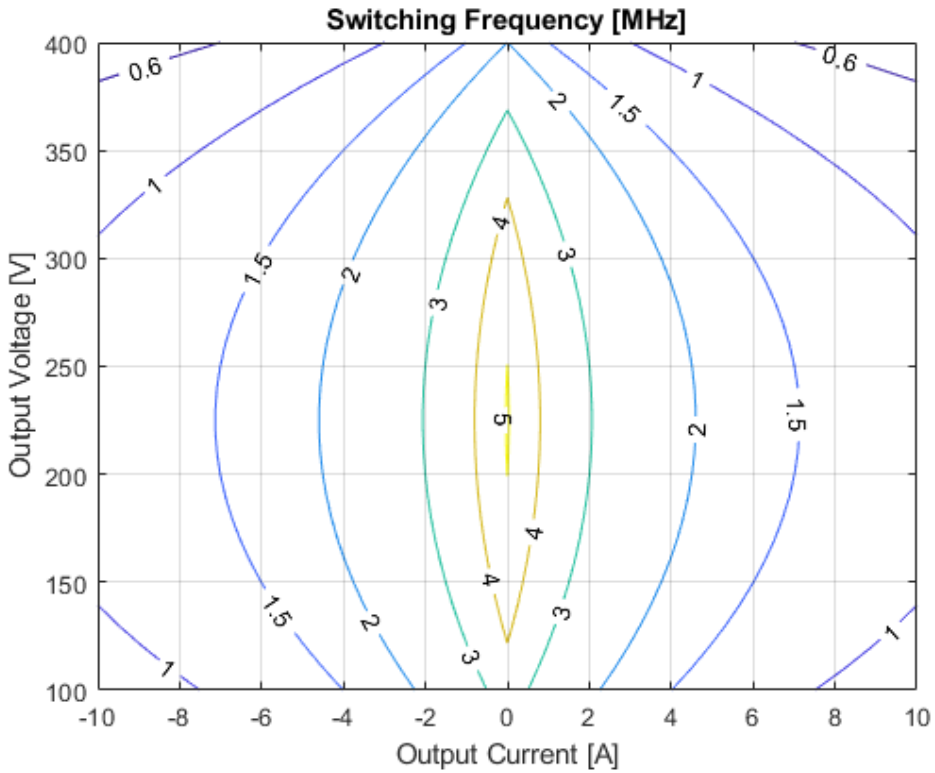


# Prototype



# Prototype

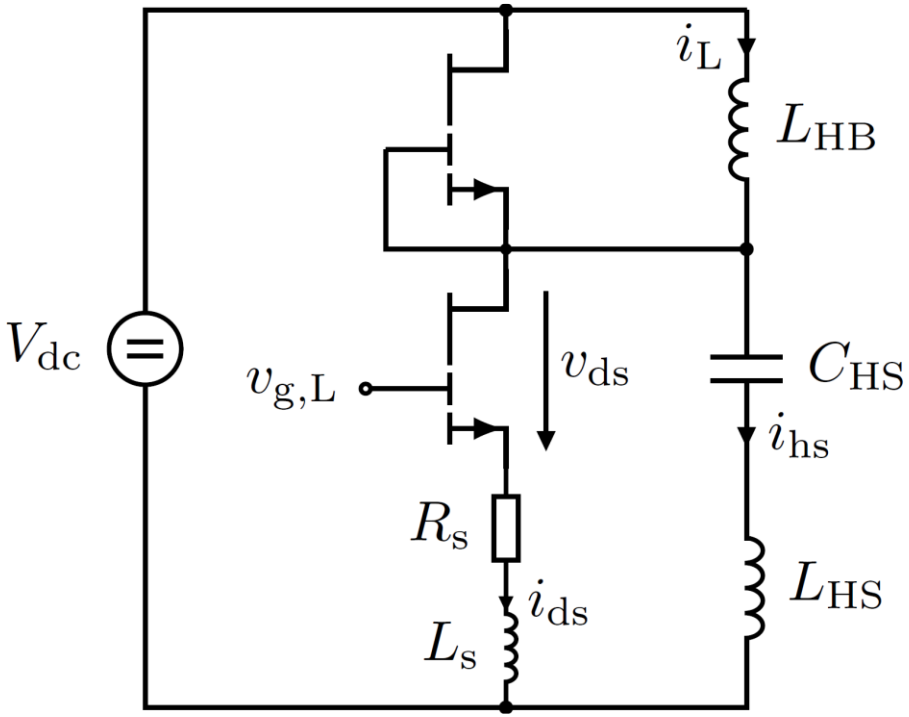
- Non-isolated DC/DC converter
  - Input voltage 450 $V_{dc}$
  - Output voltage 100 … 400 $V_{dc}$
  - Output current - 10 … 10 A
  - Maximum power 3600 W
  - Zero-voltage switching
  - Variable switching frequency

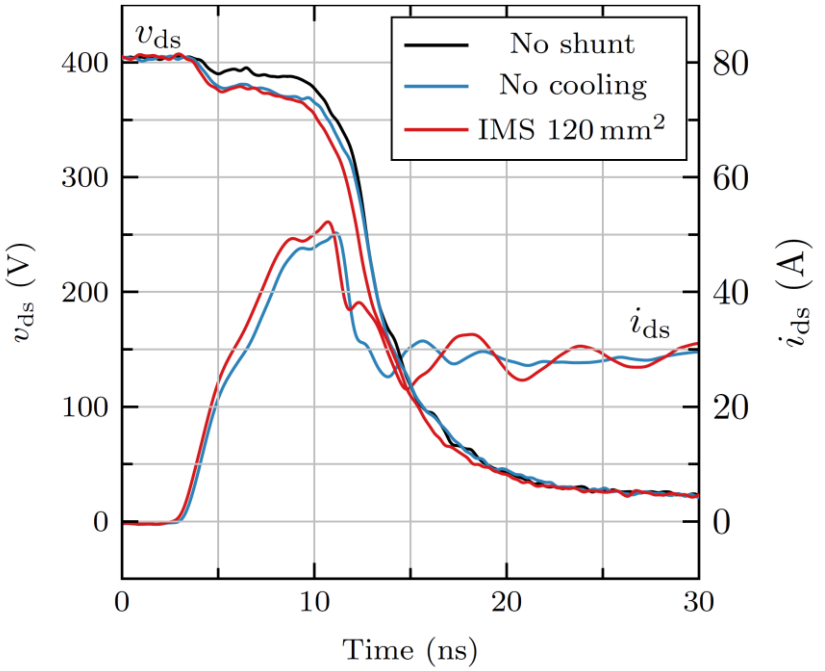


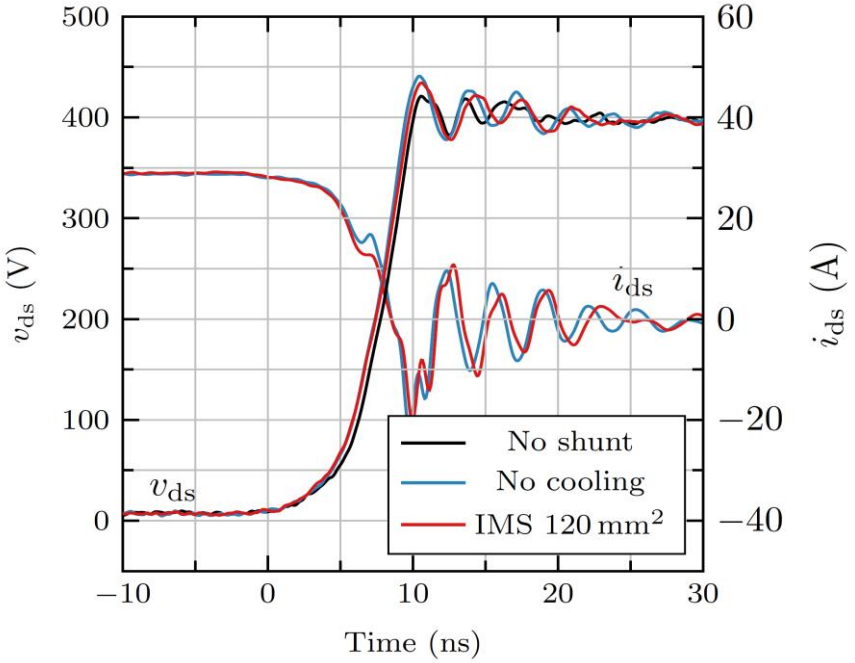

- Demonstration at stand 12

# Prototype

- Double-pulse test

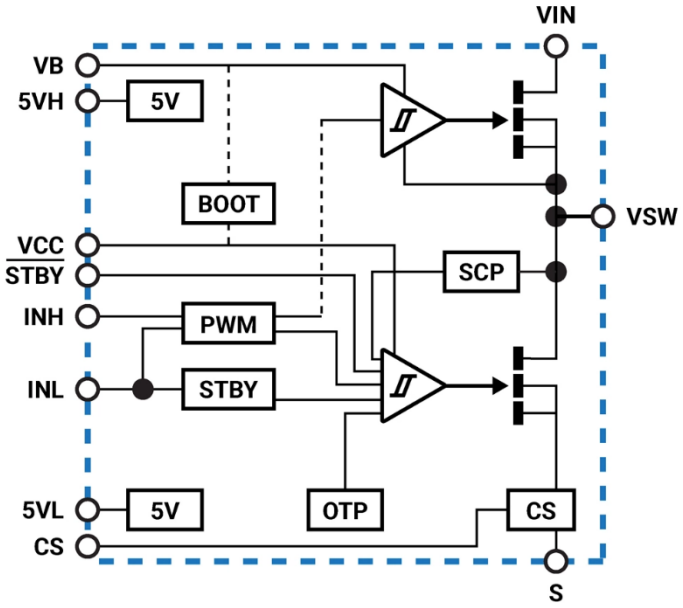


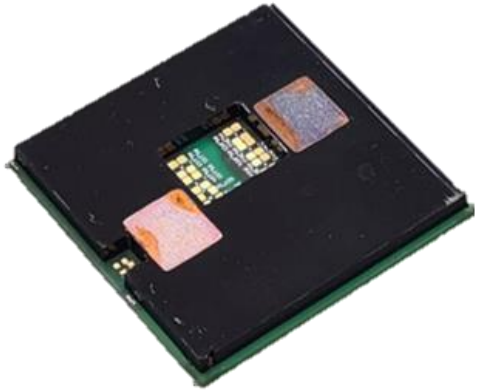



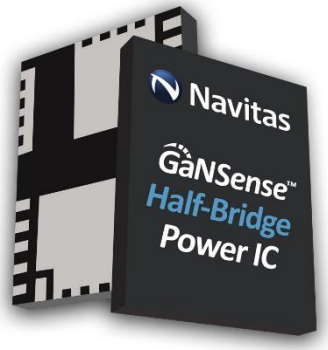
# Prototype

- Towards monolotic integration
  - ➢ Further reduction of cost

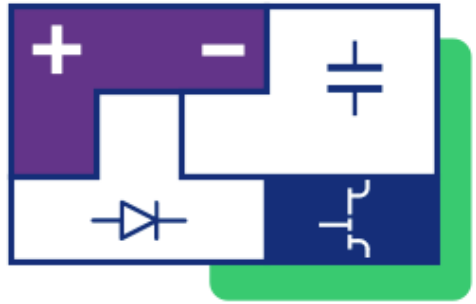


GaNext IPM




Navitas IC



ALL2GaN

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# Thank You

## For Your Attention

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