

TRENDS IN ESD PROTECTION OF AUTOMOTIVE IC'S

DESIGN, STANDARDS &
BEYOND

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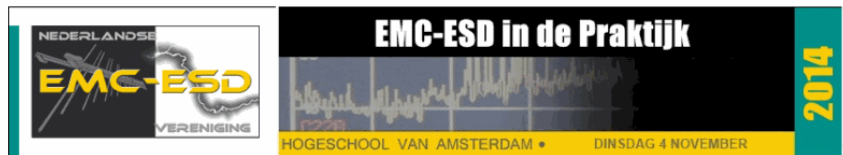
ESD PRAKTIJKDAG
4 NOVEMBER 2014



SECURE CONNECTIONS
FOR A SMARTER WORLD

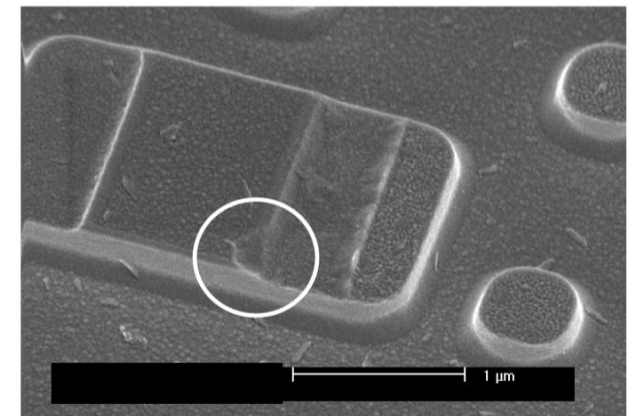
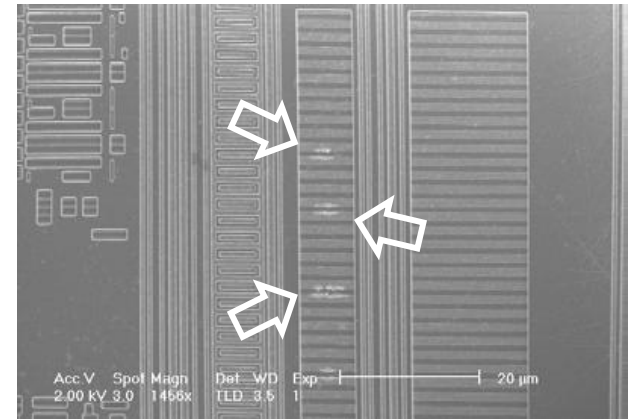
Presentation outline

- Introduction
- Component level ESD standards
- Automotive ESD standards
- System level ESD & beyond
- On-chip ESD protection design
- Summary

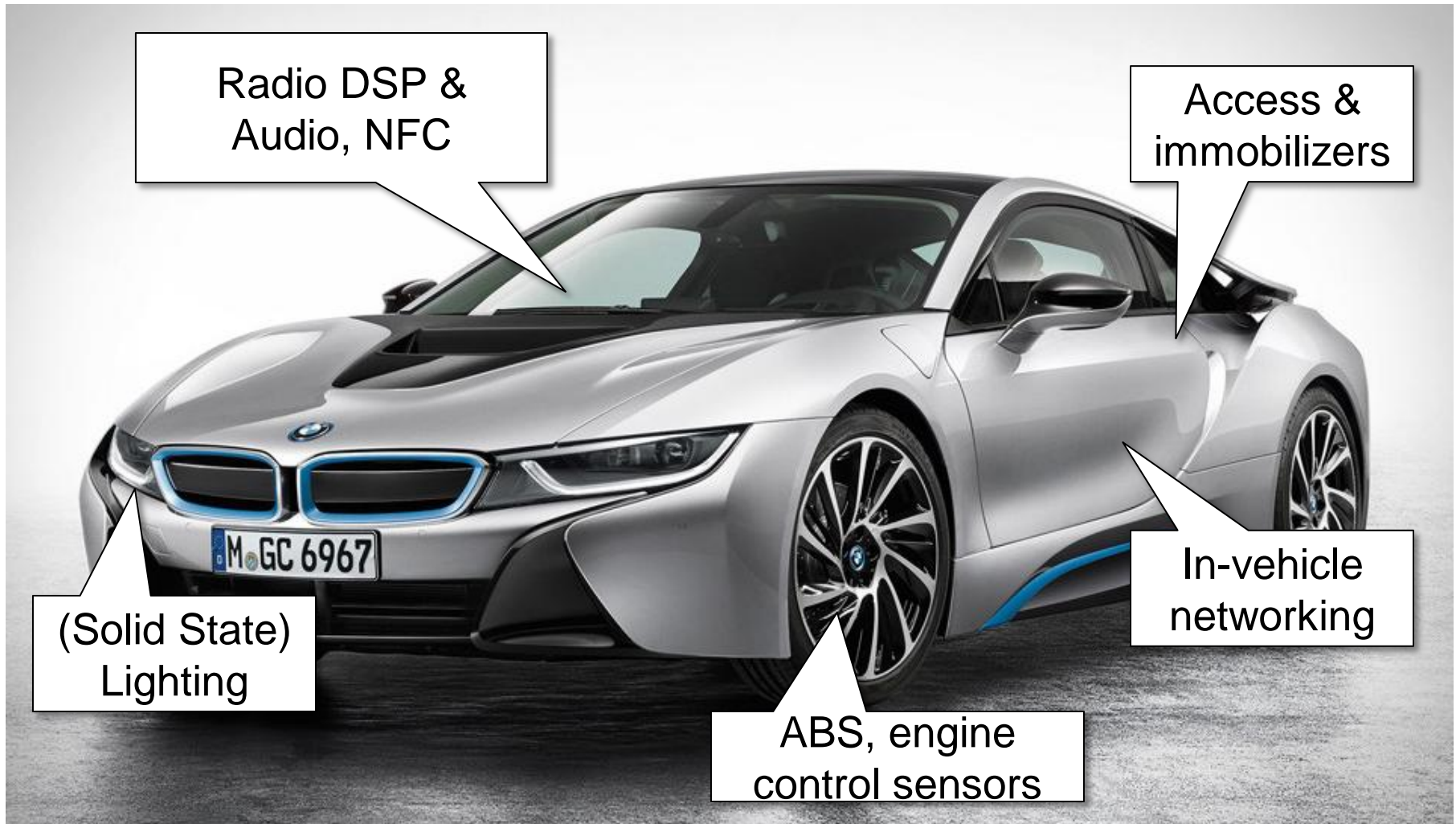


Introduction

- This is a presentation about ESD standards for electronic components for the Automotive Industry
- Automotive industry have high demanding requirements
 - High reliability
 - Safety regulations
 - Hostile environment
 - Low return rate requirement
 - Long life-span
- Semiconductor footprint for automotive is ever growing
- ESD is a key design parameter to quantify robustness



NXP supplies automotive industry



COMPONENT LEVEL ESD STANDARDS



Two worlds of ESD

Component level

- Semiconductor parts
- Handling in ESD controlled environment
- High currents, low energy



System level

- Modules, system boards and complete products
- ESD uncontrolled environments
- Higher currents, higher but still low energy



Testing ESD susceptibility

- Standards:
 - Classification: Test results in pass/fail for a given level
 - Each standard covers a limited part or real-life ESD
 - To have reproducible results
 - Describe the waveform and test procedure
- In general, semiconductor components are qualified according these standards that address different situations:

Human Body Model

A person discharges to an IC

Machine Model

A tool discharges to an IC

Charged Device Model

A charged IC discharges to its environment

System Level (IEC)

A person discharges through a tool to equipment

Phase out of Machine Model

JESD22-115C (Nov 2010)



- “Classification testing” renamed to “Characterization”

- Notes:

- “[...] in ESD used integrated quality
- Only necessary

- JEP172

The Machine Model

ESD Qualification”

ANSI/ESD S5.2 > STM5.2



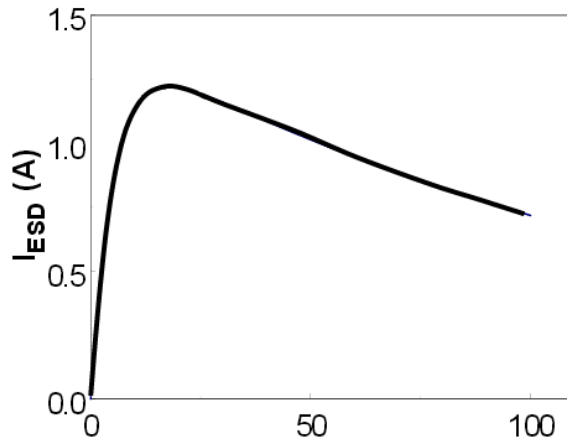
- ANSI standard S5.2 has been replaced by standard

Motivation:

Observed failures for MM are strongly correlated to HBM results. They only occur at a lower stress voltage.

Therefore, MM yields no added value and only increases cost.

ESD Standard pulses compared



2 kV HBM

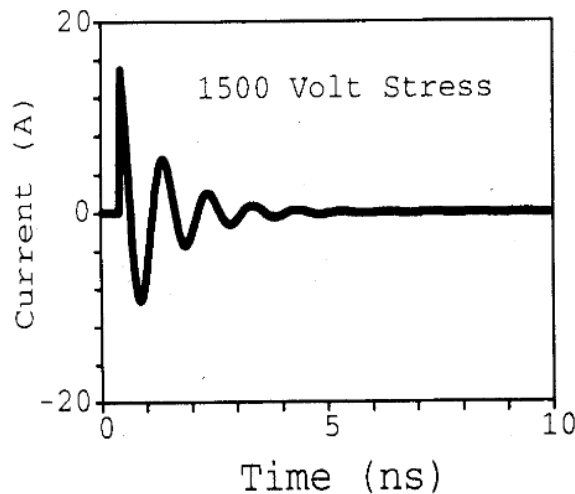
$I_p=1.3A$

$Tr \sim 8 \text{ ns}$

$Td \sim 200 \text{ ns}$

General pulse characteristics:

- High power
- Low energy
- Nano second time frame



**1500 V
CDM**

$I_p=15A$

$Tr \sim 100 \text{ ps}$

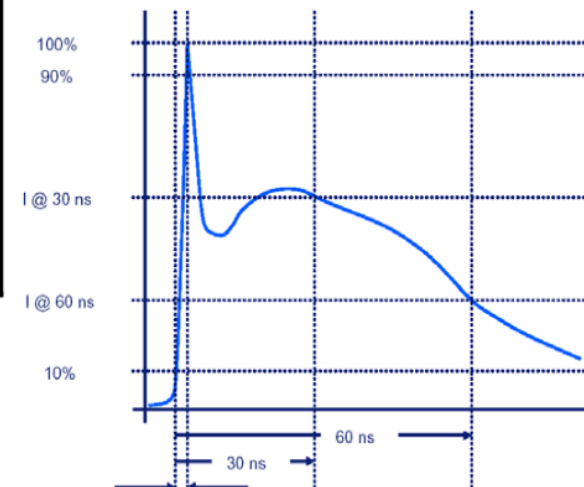
$Td \sim 1 \text{ ns}$

4 kV IEC

$I_p=14A$

$Tr \sim 200 \text{ ps}$

$Td \sim 100 \text{ ns}$



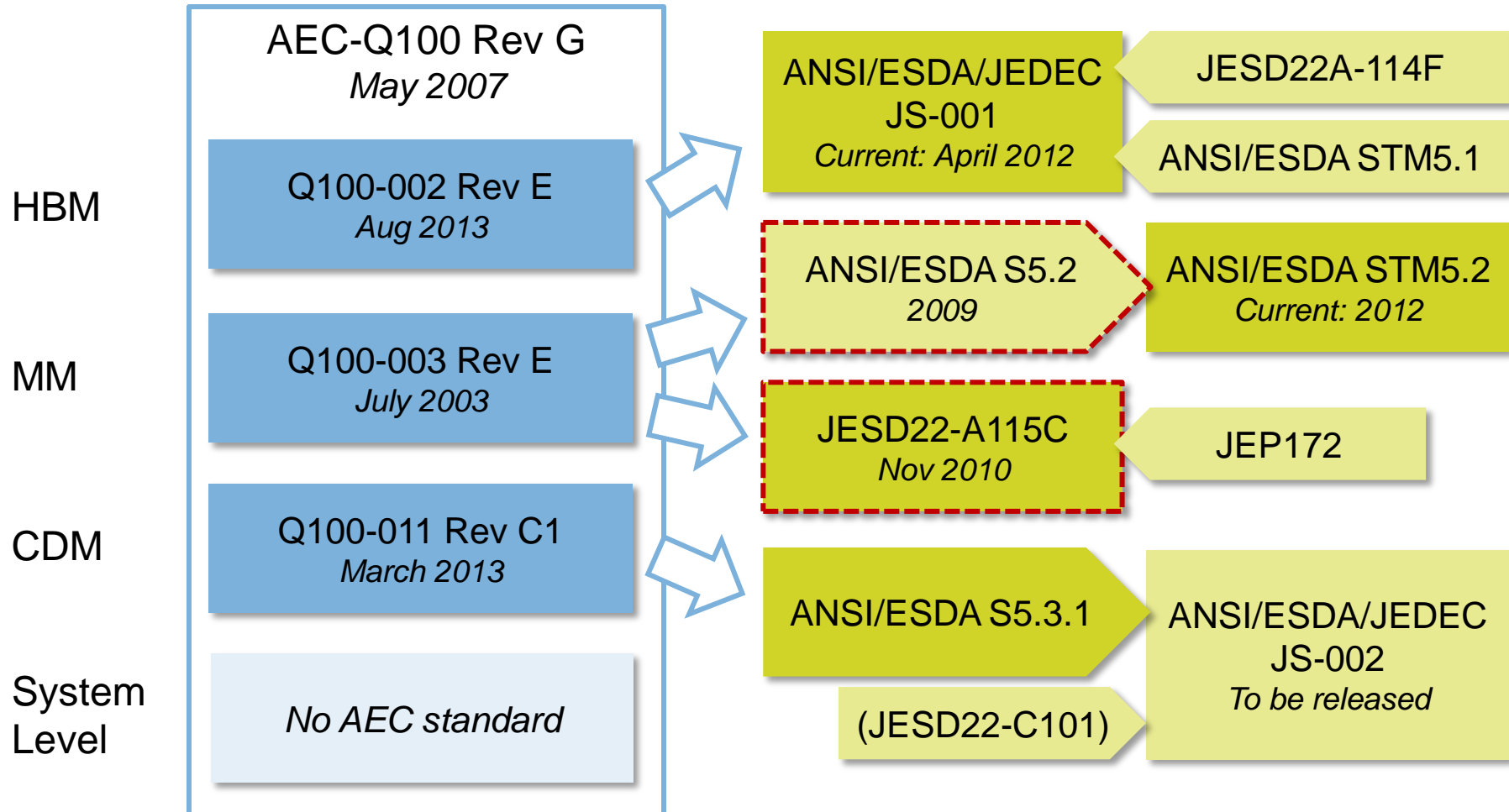
AUTOMOTIVE ESD STANDARDS

Automotive industry



- Demanding requirements
 - Hostile environment
 - Low return rate requirement
 - Long life-span
- ... for niche market!
- The Automotive Electronics Council (AEC)
 - Issues common qualification specifications for electronics for the automotive industry
 - Lead standard: AEC-Q100 (Stress Qualification for IC's)
 - **ESD and Overstress**
 - **Life test**
 - Originally established in by Ford, Chrysler and GM in early 90's
 - NXP is Technical Committee Member since 2005



Anatomy of AEC-Q100 Rev G (ESD only)



Recent developments in AEC-Q100



- AEC-Q100 Rev H is to be released soon:
 - Ballot passed Sept/Oct 2014
 - MM standard is removed
 - Intention to follow ANSI/ESDA/Jedec JS-002 for CDM
- ANSI/ESDA/Jedec JS-002 (CDM)
 - Second joint standard between ESD Association and Jedec
 - Merge of JESD22-C101 and ANSI/ESD S5.3.1
 - Focus on backward compatibility
 - Change from voltage level defined to current level defined stress

Organization			Previous step	Next step
ESDA			Accepted	Industry review
Jedec			Ballot passed	Approval by Board of Directors

A close-up photograph of a small electronic circuit board mounted on a circular test fixture. The board is populated with various components, including a green integrated circuit, resistors, and a gold-colored connector. A blue probe with a yellow tip is connected to one of the components. The entire setup is positioned under a microscope, which is visible in the upper left corner. The background is dark and out of focus.

SYSTEM LEVEL

ESD & BEYOND



System Level ESD

- No AEC standard because AEC is component level only
- Still, more and more customers require a component to PASS a system level requirements
- System level standard IEC-61000-4-2
- ANSI ESD SP 5.6 (Human Metal Model) for IC components *Ref [8]*

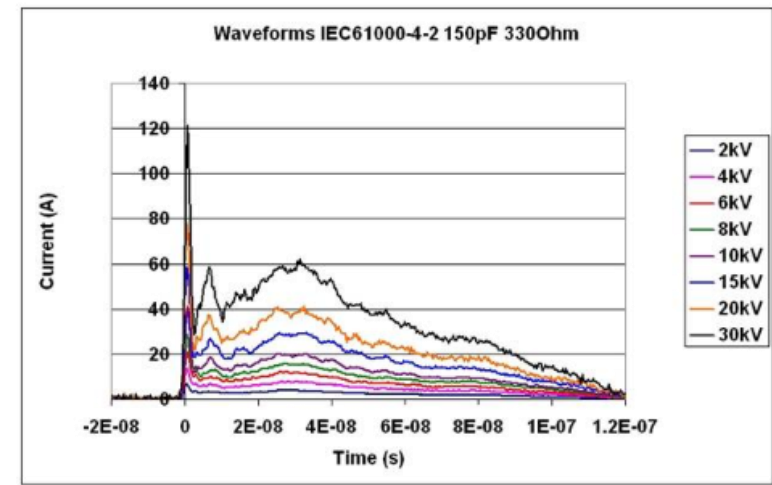
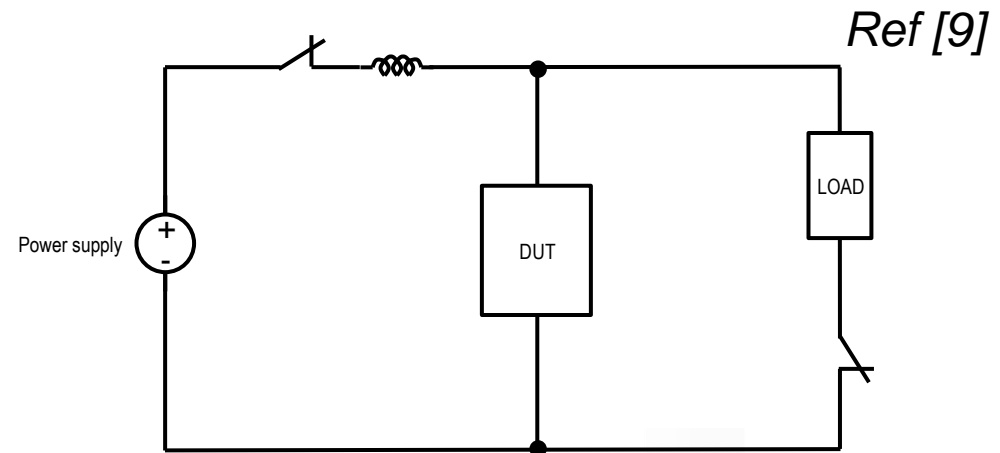
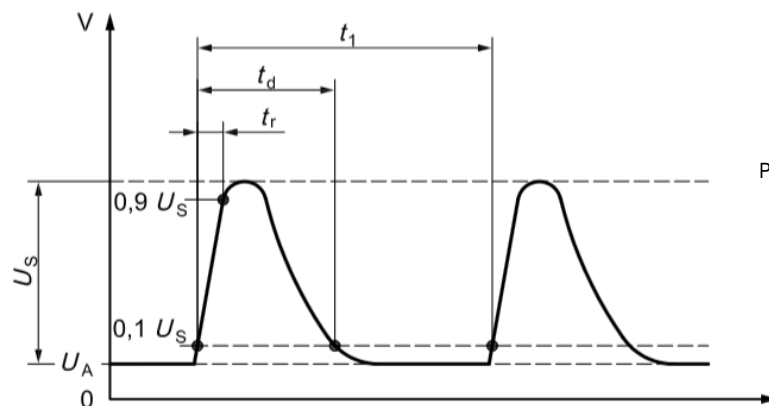


Figure 5: Measured waveforms of contact discharge from an IEC 61000-4-2 ESD gun on the prescribed calibration target

Other standards

- ISO7637-2: Electrical disturbances from conduction and coupling
 - System level standard
 - Discharge / overvoltage due to change in inductive load on the wiring loom
 - Voltage spikes up to 112Volts, duration of **50us** (250x longer than HBM!)
 - No ESD test, but EOS test!



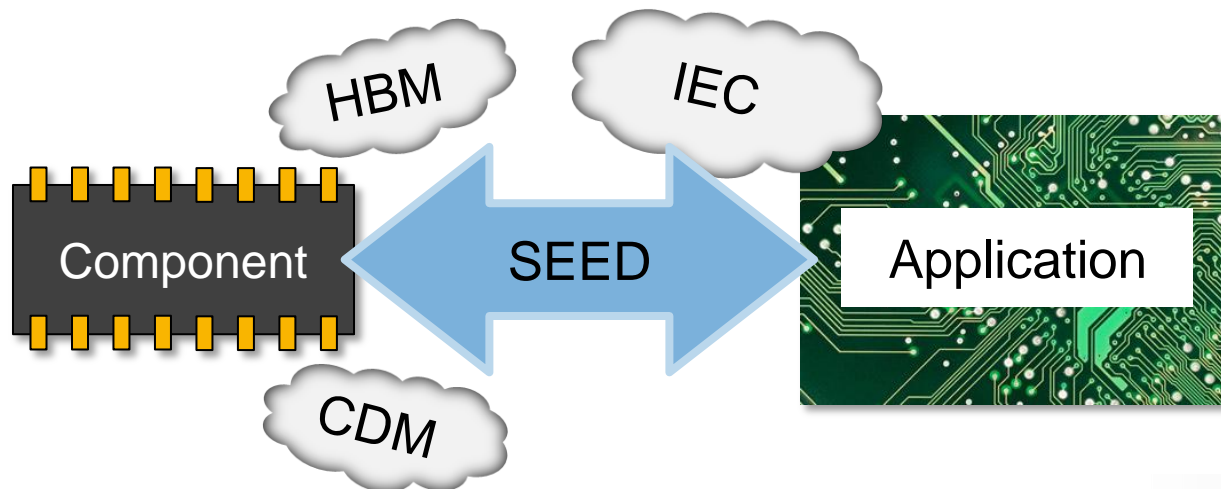
ON-CHIP ESD PROTECTION

Design for ESD robustness

- Mask sets are expensive, therefore a first-time right is eminent!
- Development of an ESD protection strategy
 - Semiconductor process knowledge
 - What can go wrong (blow-up, melt, etc)?
 - How can we prevent that?
 - Create protection infrastructure
- CAD tools
 - Simulation methods (2d simulation and/or SPICE based simulation)
 - Design verification checks. Using Programmable Electrical Rule Checksets (PERC), critical circuit topologies may be identified
- Manual review
 - Of schematic
 - Of physical layout design

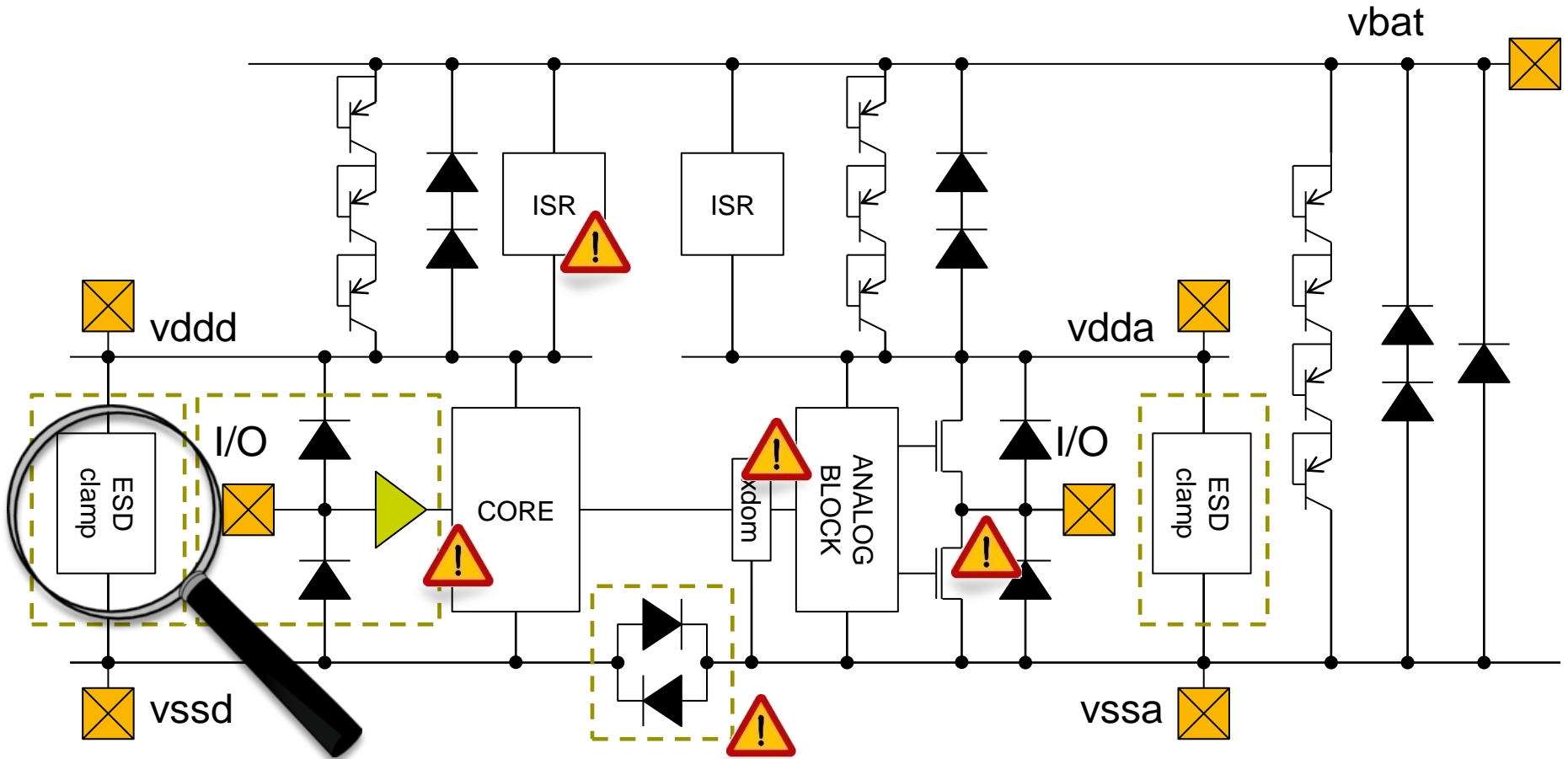
System-efficient ESD Design (SEED)

- Component level ESD does not correlate to system ESD pulses
- High HBM levels do not guarantee a ESD-safe system design, but may limit IO performance
- Understand which magnitude of stress actually arrives on the IO pin in a system application.



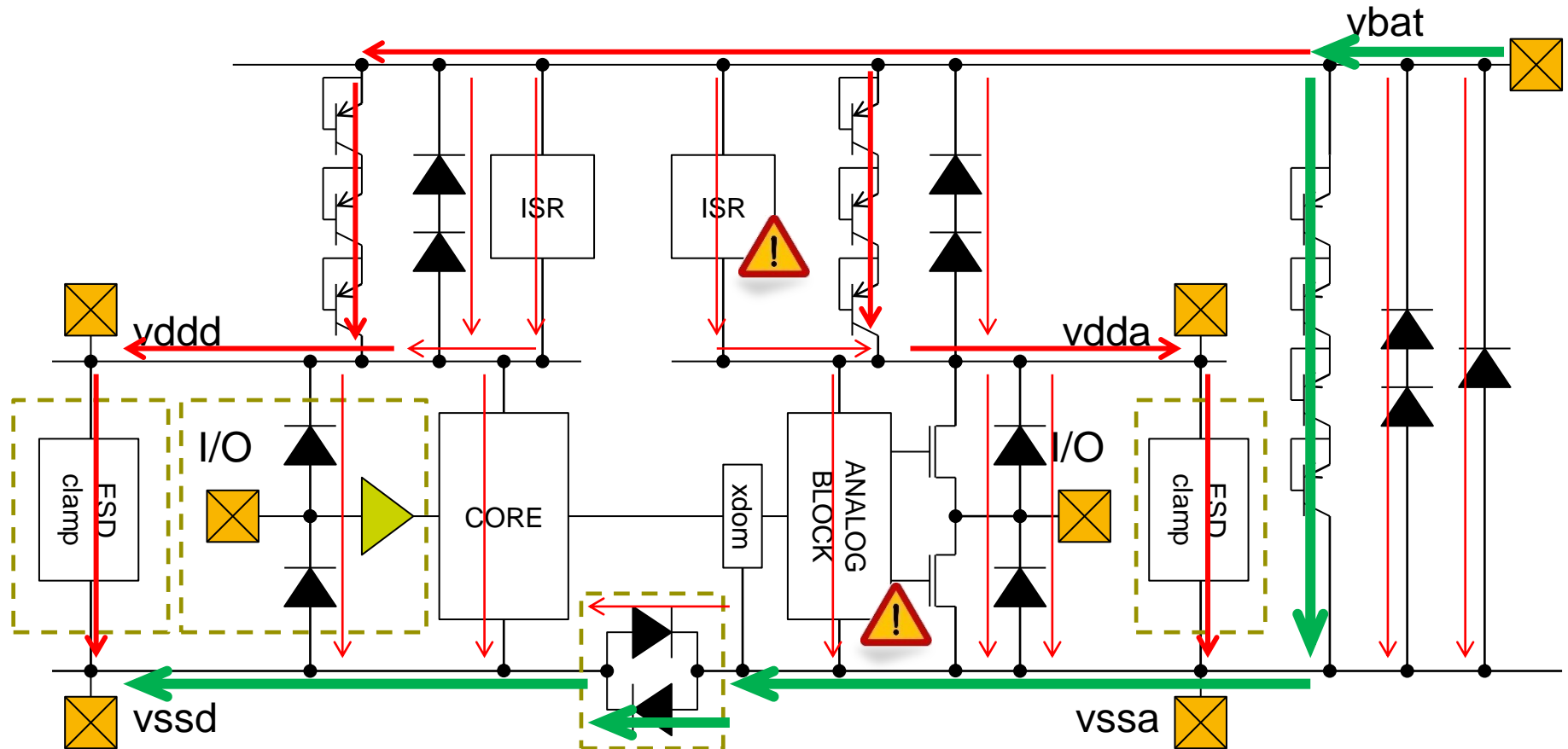
Ref [8]

Semi-automatic circuit analysis



Not a real product. Illustration purpose only.

On-chip ESD simulation



Not a real product. Illustration purpose only.

Summary

- Because the Automotive industry has high demands, design for ESD is a significant effort
- Overview of the AEC-Q100 standard is given
- Some important (expected) changes
 - Expected removal of Machine Model from AEC-Q100
 - Alignment with the soon to be released JS-002 for CDM
- For ESD robustness, engineering takes place on multiple levels
 - Device engineering, strategy development, co-design and troubleshooting
 - Usage of dedicated CAD tools
- ... to have a first-time right design cycle!

THANK YOU!

QUESTIONS?

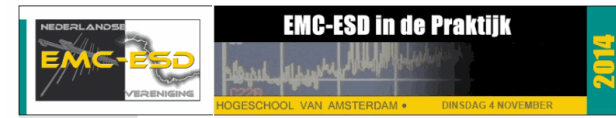


References

1. ANSI ESDA/JEDEC JS-001, Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level
2. ANSI ESD S5.3.1, Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Component Level
3. Jedec JESD22-C101, Field-induced Charged-Device Model Test Method For Electrostatic-Discharge-Withstand Thresholds Of Microelectronic Components
4. ANSI ESD STM5.2, Electrostatic Discharge Sensitivity Testing - Machine Model (MM) - Component Level
5. Jedec JESD22-A115, Electrostatic Discharge (ESD) SENSITIVITY Testing, Machine Model (MM)
6. IEC61000-4-2 Electromagnetic Compatibility (EMC) - Part 4-2: Testing And Measurement Techniques - Electrostatic Discharge Immunity Test
7. ANSI ESD SP5.6, Human Metal Model (HMM) - Component Level
8. ESDA Industry Council on ESD Target Levels, White Paper 3: System Level ESD
9. ISO 7637-2:2011 Road vehicles – Electrical Disturbances from conduction and coupling (Part 2)

Useful links

- ESD Association
www.esda.org
- Jedec
www.jedec.org
- American National Standards Institute
www.ansi.org
- Automotive Electronics Council
www.aecouncil.com
- NXP
www.nxp.com





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