# 9th International Electrostatic Discharge Workshop

# IEW


## May 3-7, 2015
## Granlibakken Conference Center & Lodge
## Lake Tahoe, California, USA

Setting the Global Standards for Static Control!

EOS/ESD Association, Inc. 7900 Turin Rd., Bldg. 3 Rome, NY 13440-2069, USA
PH +1-315-339-6937 • Email: info@esda.org • www.esda.org

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IEW 2014 Poster Session, Grand Hotel de Paris, Villard de Lans, France

# A highly rewarding experience!

The International ESD Workshop (IEW) hosts its 9th annual event at the majestic Granlibakken Conference Center & Lodge, Lake Tahoe, CA. Located in beautiful Lake Tahoe, this setting provides the perfect opportunity for participants to meet in a relaxed, invigorating atmosphere and engage in discussions about the latest research and issues of interest within the EOS/ESD community.

The IEW facilitates access to and interactions with industry leaders through invited seminars, technical sessions, special interest groups (SIGs), discussion groups (DGs), and invited speakers. This year we focus on Power Management for EOS/ESD and EDA EOS/ESD Tools Best Practices and Experiences.

Experience the uniquely interactive program of the IEW Workshop.
- Listen to viewpoints of industry experts
- Share your ideas and opinions on EOS/ESD topics
- Explore industry best practices and give your inputs
- Interact and network with high-level EOS/ESD industry experts

A highly rewarding experience and engaging experience for all! Whether you are new to EOS/ESD topics, or an old hand at it - join us at IEW 2015 to learn in an informal, interactive, and friendly atmosphere.

# EXPERIENCE IEW

Welcome to the 9th annual International ESD Workshop (IEW). This important event offers the unique opportunity to learn and discuss technical issues on EOS and ESD topics in an informal and friendly environment, encouraging extensive interactions among all attendees.

This year, the IEW will take place at the majestic Granlibakken Conference Center & Lodge in Lake Tahoe, CA. Located in beautiful Lake Tahoe, Granlibakken is surrounded by the Tahoe National Forest occupying 74 wooded acres in a picturesque mountain valley at an elevation of 6,350 feet. Friendly but shy bears and other wildlife can be spotted on occasion.

Scheduled poster sessions form the core of the technical program. These poster sessions are preceded by a brief introduction of each poster by the authors in a plenary “teaser” session. These teasers encourage the participants to select the posters of greatest interest. Meet and chat with the authors, while you expand your knowledge and network in the subsequent poster discussion session. This format provides an ideal forum for learning and interchange of new ideas. Topics covered in the poster sessions include IC EOS/ESD design, verification, test, multichip and system level ESD. For details see the schedule starting on page 13.

The discussion groups (DGs), held in the evenings, are a unique part of our interactive workshop. While each EOS/ESD topic discussion is facilitated by an expert on the subject, the main discussion will take place among the DG participants. The discussion groups will address topics of the focus issues and include 3D-IC, ESD Compact (SPICE) Models, ESD FOS (From Outside to Surface), Latch-up Testing and other interesting topics. The IEW also provides a similar forum for Special Interest Groups (SIGs), on selected subjects that may extend beyond the IEW time frame. Some SIGs have been successfully meeting for several years.

A number of stimulating state-of-the-art EOS/ESD seminars, as well as invited talks are scheduled. Come and listen to presentations discussing Power Management, EDA best practices and other exciting topics.

As a break to EOS/ESD discussions, and to provide an opportunity to enjoy the spectacular surroundings, an afternoon is reserved for recreation with fellow attendees. This is a great way to become better acquainted with your EOS/ESD colleagues.

Come and meet experts, share your views, ask questions, and extend your network with EOS/ESD experts from industry and academia. Above all, learn how to efficiently deal with today’s EOS/ESD challenges and prepare for tomorrow in an informal and interactive atmosphere. Register for this event early. This will help us in the final planning and preparation for a highly successful event. We sincerely hope that you will join us in Lake Tahoe for the 2015 IEW.

# WELCOME

## Sunday Evening Entertainment-Lake Tahoe: Stories, Facts & Fun

*Mark McLaughlin*

**Lake Tahoe: Stories, Facts & Fun:** This Snapshot History of Tahoe will showcase important and colorful characters that played a role in the development in Western Nevada and Lake Tahoe. Mark will present a collection of entertaining stories illustrating regional history including the early logging, railroad, and steamship eras. As a special feature, Mark will talk about a few easy hikes for historical exploration in the Tahoe-Truckee region.

Tahoe historian Mark McLaughlin is an award-winning, nationally published author and professional speaker with six books and more than 700 articles in print. Educated as a geographer and historian at the University of Nevada, Reno, Mark has received the Nevada State Press award five times. He has appeared on CNN, The History Channel, and The Weather Channel, and participated in many documentaries. Mark is currently working with The Weather Channel on a new Donner Party documentary. His newest book, Snowbound: Legendary Winters of the Tahoe-Sierra, is due out in 2015.

# KEYNOTE

Keynote Speaker Chair: Robert Gauthier, IBM

## A Perspective on Transistor Architectures - Bulk and SOI, Planar and FinFETs - for 28nm to 7nm Generations

*Terence B. Hook, IBM*

The industry has seen a sea of change in transistor architecture for leading-edge technologies in recent years. The wavefront of this change, while centered around the 20nm node, has propagated backward to 28nm, and of course rolls forward into 14nm, 10nm, and beyond. Across this wide spectrum, a number of permutations vie for supremacy: PDSOI, bulk planar, FDSOI, bulk FinFETs, and SOI FinFETs. For those not involved on a daily basis with these devices, the task of sorting out the key characteristics - the advantages and drawbacks of each - can be daunting. We will review the salient features and challenges of each type of device, and provide prognostication as to the future trajectory of each for leading-edge applications.

Terence Hook has been with IBM since 1980, after receiving his B.S. degree from Brown University. He earned his Ph.D. in EE from Yale University in 1986, pursuing various aspects of tunneling and interface characteristics in silicon dioxide systems under the tutelage of Prof. T-P. Ma. While at IBM he has worked on technology integration and device design for bipolar, BiCMOS, and CMOS technologies all the way from two micrometer down to the leading-edge current environment in the 5nm range. In addition to transistor architecture, some of his particular special interests have included process-induced charging and also transistor variability. He has authored many conference, journal papers, and book chapters and holds some sixty or so patents. He is currently a Senior Technical Staff Member, dividing his time between Essex Junction, Vermont, and Albany Nanotech in Albany, New York.

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# INVITED TALKS

Invited Speaker Chair: Souvick Mitra, IBM

Invited talks are one of the key elements of the workshop, featuring the theme of the workshop as well as focusing on some advanced topics of interest. There are five invited talks this year. Three of these will be aligned with the theme of this year's workshop: Power Management for EOS/ESD, EDA, and EOS/ESD Tools Best Practices and Experiences. Industry leaders and experts from TI, NXP, and Freescale will share their thoughts on these topics in the invited talks. Also an invited talk from imec will provide insight into latest technology developments and impact on ESD. In the the fifth invited talk, a renowned industry expert will discuss and deep-dive into CDM qualification with perspectives from Technology Impact, Testing and Targets.

## Invited Talk 1

**ESD Challenges Along the Technology Scaling Roadmap**

*Dimitri Linten, imec*

To maintain the scaling roadmap at the 20nm node and beyond, standard planar CMOS have been replaced by 3D FinFETs. These devices have shown improved leakage and short channel control. To maintain this technology scaling beyond the 10nm node, high mobility channel materials, like e.g. compressive strained SiGe or Ge for PMOS and III-V materials or tensile strained Ge for NMOS are being considered. Besides changing the channel material, alternative device architectures like Gate-All-Around devices (GAA) are investigated, sometimes in combination with the new channel materials. Each of these options has its own concerns related to reliability and ESD robustness.

In this talk we will present and overview of the state-of-the-art reliability research on the advanced technology options, and provide an outlook on future challenges.

Dimitri Linten received a Ph.D. degree in Electrical Engineering from the Vrije Universiteit Brussel (VUB), Brussels, Belgium in 2006. In 2001, he joined the Wireless Research group of IMEC in Leuven, Belgium. In 2006, he joined the ESD reliability team at imec. From 2012 until 2015 he was the ESD team leader at imec. In 2015 he became the R&D manager of the Device Reliability and Electrical Characterization Group. He is a senior member of the IEEE (SM13). His main research interests are device reliability including ESD for sub-10nm CMOS and beyond Si technologies.

## Invited Talk 2

**Physical Verification and ESD Robustness Check**

*Ertugrul Demircan, Freescale Semiconductor*

Physical Verification methods are increasing in complexity and content with every technology generation. New silicon processes that are developed to meet ever increasing product needs require physical verification methods to be tightly integrated with schematic design data. In this talk, we will present new verification techniques and best practices that enable fast turn around and high quality of designs. These methods include verification of multiple voltage domains, reducing dependence on physical layout marker layers for design rule application and filtering, and ESD robustness and current density/Electro-migration checks.

Ertugrul Demircan received his B.S. in EE and Physics from Bogazici University in Istanbul and Ph.D. in theoretical condensed matter physics from University of Texas at Austin in 1997. Upon graduation, he joined the Interconnect Modeling Group in Motorola Semiconductor Products Sector which then became the Freescale Semiconductor Inc. He has managed a worldwide Physical Verification Group for the development and support of all physical verification collateral for DRC, LVS, LPE, DFM as well as dummy insertion (tiling) and Electro-Migration and IR (EMIR) drop from 0.5µ to 16nm technologies. He has several published articles in international journals and holds eight US patents.


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# Invited Talk 3

## ESD Challenges in Power Management IC Design

*Ann Concannon, Texas Instruments*

In 2014, approximately 40% of world-wide Analog ICs are classified as power management ICs. This segment is predicted to grow as semiconductors proliferate in a wide range of new applications in the automotive, consumer, and industrial markets. The power management product portfolio in TI ranges from isolated AC/DC and DC/DC power supply controllers and non-isolated voltage regulators, such as switching DC/DC converters and linear regulators, to PMIC and LED drivers and display solutions. The ESD protection strategies, design tradeoffs, and technology roadmaps will be discussed for several diverse applications with examples from automotive, consumer, and mobile. ESD for IC and for system level robustness will be considered. Different approaches to meeting ESD qualification targets in an efficient way, with consideration of schedule, verification, and packaging will be elaborated.

Ann Concannon is a Distinguished Member of Technical Staff at Texas Instruments, working in the Analog ESD group, where she contributes to the corporate-level goals of improving design execution on “New Product Introduction”. She works with development teams, design teams, and external customers to engage early on ESD challenges on projects with high visibility on execution and revenue opportunities. Ann was awarded a Ph.D. from the National University of Ireland in 1996 for her contributions to the advancement of device simulation of floating gate non-volatile memory. As a Marie Curie Fellow, she worked on joint silicon device development projects with European Industry, including NXP and ST, while leading a research group at the Tyndall Institute in Ireland. After joining National Semiconductor in 2000, and subsequently Texas Instruments in 2011, Ann has been based in Santa Clara, CA, USA where she has focused on ESD and Power device SOA. Ann is a senior member of the IEEE, and an active member of the ESDA since 2000, with many publications and patents in NVM, Si and ESD.

# Invited Talk 4

## Verification Tools for ESD Protection Engineering

*Michael Khazhinsky, Silicon Laboratories; Hans Kunz, Texas Instruments*

In this talk we will review the options for EDA tools in the ESD protection design flow. The focus will be on implementation verification after the ESD network design, but examples of dimensioning, debugging, and problem analysis will also be touched upon. Three different classes of ESD verification tools will be distinguished: layout based tools, simulation based tools, and netlist inspection based tools. The talk will present examples of each of these classes and will show some results obtained with them. An important part is a discussion of practical boundary conditions for the use of such tools. The talk will end with a summary of the state of the art and a discussion on future development needs.

Theo Smedes received his M.S. and Ph.D. from the Eindhoven University of Technology in 1986 and 1991, with theses on compact device modelling. After he received his Ph.D., he worked at the Delft University of Technology on layout-to-circuit extraction with a focus on substrate coupling. In 1995 he joined Philips Semiconductors (now NXP Semiconductors), the Netherlands. He worked on the development of tools for statistical design for submicron CMOS processes. In 1999 he started working on ESD, Latch-up and EOS. In this role he has published several papers on ESD and introduced an ESD design course within NXP. Currently he is NXP Fellow for ESD and Latch-up. Theo is member of all ESDA device testing working groups. He was co-recipient of the 2007 Best Paper Award and the 2009 Outstanding Paper Award of the EOS/ESD Symposium. Theo has been a member of technical program committees of the EOS/ESD Symposium, IEW, IEDM, IRPS, IPFA, and the ESREF. He served as TPC chair, vice general chair, and general chair of the EOS/ESD Symposium from 2011 to 2013.

# Invited Talk 5

## CDM Qualification: Technology Impact, Testing Nuances, and Target Levels

*Charvaka Duvvury, ESD Consulting*

IC protection against CDM is as challenging as it is critical for the advanced technologies. Scaling of the gate oxides, increasing demand for higher speed circuits built especially in large high-pin count packages are making it impossible to meet the legacy ESD target levels for CDM. These issues are to only become more serious for the upcoming 3D ICs. For high-pin count devices, accurate testing is getting more elusive with accumulated charge buildup making it difficult to discern correct CDM threshold levels. These issues now require exploration of new simplified approaches to obtain equally valid information for efficient qualification purposes. Based on these a realistic roadmap for CDM is more important than ever to insure safe ESD control methods are rigorously implemented in production areas. These questions beg if in future CDM should be specified in terms peak current rather than some voltage levels. In this talk first an overview of the changing CDM landscape with technology, package size, and circuit speed will be presented. Some of the modeling methods will be reviewed to give a perspective on the IC package design influence on achievable CDM performance. The currently simplified test methods in practice and proposals for further simplification using sampling of identical pins will also be presented. Finally, a roadmap for CDM into the next half of this decade will be projected.

Charvaka Duvvury was a Texas Instruments fellow while he worked in the Silicon Technology Development group. He is also a fellow of the IEEE. Charvaka received his PhD in engineering science from the University of Toledo and also worked as a post-doctoral fellow in physics at the University of Alberta in Canada. He has published over 150 papers in technical journals and conferences and holds more than 75 patents. He has co-authored books on ESD design, hot carriers, and modeling of electrical overstress. He is a recipient of the IEEE EDS Education Award (2013), Outstanding Contributions Award from the EOS/ESD Association (1990), and Outstanding Industry Liaison Award twice from the Semiconductor Research Council (1994 and 2012). He served twice as the General Chair for the ESD Symposium in 1994 and 2005. He was a contributing editor for the IEEE Transactions on Device and Materials Reliability (TDMR) from 2001-2011. He has been a member of the ESD Association board of directors since 1997. Charvaka is a co-founder and co-chair of the Industry Council on ESD Target Levels.

# SEMINARS

Seminar Chair: Brett Carn, Intel

We have 4 seminars this year, looking at today's and tomorrow's challenges in the ESD Industry. The first seminar covers ESD manufacturing risks in our wafer environment in which many material choices are not geared for ESD prevention. In this first seminar we will hear about ESDFOS (Electrostatic Discharge from Outside-to-Surface) in which an ESD event does not occur through the traditional pad entry points but through the wafers themselves. Introducing a risk that can sometimes be interpreted as other failure mechanisms. In our second seminar, we will hear about the very soon to be released joint ESDA/JEDEC CDM standard (JS-002-2014), the challenges with merging the previous two separate standards and how JS-002-2014 improves on the previous two standards. Our third seminar looks at breaking down the HBM and CDM waveforms which exist in our specifications today into simple 2 pole RLC circuit models and the practical applications of how this can be used to solve ESD problems. The final seminar will discuss the challenges we see today in our ESD, Latchup and EOS and discuss future developments, such as package size, multi-chip package and high power devices, and their impacts on ESD, latchup and EOS testing.

## Seminar 1

**ElectroStatic Discharge From Outside-to-Surface (ESDFOS)**

*Peter Jacob, EMPA*

Up to now the ESD protection understanding of many ESD experts is focused on antistatic floors, clothing, workplaces etc. However, in many cases, the process-machine's-internal risks are more or less neglected and neither controlled nor any useful machine-internal ESD protection has been done. In consequence, those process sequences, where wafers and non-molded dies are handled automatically with highly static materials as blue foils, water dusting, wafer transporting on framed blue foils, die pick&place, and other preassembly and assembly process steps frequently are at less attention with respect to ESD prevention. In case of ESD, the lightning strike usually doesn't enter through the pads into the device but directly through the wafer-respectively bare die-surface by hurting the surface passivation – ESDFOS (ElectroStatic Discharge From Outside-to-Surface). Underneath it, the discharge path continues via surface metal, top-2nd-metal etc. until it reaches the substrate. Thus, the ESD protection structures at the chip pads are useless, since they are bypassed. The damage signatures differ completely from what is commonly known as ESD damage and can be mixed up easily with other failure signatures.

The seminar starts with some experimental demos, which show the principles of the charge generation in such preassembly processes. Thereafter, the different ESDFOS failure signatures are presented and discussed, also, how to distinguish them from similar looking failure signatures from other root causes. The next chapter highlights specific process-tool-related risks and useful countermeasures. Finally, a brief introduction into the German guideline 1013 and into specific measurement techniques for localization of critical charging within process tools shall round up the seminar.

IEW 2014 Seminar Presentation

After studying Technical Physics in Munich, Peter Jacob started his professional work in 1981 as a failure analysis expert in IBM semiconductor plant Boeblingen until 1992. After a short period at Hitachi Scientific Instruments, where he was responsible for electron microscopy configurations and customer trainings, he joined ETH Zurich/ Empa as a senior expert for failure analysis on micro- and power-electronics from device to system level. In parallel to this work, in 1995 he joined to Swatch Group – EM Microelectronic Marin as a principal F/A engineer. Peter has authored more than 60 contributed and invited papers including an ESREF Best Paper. He volunteers in the German ESD Forum, EDFAS and EuFANet. In recognition of his annual lectures in scanning electron microscopy, he was appointed in 2007 to a Honorary Professor of Technical University Munich and in 2010 he received the International Barkhausen Award of Technical University Dresden.

## Seminar 2

**The New JS-002 ESDA/JEDEC Joint CDM Standard: Considerations and Improvements on Existing Standards**

*Alan Righter, Analog Devices*

The new ESDA/JEDEC Joint CDM Standard (JS-002) has been completed, which is a combined version of features of the ESDA and JEDEC test platforms, and introduces measurement and verification improvements over both previous ESDA and JEDEC CDM standards. This seminar describes differences in the ESDA and JEDEC methods, how they were resolved in the new JS-002 standard, and describes the issues and improvements from operational, theoretical, measurement, and instrumentation work which spurred the development of this new single CDM test platform for the new standard. Future work will also be described.

Alan Righter is the ESDA Co-chair (along with JEDEC Co-chair Terry Welsher) of the ESDA/JEDEC Standard Joint Working Group (JWG), responsible for development of the new Joint CDM standard. Alan has worked at Analog Devices, Wilmington, MA since 1997 and currently is a Senior Staff ESD Engineer responsible for ESD robustness of foundry manufactured products and active in customer ESD support. Alan earned a Ph.D. from the University of New Mexico in 1996 and previously worked at Sandia National Laboratories in Albuquerque, NM from 1984-1997. He is currently active on the ESD Association Board of Directors and is also the ESDA Secretary.

## Seminar 3

**Demystifying Measurements from HBM and CDM ESD Testers (How To Solve ESD Problems by Thinking in Pictures)**
*Timothy J. Maloney, Intel*

"Think in pictures" if at all possible, we are told, in order to achieve the highest level of comprehension of a scientific topic. Math leads to visualization, and visualization leads right back to math reasoning that is robust and self-checking. The tester waveform for Human Body Model (HBM) or Charged Device Model (CDM) ESD is itself a picture but understanding it, manipulating it, and characterizing it involve math concepts like integration and convolution—readily visualized—and finish with simple circuit models (more pictures) that describe what we see. At this point we are ready for analysis (take a measured waveform and extract the essential circuit elements) or synthesis (take a circuit model and generate waveforms, noting the effect of each element), and we can transition smoothly between time and frequency domains. We find that most HBM or CDM waveforms can be fit to a simple 2-pole RLC circuit model; the point to note is just that the lumped elements for HBM and CDM have very different values. Remarkably, the same methods apply to describing waveform measurements with frequency-limited oscilloscopes, a major issue with CDM, and how to adapt to that. This seminar will review the author's published work on these subjects from 2009 to the present (accessible as esd09.pdf to esd14.pdf at https://sites.google.com/site/esdpubs/documents), with an emphasis on how such visualization can help all of us to acquire insight into our data, and drive improved testing methods.

Timothy J. Maloney received an S.B. degree in physics from the Massachusetts Institute of Technology in 1971, an M.S. in physics from Cornell University in 1973, and a Ph.D. in electrical engineering from Cornell in 1976, where he was a National Science Foundation Fellow. He was a Postdoctoral Associate at Cornell until 1977, when he joined the Central Research Laboratory of Varian Associates, Palo Alto, CA. At Varian until 1984, he worked on III-V semiconductor photocathodes, solar cells and microwave devices, as well as silicon molecular beam epitaxy and MOS process technology. Since 1984 he has been with Intel Corp., Santa Clara, CA, where he has been concerned with integrated circuit ESD protection and testing, CMOS latchup, fab process reliability, signal integrity, system ESD testing including cable discharge, and design of ESD power clamp and diode cells. He is now a Senior Principal Engineer at Intel. He has received the Intel Achievement Award for his patented ESD protection devices, which have achieved breakthrough ESD performance enhancements for a wide variety of Intel products. He now holds thirty-seven patents, with several more pending. Dr. Maloney received Best Paper Awards for his contributions to the EOS/ESD Symposium in 1986 and 1990, was General Chairman for the 1992 EOS/ESD Symposium, and received the ESD Association's Outstanding Contributions Award in 1995. He has taught short courses at UCLA, University of Wisconsin, and UC Berkeley. He is co-author of a book, "Basic ESD and I/O Design" (Wiley, 1998), and is a Fellow of the IEEE. Tim Maloney was the subject of a Volunteer Spotlight column in the ESDA's Threshold newsletter, March/April 2010 (p. 6). It can be found in the online archives at http://www.esda.org/threshold_archives.cfm.

## Seminar 4

**Challenges and Future Developments in ESD/LU/EOS Testing**
*Marcos Hernandez, Tom Meuse, Thermo Fisher Scientific*

This seminar will discuss some of the possible pitfalls that standards bodies, tester manufacturers and the device industry may face as ESD, LU and EOS testing requirements continue into the future. Test requirements, like device and system designs are constantly changing! As new threats arise, this leads into investigations into their root cause, which leads into protection scheme development and of course verification / test methods need to be developed as well. Although device and system level ESD testing requirements are rather stable, they may be influenced by new technologies and failure scenarios. As package size (pin count), multi-dimensional packaging and higher power devices become the norm, Latch-up (LU) testing becomes increasingly more difficult and may require some new approaches in the way LU testing is performed. In addition to issues related with ESD and LU testing requirements, Electrical Overstress (EOS), which as it's "all" encompassing name indicates, may lead to new testing requirements and new challenges as well!!

Our hope is this seminar will lead to some new thinking and perhaps some lively discussions on the testing requirements for today' and tomorrow's electronics!

Marcos Hernandez is the Senior Manager of Technology for the ESD/EMC line of products at Thermo Scientific in Wilmington, MA. Thermo Scientific Fremont produces ESD test equipment for EMC, HBM, MM, CDM, TLP and Latch Up verification. A former member of the JEDEC JESD 14.1 Working group, and current member of the ESDA HBM/JEDEC joint working group, CDM and MM, before his position at Thermo Scientific he has worked at Oryx Instruments as senior systems engineer, PRI Automation as a engineering consultant and at Process Diagnostics in Sunnyvale CA as the Senior Systems Engineer for the production of Ion implanter optical monitors. Marcos was a full time Electronics Computer Technology and Semiconductor Manufacturing instructor at San Jose City College for nine years and received a BS degree in Chemical Engineering from the University of Guanajuato, Mexico.

Tom Meuse is the Applications/Product/Technology Manager for the ESD line of products at Thermo Fisher Scientific. Tom has worked on many of the Thermo Surge and ESD simulator designs, in both an engineering capacity and as the project manager on both system level and device level testers. Tom is a member of the ESD Association Device Testing (WG-5.0) committee and the JEDEC JC-14.1 Committee on Reliability Test Methods. He's also a member of the Joint ESDA/JEDEC Device Testing work group and a contributing member to the Industry Council on ESD Target Levels.

# DISCUSSION/SPECIAL INTEREST GROUPS

Discussion/Special Interest Groups Co-Chairs:
Michael Khazhinsky, Silicon Laboratories, Michael.Khazhinsky@silabs.com
Scott Ruth, Freescale Semiconductor, scott.ruth@freescale.com

The evening discussion groups are an integral part of the workshop. Two parallel discussion groups are offered each evening Monday through Wednesday. Each discussion group has one or more moderators with extensive expertise on the topic to help guide and inspire the discussion. The success of these sessions depends on your active participation. We encourage you to bring along data, ideas and other items of interest to share. Contacting session moderators with questions, comments or suggestions prior to the event is also encouraged. As the workshop approaches, please check the IEW web site for updates from the discussion group moderators. Interested in forming a new Special Interest Group (SIGs), focused on one compelling topic of mutual interest? Please contact Scott Ruth and Michael Khazhinsky (Scott.Ruth@freescale.com, Michael.Khazhinsky@silabs.com) for SIG creation details.

## Discussion Groups Session A

### DG A.1

**ElectroStatic Discharge From Outside-to-Surface (ESDFOS)**

Moderator: Peter Jacob, EMPA, (peter.jacob@empa.ch)

ESDFOS (ElectroStatic Discharge From Outside-to-Surface) means a specific surface-ESD event, which happens in most cases in the preassembly processes (between final wafer testing and capsulated device). ESDFOS events, happening in the waferfab, usually can be recognized and sorted out in the wafer test. If a severe process problem related to ESDFOS would happen in the wafer fab, the root cause can be identified rather simple, since the damage will be buried by the subsequent layers – thus allowing a clear correlation to the last process steps before it happened. However, after the wafer level final test, a long series of assembly processes start, where in-between no functional testing can be done and usually no further layer processing is applied to the wafer (except PI-passivation and RDL-processing in specific cases). The usual standard process sequence is frontside-taping/ backlapping/ framing/ frontside detaping/ wafer dicing/ post cleaning/ die-pick&place/ wire bonding/ packaging (molding) or MCM or COB… Most of these processes are automated and include high ESD risks due to missing useful internal ESD protection. For a useful protection within the machines, existing standards are hardly applicable, yet – but a guideline of the German ESD Forum e.V. (1013) is already available.

The discussion group is open for discussion of the following topics:

- ESDFOS failure diagnosis and how to distinguish from other, similar-looking failures
- Discussion of most critical process steps
- Discussion on process risk evaluations and charging measurement methodologies
- Introduction into the (German ESD Forum) guideline 1013 on the topic

### DG A.2

**ESD Compact Models**

Moderator: Michael Stockinger, Freescale Semiconductor, (M.Stockinger@freescale.com)

Device compact models have become an important prerequisite for on-chip ESD event simulations. Due to the ever shrinking ESD design window and increased complexity of ESD protection networks, designing ESD protection solely on TLP device data and back-of-the-envelope calculations has become a thing of the past. Standard device models supplied by technology design kits usually fail to work in the high-current ESD regime. Every ESD engineer has likely dealt with dedicated ESD compact models of some sort – from simple diode models to more complex MOSFET snapback and SCR models. Shy of any standardization, there appear to be many different types of ESD models in use – empirical vs. physical, static vs. dynamic, piece-wise-linear vs. fully differentiable, etc. ESD designers are often challenged to create their own compact models, which may have led to a large variety of different ESD models for similar devices. This discussion group will survey what ESD compact models are currently out there. Your participation will be key to capturing as large a cross-section of models as possible. One goal is to summarize the existing variety of models and to categorize them based on certain aspects of the models. This should ultimately lead to a technical report issued by the ESDA.

# Discussion Groups Session B

## DG B.1

**Latch-up for Special Pin Types**

Moderator: Robert Lunifeld, Intel, (robert.g.lunifeld@intel.com)

Semiconductors have seen a proliferation of pin types that do not clearly fit into the power supply (overvoltage test) or Input/Output (I-test) categories. What latch-up test type should be used for these special pin types? There are also a number of categories of static pin types that require special consideration. Is risk low enough to omit latch-up testing? Can testing be relaxed? Internal voltage regulators have also added complexity to latch-up testing. In what mode should testing be conducted? Should alternate methods of observing latch-up be considered? The JESD 78 team is looking to provide more comprehensive guidance in this area in an upcoming version of the standard.

## DG B.2

**3D IC**

Moderator: Dimitri Linten, imec, (linten@imec.be)

2.5 & 3D ICs are rapidly becoming a reality in today's semiconductor world. In these technologies, Through Silicon VIA's (TSV) are used to connect different design modules and chips within the same package. All potential ESD threats have been heavily discussed over the last years, but only recently it starts to be described in the open literature (two presentations at this event). Since 2014, the GSA (Global Semiconductor Alliance) and ESDA teamed up to compiling a white paper on the topic, providing an initial guideline to the industry. In this discussion group we would like to discuss the white paper and explore how we can move this topic forward.

Please contact the moderator in order to receive the white paper draft prior to the event.

# Discussion/Special Interest Groups Session C

## SIG C.1

**ESD Foundry Parameters and ESD IP**

Moderator: Harald Gossner, Intel, (harald.gossner@intel.com)

The ESDA working group on ESD Foundry parameters has successfully finalized a Technical Report on the required ESD technology parameters required from a foundry technology (TR22). The most efficient application of the recommendations is planned to be discussed with foundry representatives. In the next step work has been started on the models and rules which will be specified by IP suppliers towards IC level ESD integration to guarantee first time design accuracy. An industry survey has been done and the results are going to be highlighted in the discussion group scheduled during IEW. Also a first proposal of essential rules and models will be presented for feedback. Join the discussion group and bring your own experience with IP module integration to the team.

## DG C.2

**Forward Looking Considerations in ESD Testing**

Moderator: Terry Welsher, Dangelmayer Associates, (terry@dangelamyer.com)

In recent years significant changes have been made to the HBM test method which have addressed a number of issues including reducing false failures due to cumulative effects and reduction in test time. Some rational methods for sampling i/o pins have also been introduced. Even with all of these improvements, HBM remains as a significant burden for device qualification and determination of relative HBM robustness. With the extensive effort put into HBM testing, it is useful to explore whether the threshold as currently defined (highest known passing level of the single weakest pin) is a good metric, particularly for high pin count devices. In this DG, we will explore alternate means of collecting and reporting ESD threshold information which are better indicators of risk. We will also discuss how to present ESD data to customers in a rational way in data sheets or reliability reports. Some of this will apply to CDM as well. Finally, we will also entertain discussions about the future of HBM testing. Why do we still need it? Or do we?

IEW 2014 Discussion Group

# TECHNICAL SESSIONS

Technical Session Chair: Ann Concannon, Texas Instruments

This year's IEW technical program consists of two sessions, where peer-reviewed poster presentations are discussed together with the authors and interested colleagues. The authors will introduce their work in a short podium "teaser" presentation prior to the extended interactive discussion with the workshop participants at the posters. This format allows an in-depth exchange of ideas among a diverse audience, in a very informal setting. A wide variety of ESD subjects will be covered: the first session will concentrate on IC level ESD issues, from design, ESD & Latch-up CAD verification flows and also characterization techniques in the ESD time domain. The second session will cover system level ESD considerations; with both onchip and external ESD protection concepts reviewed. In addition to system level ESD, several posters consider the challenges of integrating multichip together with passives in MCM-like mini-systems.

## Technical Session A: IC ESD Design, Verification, and Test

### A.1 25 Ohm Contact CDM – A Reproducible Alternative to FICDM

*Nathan Jack, Timothy Maloney, Intel*

The objective of this work is to develop a CDM tester that reproducibly delivers current waveforms that preserve the essential characteristics of the JEDEC field-induced CDM tester (FICDM). As CDM qualification levels decrease to meet scaling and circuit performance demands, the variation inherent to the air spark discharge of the JEDEC FICDM tester will increase from inconvenient to intolerable. Previously identified problems with relay-based CDM testers are addressed with a relay-based contact CDM tester having a 25 ohm discharge impedance and controllable rise time. By removing zap-to-zap variation, unnecessary margin and test effort can be removed from the ESD design process.

### A.2 Defect Characterization after ESD Stress: Merging TLP and Pulsed IV Techniques

*Dimitri Linten, R. Boschke, G. Hellings, S. H. Chen, M. Scholz, A. Alian, imec; Z. Ji, imec and Liverpool John Moores University*

In R&D devices using new materials are studied for intrinsic ESD reliability, e.g. planar InGaAs. Study of the TLP IV shape can give information about device degradation and walkout, which can be attributed to charging of traps during the TLP pulse. Standard TLP does not provide enough insight, hence the TLP is extended towards a more general Pulsed IV setup using 3 probes instead of the standard two probes. Using the new setup, two kind of defects are identified for the InGaAs example. The origin and location can be linked back to the material properties. The proposed integrated PIV system in TLP enables to model the full TLP IV graph.

### A.3 High Leakage Issue for Dual-Time-Constant ESD Clamp during Slow Power-up Corner Simulation

*Jian Liu, Nate Peachey, Qorvo (RF Micro Devices)*

This work reports the design and optimization for a novel dual-time-constant (dual-TC) ESD clamp, as well as simulation and measurement results. Compared with the traditional "BigFET" ESD clamp, the dual-TC ESD clamp has the advantage of only responding to the fast ESD transient pulses while keeping off to slow non-ESD pulses, leading to a short circuit start-up time during circuit normal power up. Moreover, it is also able to shut off the clamp after the circuit is powered up, providing latch-up immunity to the transients on the power supply during normal circuit operation.

### A.4 ESD IP Explorer: A Tool for ESD Network Verification at Chip Scale

*Benjamin Viale, STMicroelectronics, Ampère lab; Mathieu Fer, Jean-Daniel Lise, Lionel Courau, Alexandre Dray, Philippe Galy, STMicroelectronics; Bruno Allard, Ampère lab*

The need for denser, faster, and less power consuming products has been guiding IC design strategy choices. To increase chip performances and density, using chip scale packaging techniques, wirebonds are replaced with bumps, vertically accessing highest metal levels. Bumps with direct access to the core power grid require the use of stand-alone core ESD protections. Therefore, the ESD network is now disseminated across the entire IC. Full-chip ESD verification is a key point for IC reliability and must absolutely accommodate these changes. Commercial and in-house tools are used to verify the core part. However, it is not possible to evaluate chip overall ESD robustness by only verifying distinct parts of the ESD network separately. A novel tool for ESD verification at chip scale based mainly on graph theory is proposed: ESD IP Explorer.

### A.5 RMAP – Software for Resistance Verification of Power Nets and ESD Protection Structures

*Maxim Ershov, Meruzhan Cadjan, Silicon Frontline Technology; Thomas Jochum, Intersil*

The objective of this paper is to present a new software tool and methodology for automated resistance verification of power nets and ESD protection structures. RMAP calculates resistance from the pads to all points on a net, and presents the results as color plots, enabling quick interactive visual inspection and verification.

### A.6 Latch-up Verification/Rule Checking Throughout Circuit Design Flow

*Michael Khazhinsky, Silicon Labs; John Scott, Peter Michelson, Mentor Graphics*

The verification of latch-up protection networks in modern integrated circuits is a difficult challenge. Traditional latch-up geometrical rule checks using DRC tools can only provide limited verification. While DRC checks are still useful at early design stages, relying on conventional DRC latch-up checking exclusively, poses a significant risk of missing hidden latch-up pitfalls. In this work we review a typical latch-up prevention flow and then compare to the dual DRC and PERC-based latch-up verification flow. We will provide an example of identifying latch-up injectors using EXT marker layer and describe how it could be used in both a DRC and PERC based verification flow. Additional examples of latch-up verification case studies related to hot pwells, guard rings and well ties will be analyzed.

# Technical Session B: Multichip and System Level ESD

### B.1 ESD Protection Design in Smart Interposer

*M. Scholz, G. Hellings, D. Linten, M. Detalle, A. La Manna, G. Van Der Plaats, E. Beyne, imec*

3D integration like wafer to die and die to die stacking are an option for the integration of different functionality like power management, logic and memory in one system-in-package. Passive silicon interposer are currently the most promising technology to provide the interconnects for the connection of stacked dies with each other and also to the package substrate and package pins. We will introduce the concept of smart interposer: a low-cost front-end of line processing is added to a passive interposer technology. This enables additional functionality like ESD protection design, design for testing and MiM capacitors.

### B.2 IEC and DPI Design Tradeoff for Automotive LIN

*Yue Zu, Akram Salman, Anand Gopalan, Ann Concannon, Texas Instruments*

Automotive LIN bus has a requirement to robustly withstand injected RF disturbances (DPI, Direct Power Injection) from 1M Hz to 1G Hz at different power levels such that the communication is not effected. With certain source impedance, this translates to an AC signal of the injected frequency on the LIN bus. Transient turn on of the ESD cell during DPI can cause the impedance of the ESD discharge path to drop so that the voltage on LIN bus collapses and fail DPI. The competing mechanisms of DPI immunity and IEC 61000-4-2 immunity result in a diminished design window. In this presentation, the design window required to satisfy both IEC and DPI requirements of the LIN IP is defined using SPICE simulation and silicon experiments.

### B.3 Comparison Analysis for ESD, EOS and HMM Immunity with ESD Protection Scheme Differences

*Han-Gu Kim, Jae-Hyok Ko, Sungpil Jang, Minchang Ko, Kyoungki Jeon, Samsung*

The purpose of this paper is to find the best solution for ESD scheme with the strong immunity in ESD, EOS and HMM. Comparison analysis for ESD, EOS and HMM test results with different ESD protection schemes is presented. The TLP measurement is evaluated for each of the devices that are included in ESD protection scheme. The immunity for each ESD protection schemes is evaluated by ESD, EOS, and HMM. According to our analysis until now, some split items are strongly affected by rising and duration time of ESD, EOS, and HMM.

### B.4 Capacitor Effect on EOS Immunity

*Jae-Hyok Ko, Han-GuKim,Sang-Yong Cho, Jin Heo, Jong-KyuSong, Samsung*

This work investigated the effect of different kinds of capacitors on the EOS immunity level of the semiconductor ESD protection device. Measurement results can provide an understanding of the gap between system-level EOS and component-level EOS. Based on these results, there is a need to think carefully about the improvement methodology for the System (or board) Efficient EOS Design.

### B.5 Basic Design Considerations for High Speed Data Line TVS Protection

*Jordan Davis, ON Semiconductor*

As the data speeds of varying interfaces has increased into the megabit and gigabit regimes, considerations involved in designing discrete TVS protection parts for these interfaces have become more complex than simply designing to meet a survival specification. In this poster presentation, the key parameters will be review in the design process for high speed TVS protection parts. In addition, three potential architectures will be reviewed. The two parameters that have emerged as key for protecting these interfaces are capacitance and clamping voltage. Capacitance budget directly relates to the amount of allowable TVS protection as well as to the impact on signal integrity. While clamping voltage relates to the amount of stress the device under protection experiences. The balance of these becomes challenging as the data speed increases and the geometry of integrated circuits decreases.

### B.6 2.5D Interposer FPGA: ESD Protection for Die-to-Die IOs

*James Karp, Mohammed Fakhruddin, Michael Hart, Phoumra Tan, Dean Tsaggaris, Vassili Kireev, Xilinx Inc.*

ESD protection for die-to-die IO discussed for 2.5D interposer FPGA, including ESD specification, ESD elements footprint, and qualification methodology. S20.20 ESD standard describes the interposer assembly environment and sets 100V HBM specification with no reference to CDM. For 50,000 die-to-die IOs per FPGA, ESD elements must be size-optimized to alleviate ESD related silicon cost. 20nm test-chip for die-to-die IOs demonstrates “self-protecting” diode ESD solution that passes 120V HBM and 20-25V CDM. HBM & CDM results are shown to scale together and correlate to size of ESD elements. Small voltage CDM has peak current variations due to un-sustained arc.

# SCHEDULE

## Sunday, May 3, 2015

| | |
|---|---|
| 1:30 PM-4:00 PM | Registration: Pick up badges and handouts. |
| 4:00 PM-4:30 PM | Hotel check-in: Get room assignment & room key. |
| 12:00 PM-1:30 PM | Lunch |
| 1:30 PM-4:30 PM | Free Time |
| 4:30 PM-6:00 PM | Hosted Reception |
| 6:00 PM-7:30 PM | Dinner |
| 7:30 PM-8:30 PM | Welcome/Entertainment **Lake Tahoe: Stories, Facts & Fun** *Mark McLaughlin* |
| 8:30 PM-9:30 PM | Networking/Social Gathering |

## Monday, May 4, 2015

| | |
|---|---|
| 7:30 AM-9:00 AM | Breakfast |
| 9:00 AM-9:30 AM | Welcome |
| 9:30 AM-10:40 AM | **Keynote: A Perspective on Transistor Architectures - Bulk and SOI, Planar and FinFETs - for 28nm to 7nm Generations** *Terence B. Hook, IBM* |
| 10:40 AM-10:50 AM | Break |
| 10:50 AM-12:20 PM | **Seminar 1: ElectroStatic Discharge From Outside-to-Surface (ESDFOS)** *Peter Jacob, EMPA* |
| 12:20 PM-1:50 PM | Lunch |
| 1:50 PM-2:50 PM | **Invited Talk 1: ESD Challenges Along the Technology Scaling Roadmap** *Dimitri Linten, imec* |
| 2:50 PM-3:35 PM | **Technical Session A:**<br>**A.1 25 Ohm Contact CDM – A Reproducible Alternative to FICDM**<br>Nathan Jack, Timothy Maloney, Intel<br>**A.2 Defect Characterization after ESD Stress: Merging TLP and Pulsed-IV Techniques**<br>Dimitri Linten, R. Boschke, G. Hellings, S. H. Chen, M. Scholz, A. Alian, imec; Z. Ji, imec and Liverpool John Moores University<br>**A.3 High Leakage Issue for Dual-Time-Constant ESD Clamp during Slow Power-up Corner Simulation**<br>Jian Liu, Nate Peachey, Qorvo (RF Micro Devices)<br>**A.4 ESD IP Explorer: A Tool for ESD Network Verification at Chip Scale**<br>Benjamin Viale, STMicroelectronics, Ampère lab; Mathieu Fer, Jean-Daniel Lise, Lionel Courau, Alexandre Dray, Philippe Galy, STMicroelectronics; Bruno Allard, Ampère lab<br>**A.5 RMAP – Software for Resistance Verification of Power Nets and ESD Protection Structures**<br>Maxim Ershov, Meruzhan Cadjan, Silicon Frontline Technology; Thomas Jochum, Intersil<br>**A.6 Latch-up Verification/Rule Checking Throughout Circuit Design Flow**<br>Michael Khazhinsky, Silicon Labs; John Scott, Peter Michelson, Mentor Graphics |
| 3:35 PM-4:50 PM | **Poster Discussion Session A** |
| 4:50 PM-6:10 PM | **Seminar 2: The New JS-002 ESDA/JEDEC Joint CDM Standard: Considerations and Improvements on Existing Standards** *Alan Righter, Analog Devices* |
| 6:10 PM-7:30 PM | Dinner |
| 7:30 PM-8:30 PM | **Discussion Group Session A: Parallel Groups**<br>DG A.1 - ElectroStatic Discharge From Outside-to-Surface (ESDFOS)<br>DG A.2 - ESD Compact Models |
| 8:30 PM-9:30 PM | Networking/Social Gathering |

## Tuesday, May 5, 2015

| | |
|---|---|
| 7:30 AM-9:00 AM | Breakfast |
| 9:00 AM-9:10 AM | Announcements |
| 9:10 AM-10:30 AM | **Seminar 3: Demystifying Measurements from HBM and CDM ESD Testers (How To Solve ESD Problems by Thinking in Pictures)** *Timothy J. Maloney, Intel* |
| 10:30 AM-10:40 AM | Break |
| 10:40 AM-11:40 AM | **Invited Talk 2: Physical Verification and ESD Robustness Check** *Ertugrul Demircan, Freescale Semiconductor* |
| 11:40 AM-12:20 PM | Report on DG Sessions A |
| 12:20 PM-1:50 PM | Lunch |
| 1:50 PM-6:00 PM | Open Time |
| 6:00 PM-7:30 PM | Dinner |
| 7:30 PM-8:30 PM | **Discussion Group Session B: Parallel Groups**<br>DG B.1 - Latch-up for Special Pin Types<br>DG B.2 - 3D IC |
| 8:30 PM-9:30 PM | Networking/Social Gathering |

## Wednesday, May 6, 2015

| | |
|---|---|
| 7:30 AM-9:00 AM | Breakfast |
| 9:00 AM-9:10 AM | Announcements |
| 9:10 AM-10:10 AM | **Invited Talk 3: ESD Challenges in Power Management IC Design** *Ann Concannon, Texas Instruments* |
| 10:10 AM-10:20 AM | Break |
| 10:20 AM-11:40 AM | **Seminar 4: Challenges and Future Developments in ESD/LU/EOS Testing** *Marcos Hernandez, Tom Meuse, Thermo Fisher Scientific* |
| 11:40 AM-12:20 PM | Report on DG Sessions B |
| 12:20 PM-1:50 PM | Lunch |
| 1:50 PM-2:50 PM | **Invited Talk 4: Verification Tools for ESD Protection Engineering** *Michael Khazhinsky, Silicon Laboratories; Hans Kunz, Texas Instruments* |
| 2:50 PM-3:15 PM | Picture / Break |
| 3:15 PM-4:00 PM | **Technical Session B:**<br>**B.1 ESD Protection Design in Smart Interposer**<br>M. Scholz, G. Hellings, D. Linten, M. Detalle, A. La Manna, G. Van Der Plaats, E. Beyne, imec<br>**B.2 IEC and DPI Design Tradeoff for Automotive LIN**<br>Yue Zu, Akram Salman, Anand Gopalan, Ann Concannon, Texas Instruments<br>**B.3 Comparison Analysis for ESD, EOS, and HMM Immunity with ESD Protection Scheme Differences**<br>Han-Gu Kim, Jae-Hyok Ko, Sungpil Jang, Minchang Ko, Kyoungki Jeon, Samsung<br>**B.4 Capacitor Effect on EOS Immunity**<br>Jae-Hyok Ko, Han-GuKim,Sang-Yong Cho, Jin Heo, Jong-KyuSong, Samsung<br>**B.5 Basic Design Considerations for High Speed Data Line TVS Protection**<br>Jordan Davis, ON Semiconductor<br>**B.6 2.5D Interposer FPGA: ESD Protection for Die-to-Die IOs**<br>James Karp, Mohammed Fakhruddin, Michael Hart, Phoumra Tan, Dean Tsaggaris, Vassili Kireev, Xilinx Inc. |

## Wednesday, May 6, 2015 continued

| | |
|---|---|
| 4:00 PM-5:15 PM | **Poster Discussion Session B** |
| 5:15 PM-6:15 PM | **Invited Talk 5: CDM Qualification: Technology Impact, Testing Nuances, and Target Levels** *Charvaka Duvvury, ESD Consulting* |
| 6:15 PM-7:30 PM | Dinner |
| 7:30 PM-8:30 PM | **Discussion/Special Interest Group Session C: Parallel Groups**<br>SIG C.1 - ESD Foundry Parameters and ESD IP<br>DG C.2 - Forward Looking Considerations in ESD Testing |
| 8:30 PM-9:30 PM | Hosted Reception |

## Thursday, May 7, 2015

| | |
|---|---|
| 7:30 AM-9:00 AM | Breakfast |
| 9:00 AM-9:10 AM | Announcements |
| 9:10 AM-9:40 AM | Industry Council Report |
| 9:40 AM-10:20 PM | Report on DG/SIG Sessions C |
| 10:20 AM-10:35 AM | 2016 Announcements and Closing |
| By 11:00 AM | **Hotel Check-Out** |

IEW 2014 group photo, Grand Hotel de Paris, Villard de Lans, France

# TRAVEL ARRANGEMENTS & ACCOMMODATIONS

Granlibakken Conference Center and Lodge, located in beautiful Lake Tahoe, provides an opportunity to meet in a relaxed, invigorating atmosphere. From the lodging to the activities, you'll see that our multi-functional retreat conference center and resort has what it takes to be that perfect Lake Tahoe destination.

## IEW ACCOMMODATIONS:

At Granlibakken we have a wide variety of Lake Tahoe lodging options, from bedrooms, studios and suites to one to eight bedroom townhouses, each decorated to complement the resort's natural Tahoe City setting.

Each room features the following amenities:

- Cable television with DVD
- Direct dial phone with voicemail and LAN / WLAN internet access
- In-room coffee maker
- In-room fan
- Complimentary parking

All rooms come with our resort amenities which include an outdoor heated pool, outdoor hot tub, indoor sauna, hiking and biking trails, tennis courts and gym. On property Day Spa, Treetop Adventure Park, bike rentals and a ski & sledding hill are available for additional fees.

## GUESTS AND SPOUSES:

You are welcome to bring a guest to IEW. Accommodations are available for spouses and guests in the same room for an extra $300 US dollars per person. Guest fees are payable to ESDA. Guests will be charged for full stay, no partial stay allowed. Attendees must list guests with their initial registration to allow for room arrangements. For accommodations including children please contact ESDA for more information.

● Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 1-315-339-6937.

## RESPONSIBILITIES OF ATTENDEES:

Please come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees. Enjoy IEW!

In keeping with the relaxed and informal atmosphere of the Workshop, we ask that attendees not overtly solicit, promote, or attempt to sell a commercial product or service at the Granlibakken Conference Center and Lodge. On the other hand, we strongly encourage making business acquaintances and arranging meetings to be held after the workshop.

## ON-SITE GUEST ACTIVITIES:

- Walking to Tahoe City or the Truckee River along our forest path (1.4 miles)
- Playing a game of tennis on one of the resort's five courts
- Taking in the surrounding beauty on our private nature trail
- Enjoying the sun beside our luxurious pool and hot tub area
- Relaxing in our rejuvenating sauna
- Building up a sweat on our outdoor par course
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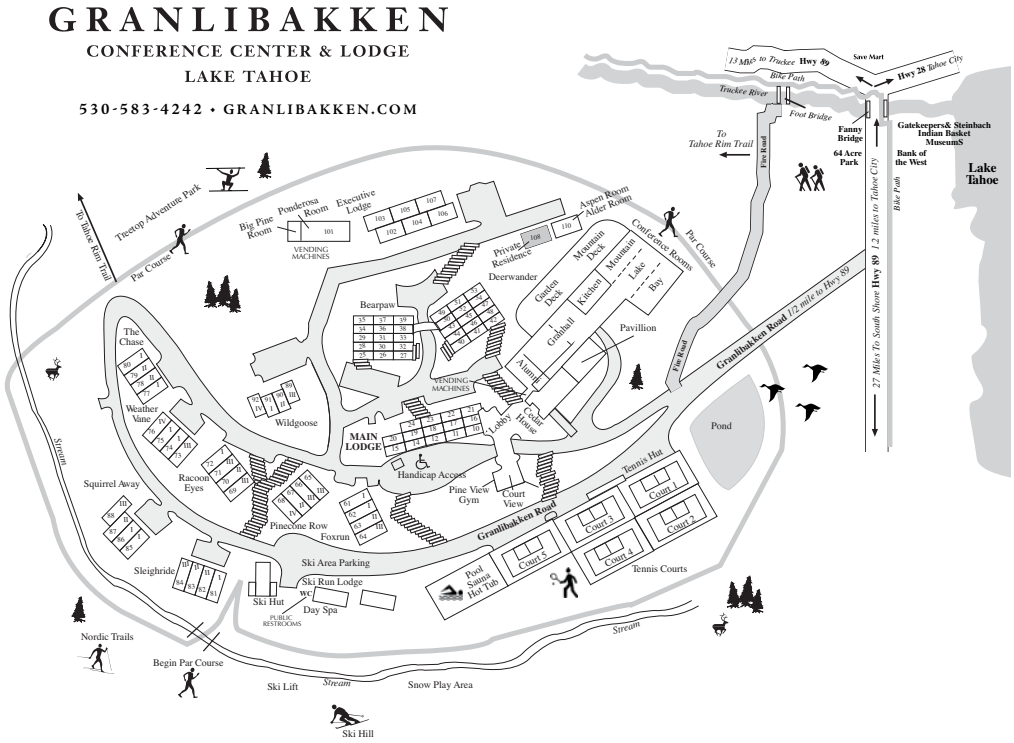
- Treetop ropes course and tours in our Adventure Park
- Mountain bike rentals available on property, provided by West Shore Sports





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Granlibakken offers airport shuttle service from and to the Reno/Tahoe International Airport for $98/person (single rider) or $49/person (2 + passengers). Guests wishing to book the shuttle should call (800) 543-3221 seven days or more in advance. The airport shuttle is by reservation only.

## BY CAR

### FROM SACRAMENTO (100 MILES)

Take Interstate 80 East toward Reno/North Lake Tahoe. Take Exit 185 for State Highway 89S at the traffic circle. Take the first exit onto CA-89 S. Drive 15 miles to Tahoe City, CA. As you enter Tahoe City, before the stop light in Tahoe City, bear to your right and continue on 89 South one-half mile to Granlibakken Road. Turn right. Drive one-half mile to Granlibakken Registration Desk located at the Porte Cochere at the main entrance.

### FROM SOUTHERN CALIFORNIA

Take I-405 North toward Sacramento. Continue on I-5N. Take exit 522 to merge onto I-80 E toward Reno. Follow directions listed above from Sacramento to North Lake Tahoe/Granlibakken.

### ALTERNATE FROM SOUTHERN CALIFORNIA

Take I-5N to 14 N exit toward Lancaster/Palmdale. Turn right on CA-14 and take slight left at US 395 to Highway 495 to East 14 to US 395 N. Continue to follow US-395 entering Nevada. Turn left at US-50. Turn right at NV-28 entering California. Continue on CA-28/North Lake Blvd to Tahoe City. Turn left at the stop light in Tahoe City onto CA-89 S. Drive one-half mile to Granlibakken Road and turn right. Drive one-half mile to Granlibakken Registration Desk located at the Porte Cochere at the main entrance.

### FROM RENO/TAHOE INTERNATIONAL AIRPORT (54 MILES)

Take Highway 395 North on-ramp from the Airport to I-80 West/Sacramento to Exit 185 (Truckee) to CA-89 S to Tahoe City. Follow directions listed above from Sacramento to North Lake Tahoe/Granlibakken.

# International ESD Workshop Registration

**May 3-7, 2015 Granlibakken Conference Center & Lodge Lake Tahoe, CA**

**Workshop registration includes a room reservation and provided meals**

## Register Online at http://esda.org/onlineregistrations.html

## Registration Fee $2,195

### Discount before March 20th: members $1,795 / non-members $1,995

The registration fee includes full workshop attendance and handout materials, four nights' lodging (Sun-Wed), plus 12 meals (Sunday Lunch-Thursday Breakfast), as well as morning and afternoon breaks.

Cancellation & refund requests will be considered if received in writing no later than March 20th 2015, and are subject to a $50 fee. Any other approved dispositions will also be assessed a $50 fee.

Register 5 or more people from one company at the same time and save $100 per person
Please contact the ESD Association prior to registering.

Students wishing to apply for reduced registration Please contact the ESD Association prior to registering.

IEW 2014 attendees enjoying free time and networking.

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# International ESD Workshop Registration Form

**May 3-7, 2015 Granlibakken Conference Center & Lodge Lake Tahoe, CA**

**Workshop registration includes a room reservation and provided meals**

Attendee: _____

Company: _____

Address: _____

City: _____ State: _____ Zip: _____ Country: _____

Phone: (  ) _____ E-mail: _____ Fax: (  ) _____

Address is: *(Please check one)* ☐ home or ☐ office

☐ Please check here if you would like a printed set of notes. ☐ Check if, under the Americans with Disabilities Act, you require any auxiliary aids or services.

•Please List Your Guests: Adults (Name) _____

Guests staying in the room of a registered attendee will be charged $300 US dollars per person. Guest fees are payable to ESDA. Guests will be charged for full stay, no partial stay allowed. For accomodations including children please contact ESDA for more information.

•Please indicate any special dietary needs. _____

Arrival: Date _____ Time _____ • Departure: Date _____ Time _____

## Registration Fee $2,195

**Discount before March 20th: members $1,795 / non-members $1,995**

The registration fee includes full workshop attendance and handout materials, four nights' lodging (Sun-Wed), plus 12 meals (Sunday Lunch-Thursday Breakfast), as well as morning and afternoon snacks and drinks.

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- Register 5 or more people from one company at the same time and save $100 per person. Please contact the ESD Association prior to registering.

## Method of Payment

☐ Check Only U.S. currency, checks drawn on a U.S. bank that is a member of the U.S. Federal Reserve will be accepted.

Credit Card *(check one)* ☐ AMEX® ☐ Visa® ☐ MasterCard® ☐ Discover®

Card Number: _____

Exp. Date: _____ Security Code: _____

**Total Enclosed** $ _____

**Make checks payable to: ESD Association**
**Purchase orders not accepted for registration**

Name on Card: _____ Signature: _____

Billing Address: _____

## Discussion/Special Interest Groups

I am interested in the following discussion/Special Interest group(s)

| Choose one from group A | Choose one from group B | Choose one from group C |
|---|---|---|
| ☐ DG A.1 | ☐ DG B.1 | ☐ SiG C.1 |
| ☐ DG A.2 | ☐ DG B.2 | ☐ DG C.2 |

## Posters

Will you be bringing a poster to the open poster session? ☐ Yes ☐ No

If yes, what is the title of your poster? _____

## Special Interest Groups

Would you like to form a new SIG? ☐ Yes ☐ No

If yes, what is the proposed topic for your group? _____

# IEW 2016

## International Electrostatic Discharge Workshop

# Save the date:

# IEW
# May 16-19, 2016
# Evangelische Akademie
# Tutzing, Germany

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