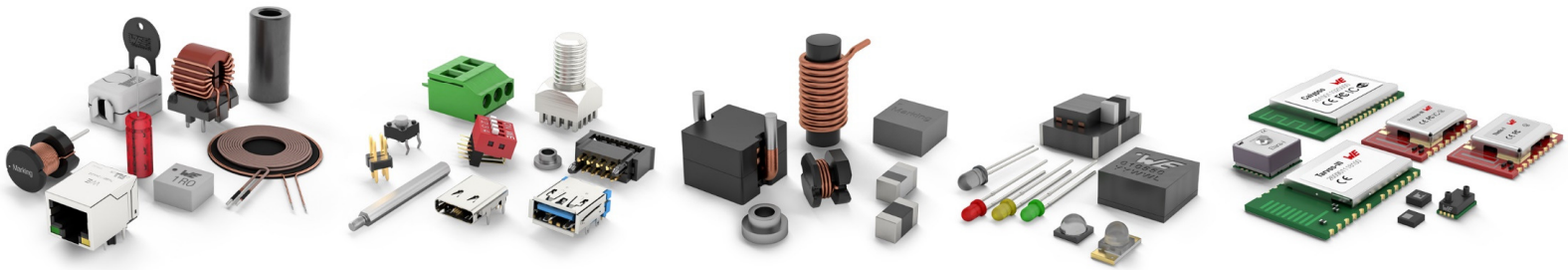


EMC DESIGN TIPS

Raf Vleugels
FAE

de Nederlandse EMC-ESD Vereniging

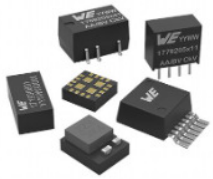
EMC-ESD Event 2023

Hotel van der Valk Vianen

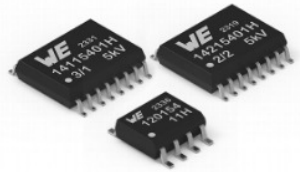
Dinsdag 21 november

PASSIVE COMPONENTS

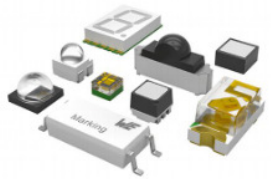
POWER MODULES (MAGI³C SERIES)



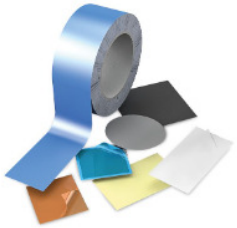
DIGITAL ISOLATORS



OPTOELECTRONICS

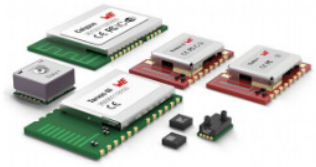


THERMAL MANAGEMENT



ELECTROMECHANICAL COMPONENTS

WIRELESS CONNECTIVITY & SENSORS



AUTOMOTIVE

WÜRTH ELEKTRONIK
MORE THAN YOU EXPECT

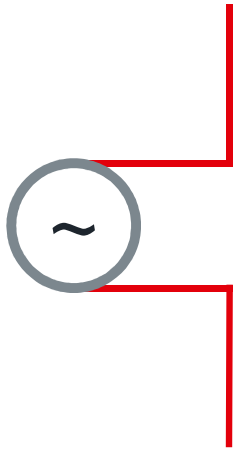
EMC-ESD Event 2023

Agenda

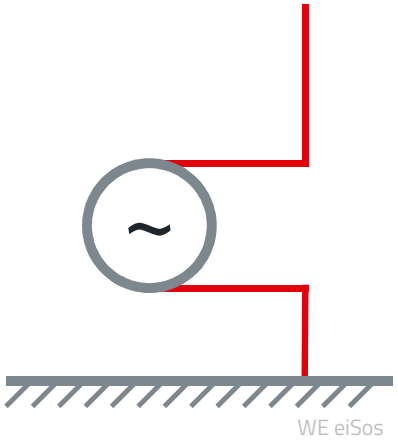
- Coupling paths
- Filter Placement
- Layout Considerations
  - Power Inductors
  - Overvoltage Protection
- Summary
- Q&A

COUPLING PATHS

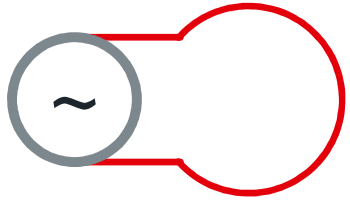
Everything is an antenna



Electric Dipole Antenna



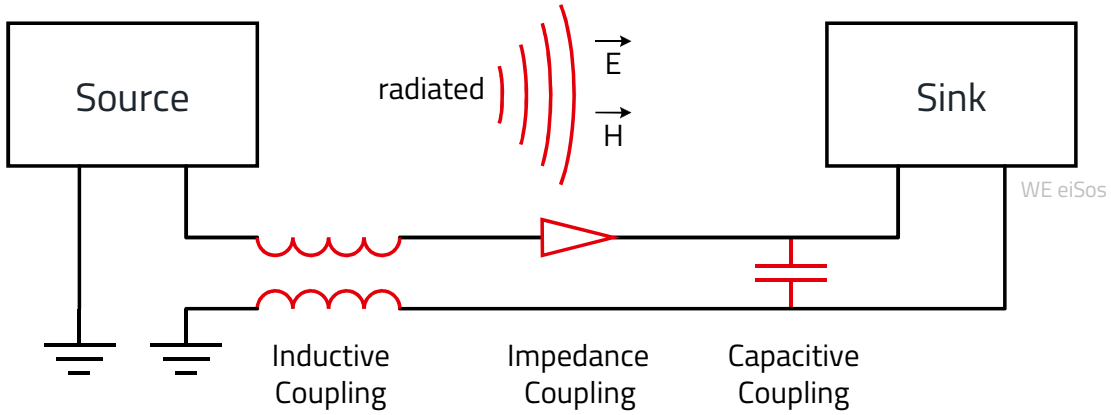
Electric Monopole Antenna



Magnetic Loop Antenna

Reducing EMI

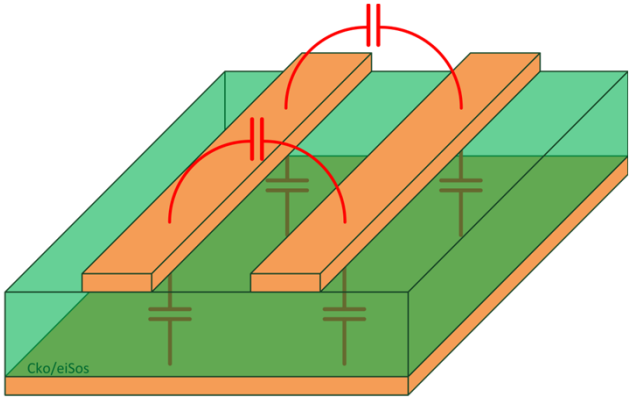
- Sufficient EMC can be achieved by suited measures at the noise source, coupling path or sink.
  - **Primary Measure** Reduce emission from noise source
  - **Secondary Measure** Break coupling paths
  - **Tertiary Measure** Increase immunity of the sink



Capacitive Coupling

Origins

- Originates from high dU/dt
- Parallel conductors form a parasitic capacitance
- Coupling capacitance is directly proportional to the length of the parallel trace run



Isolating Components	typ. Coupling Capacitance
Optocoupler	1 ~ 5pF
Solid State Relay	5 ~ 10pF
Electromechanical Relay	10 ~ 100pF
Transformers in SMPS	Up to 1000 pF

Capacitive Coupling

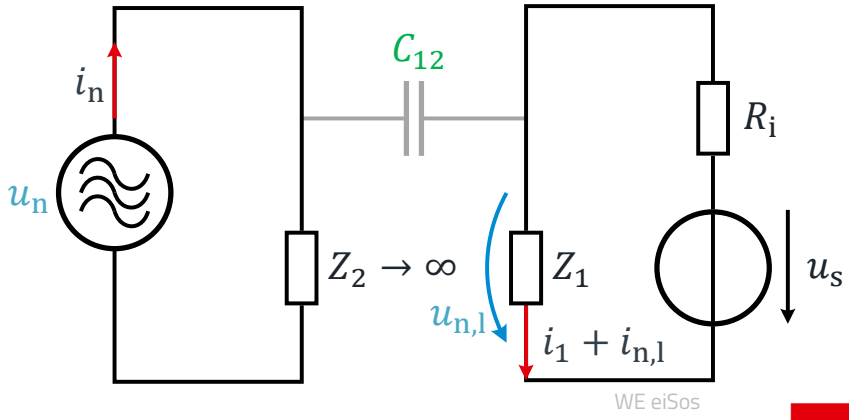
Effects

- Dominant, if structure dimensions are smaller than 10% wavelength of the exciting electric field (< λ/10).
  - Why λ/10? → Harmonics

- Voltage interference at the load:

$$u_{n,l} = i_n \cdot \frac{R_i \cdot Z_1}{R_i + Z_1} = C_{12} \cdot \frac{du_n}{dt} \cdot \frac{R_i \cdot Z_1}{R_i + Z_1}$$

$$C_{12} = \varepsilon * \frac{A}{d}$$



Capacitive Coupling

Measures to decrease coupling

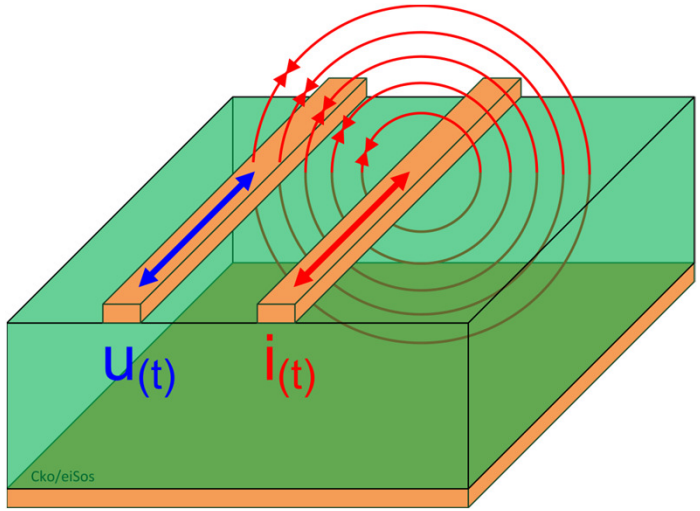
- **Primary Measure**
  - Decrease dV/dt by selecting a slower signal edges
  - A Low pass filter to take off the edges

- **Secondary Measure**
  - Shorten/avoid parallel trace runs
  - Small areas for switched polygons (e.g. DC/DC switch node)
  - Increase distance between affected paths
  - Electrical shielding (Cable, PCB, Housing)

Inductive Coupling

Origins

- Originates from high dI/dt
- Parallel traces form a parasitic transformer
- Mutual Inductance increases with shorter distance



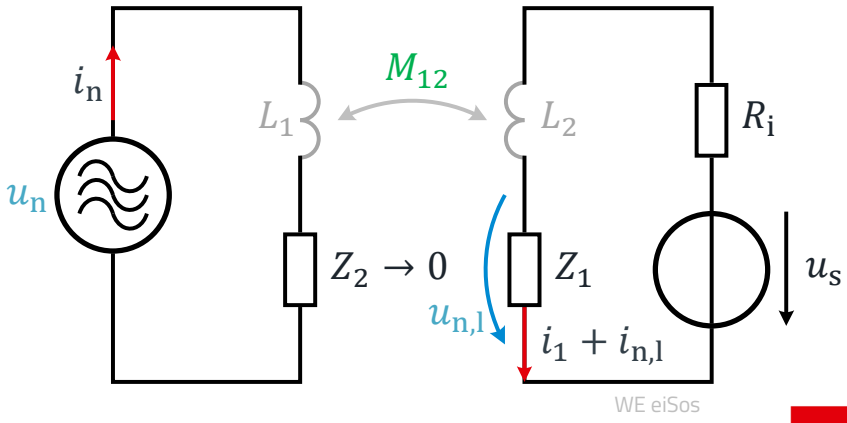
Inductive Coupling

Effects

- Takes effect, if loops are larger than 25% the wavelength of the exciting magnetic field (< λ/4).
- Voltage interference at the load:

$$u_{\mathrm{n,l}} = M_{12} \cdot \frac{\mathrm{d}i_{\mathrm{n}}}{\mathrm{d}t} \cdot \frac{Z_1}{R_{\mathrm{i}} + Z_1}$$

$$M_{12} = \mu * N_1 N_2 * \frac{A}{l}$$

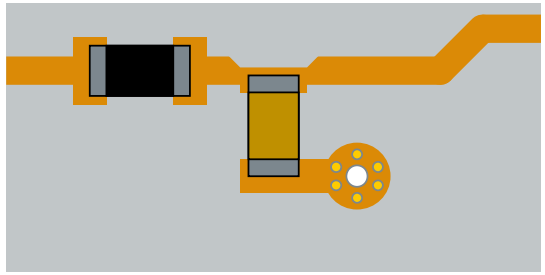


Inductive Coupling

Measures to decrease coupling

- **Primary Measure**
  - Decrease dI/dt by selecting a lower switching frequency and slower signal edges
  - A filter Inductor/Ferrite to take off the edges

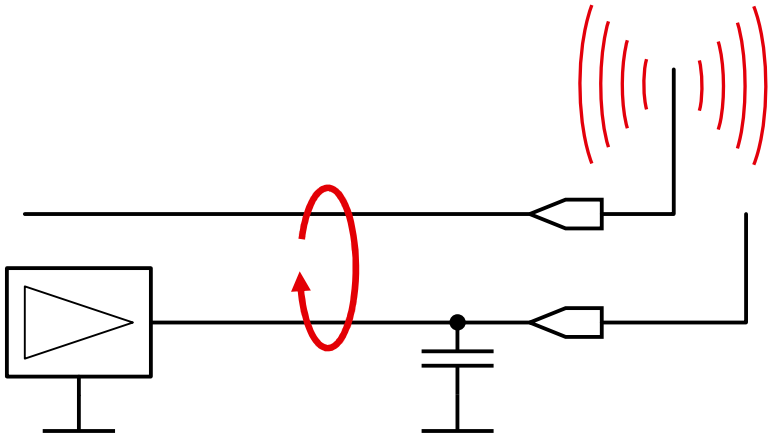
- **Secondary Measure**
  - Decrease magnetic loop area
  - Increase distance between affected circuits
  - Orthogonal component placement
  - Magnetic shielding with ferrite materials (soft permeability, high μ_r)



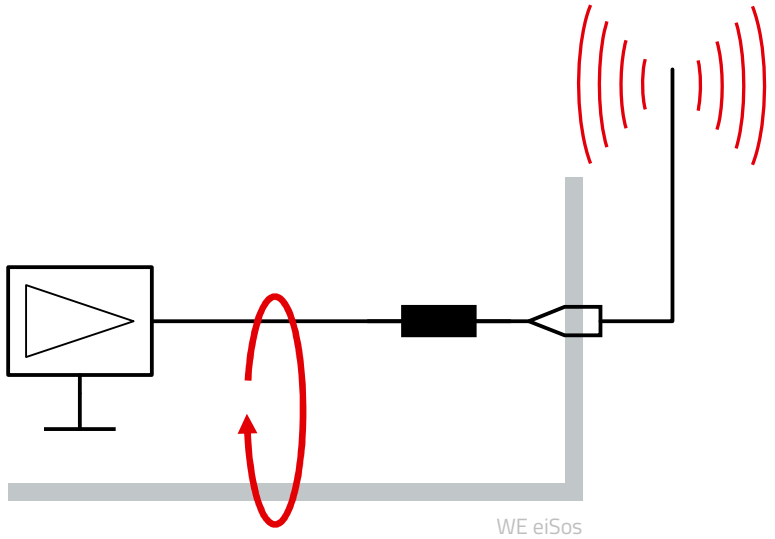
FILTER PLACEMENT

Filter Placement

Noise can bypass a misplaced Filter



Bypassing via parallel Lines

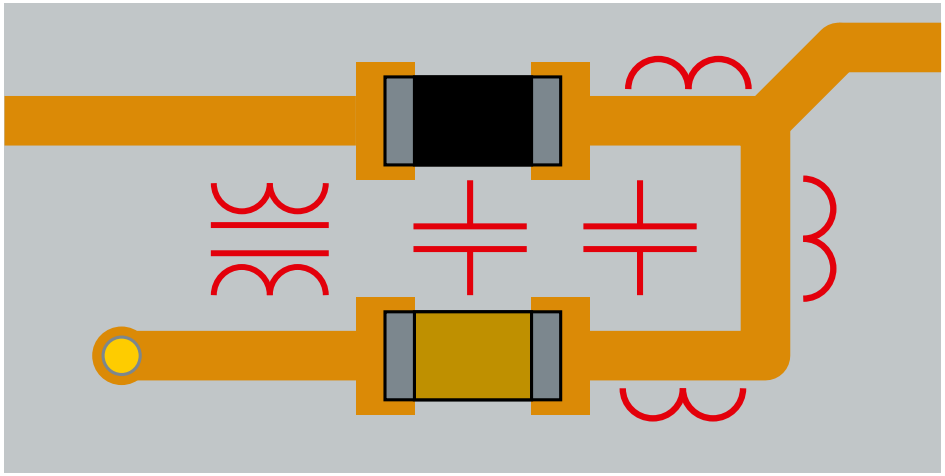


Bypassing via chassis parts

Filter Placement

Noise coupling in Single-Ended Filters

- Inductive coupling between filter input and GND via
- Capacitive coupling – increases with frequency
- Conductor inductance – traces too long
  - 1nH per 1mm
  - 0.5nH per Via



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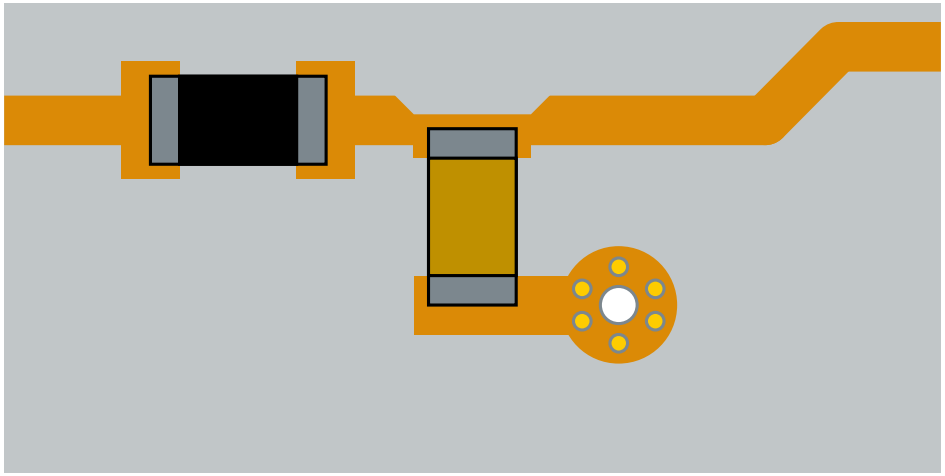
Filter Placement

Noise coupling in Single-Ended Filters

- Consticion of the trace at the capacitor's connection reduces reflections in the GHz range (VSWR)
- Orthogonal arrangement of L and C to minimize capacitive coupling
- Vias to GND can be tied to PE using e.g. a steel spacer



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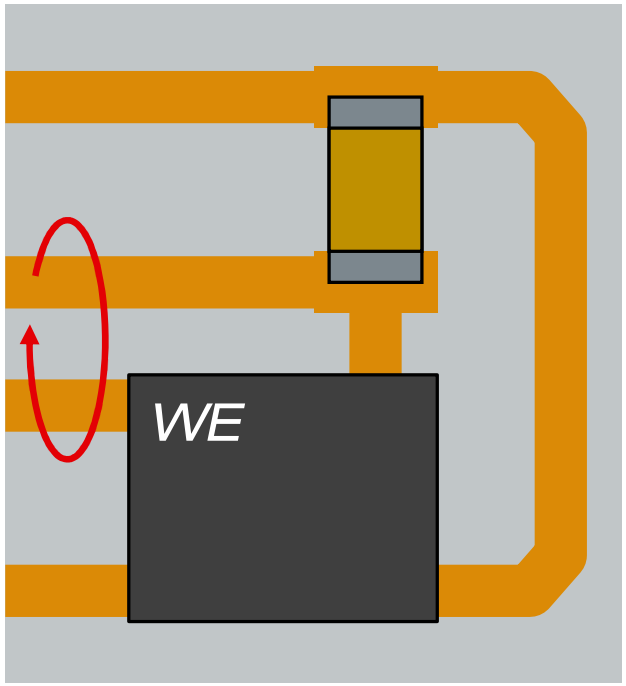
Filter Placement

Coupling Paths in Common Mode Filters

- CM-Filter as close to the connector as possible
  - Overvoltage is also running in CM!
- Avoid GND Plane beneath Choke
  - Possible coupling path / mode conversion
- Keep an eye on noise feedback from filter output to input



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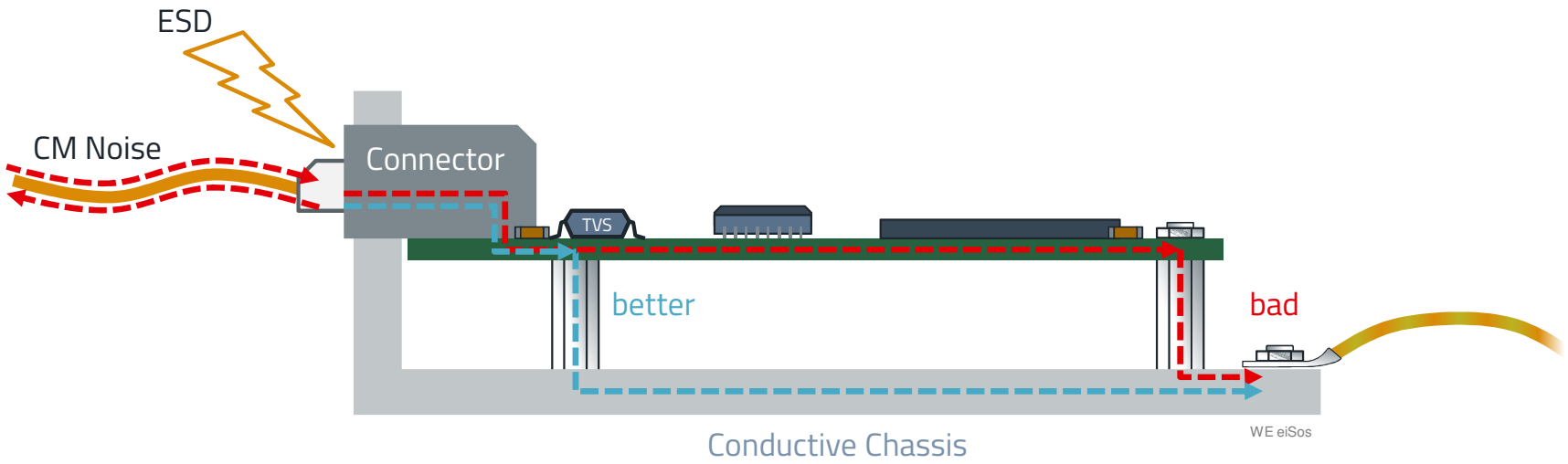
Inductive Coupling from CMC Output to Input

Filter Placement

Diverting Noise to Earth



- Grounding studs have to placed so that disturbances don't affect the electronic parts
- Reference ground for ESD (and common mode noise) is earth potential

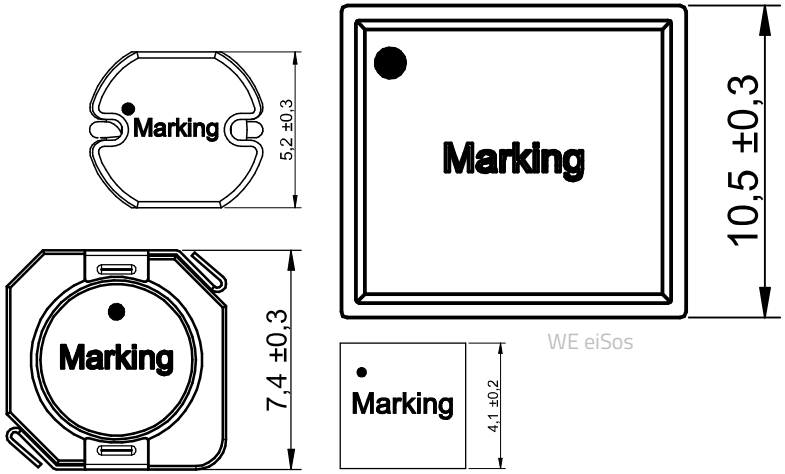
POWER INDUCTORS

Layout Considerations

Orientation of a Power Inductor

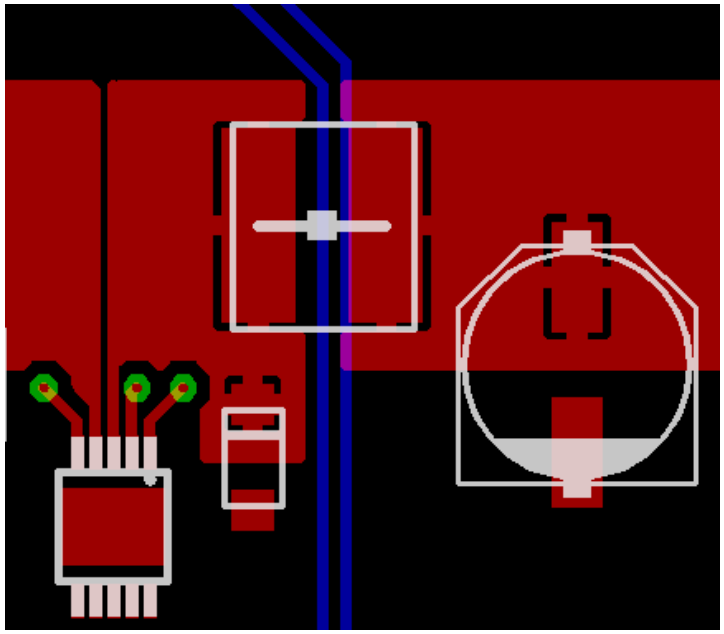
Keeping the Hot Node as small as possible

- Power Inductors with more than one layer of windings usually have marking indicating the start of winding
- Start of winding should be facing the Hot Node, so outer winding can act as a self shielding
- Even for Inductors with only one layer, orientation can make a difference (Height of terminal)
- Not every Inductor has a distinct start of winding due to the production process (e.g. Rod Cores)

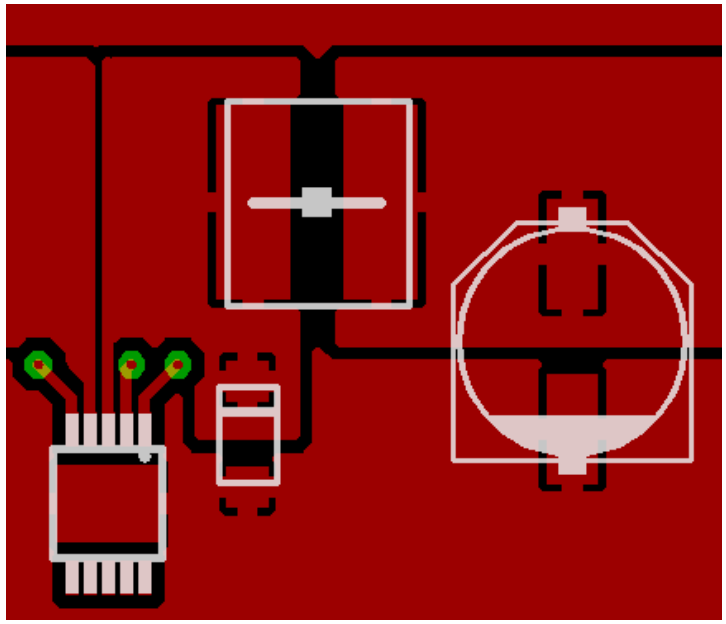


Traces below Power Inductors

Bottom side of Power Inductors is not shielded



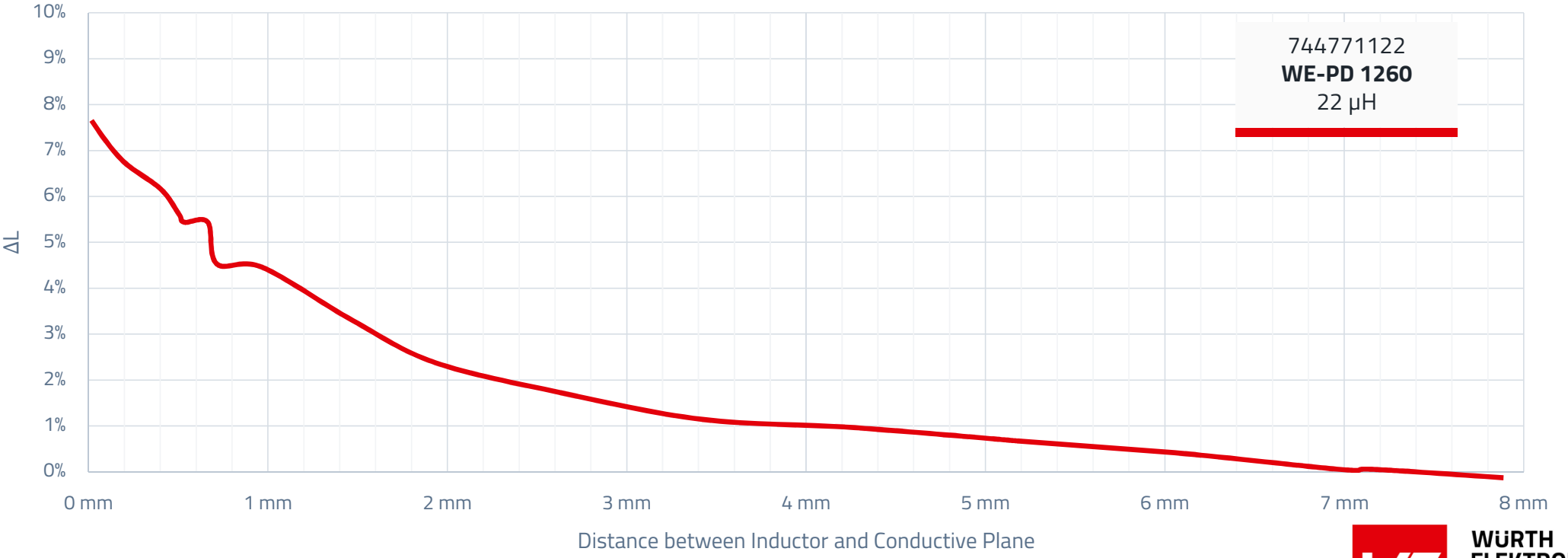
bad



good

Conductive Plane below Power Inductor

Influence on Inductance



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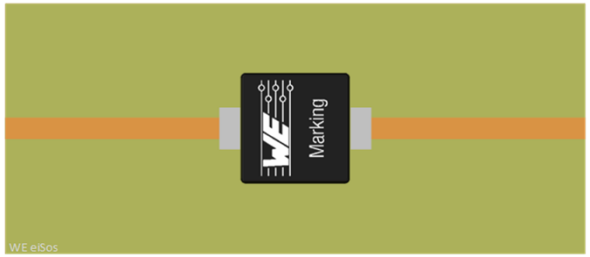
Conductive Plane below Power Inductor

Layout Options

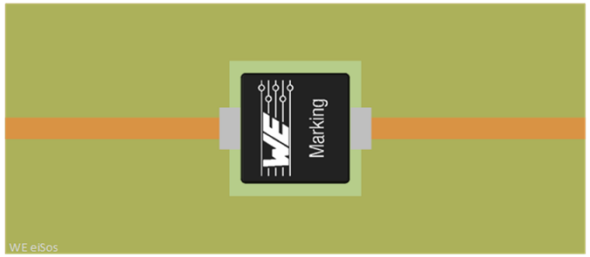
Continuous GND Plane



\+ Shielding the electric Near Field

\- Eddy Currents affect Inductance

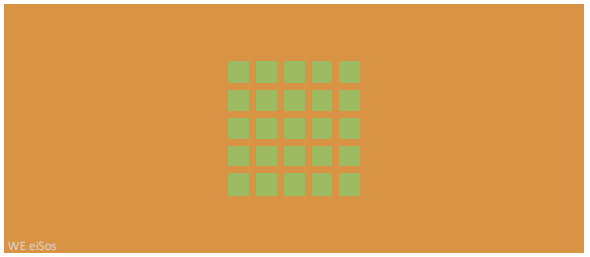
Opening in GND Plane



\+ Reduced Eddy Currents

\- Radiated Noise through PCB

Tradeoff - GND Grid



\+ Reduced Eddy Currents

\+ Reduced radiated Noise

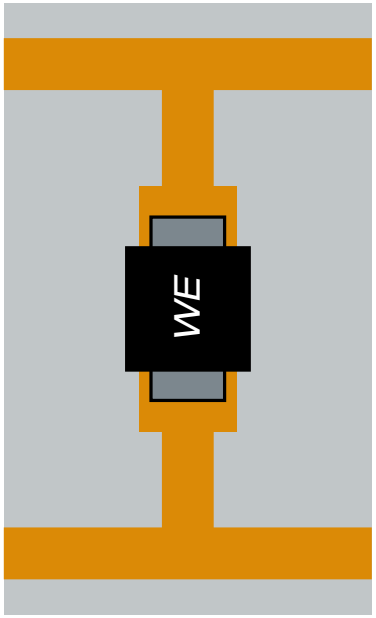
\- Increased Layout Efforts

OVERVOLTAGE PROTECTION

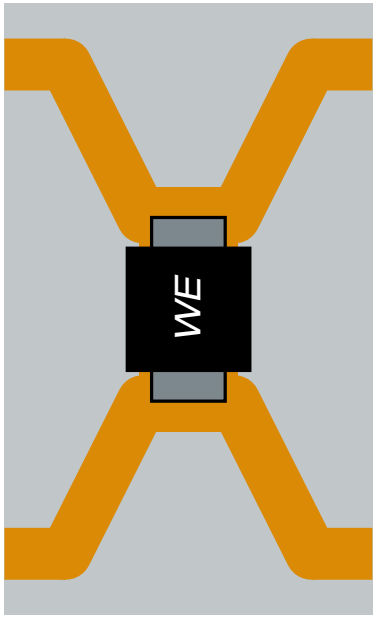
Layout Considerations

Routing OVP-Components

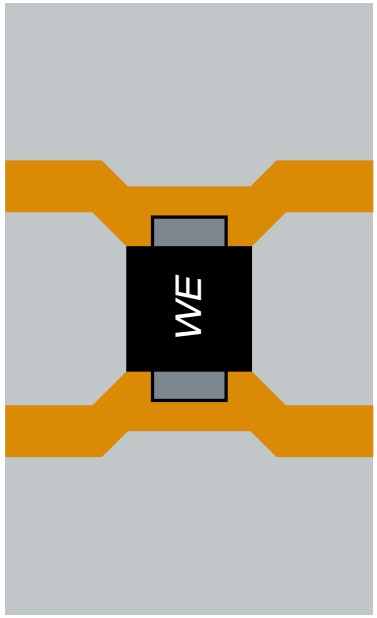
Keep Traces short and low impedance



Bad
Stub Traces



Good
Routing across SMD Pads



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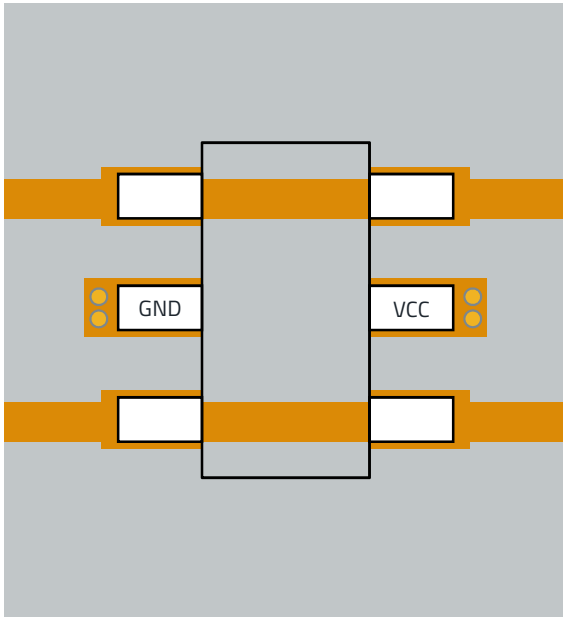
Best
Using Constictions at SMD Pads

Routing OVP-Components

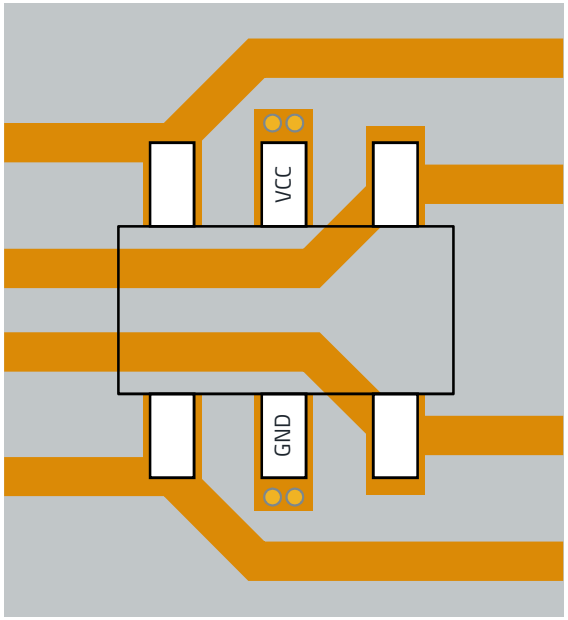
Keep Traces short and low impedance

- For TVS Diodes, multiple strips have to be coordinated across the component
- Parallel Vias to GND/ VCC plane for low impedant connection
- “Flow Through” design simplifies routing
- Impedance controlled traces and symmetrical routing for data lines

Routing for 2 Lines



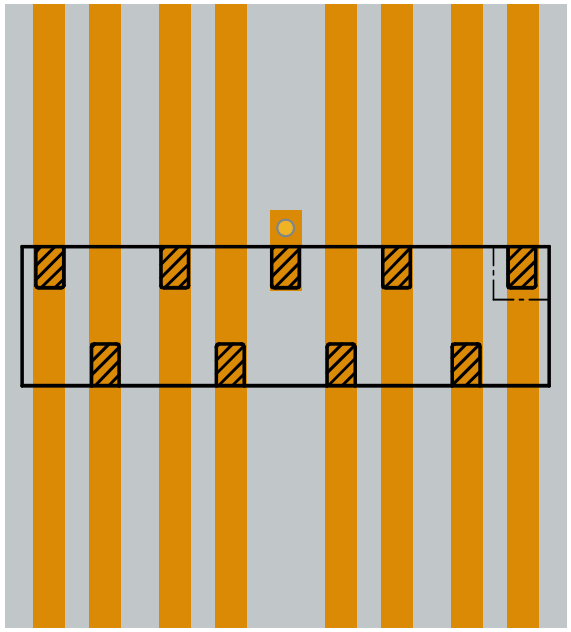
Routing for 4 Lines

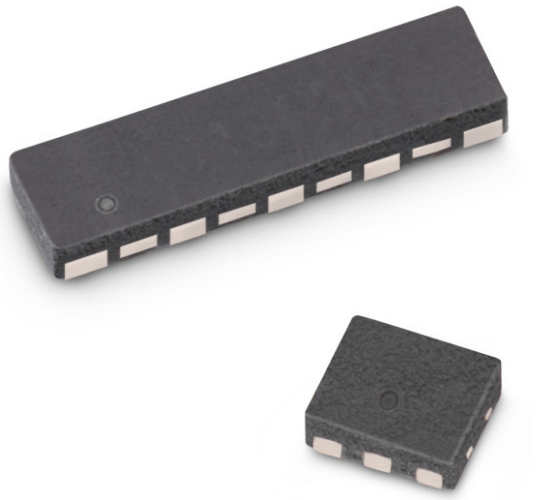


Routing OVP-Components

Special Design for High Speed Interfaces

- Higher requirements on impedance controlled traces and symmetrical routing
- “Flow Through” design simplifies routing

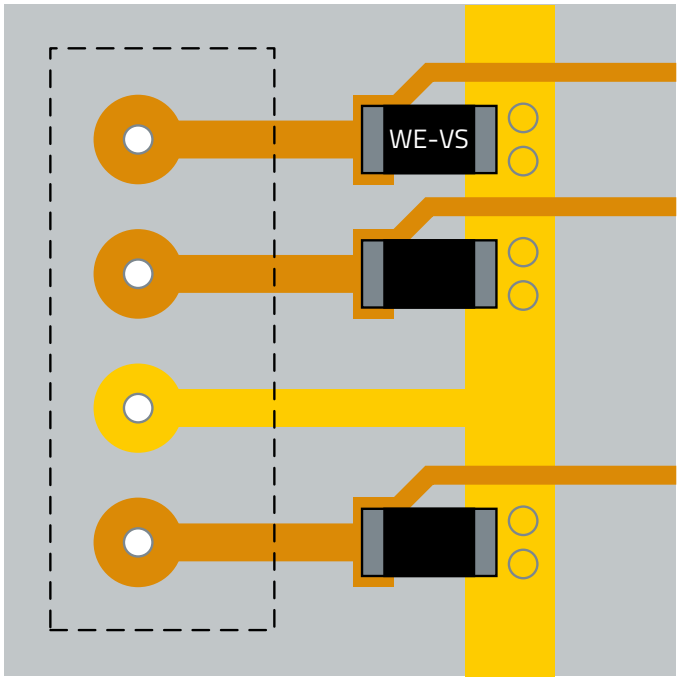




Connecting SMD Varistors

Separating Overvoltage Stressed Ports

Wide traces to Varistor terminals

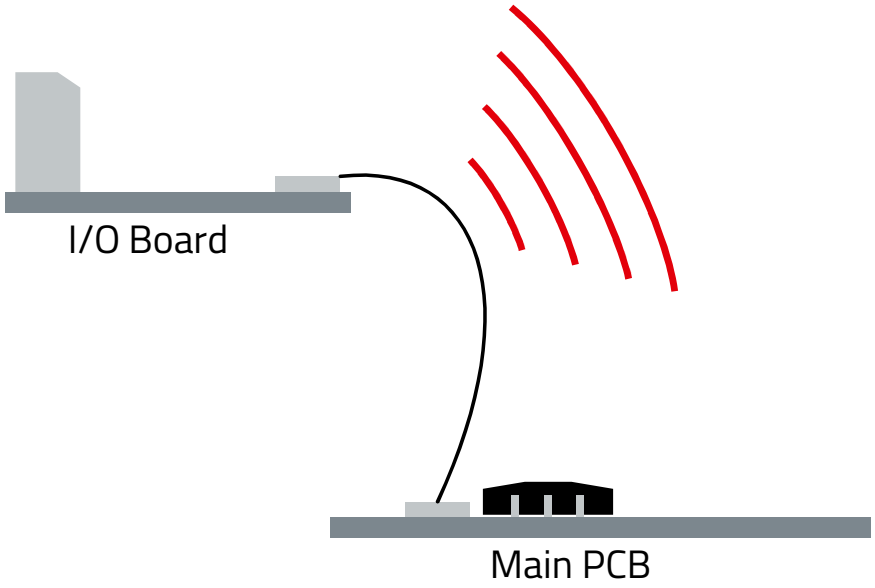


Regular traces for useful Signal

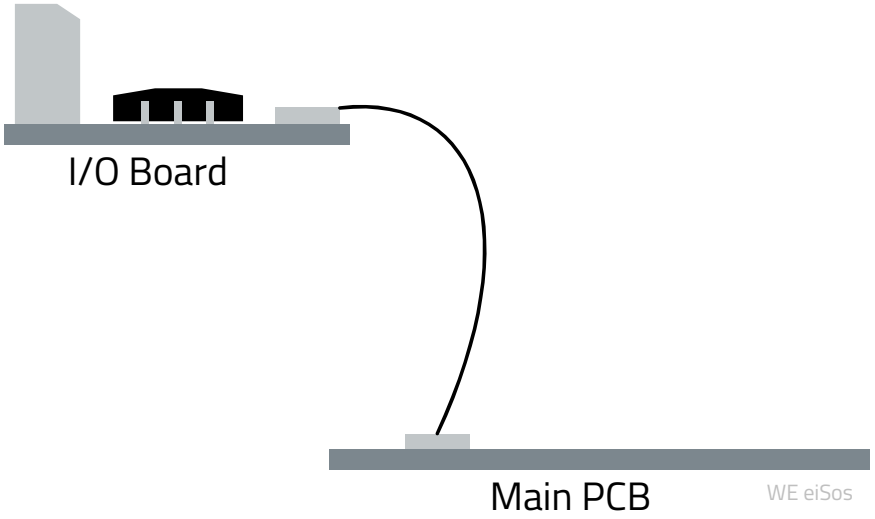
GND Trench

I/O Boards

Where to Place Overvoltage Protection



Placement on Main PCB



Placement on I/O Board

SUMMARY

Summary

- Coupling paths:
- Filter placement:
  - Avoid unwanted coupling
  - Divert noise to earth
- Power inductors:
  - Start of winding – dot marking
  - No traces underneath power inductor
- Overvoltage protection:
  - Keep traces short and low impedance
  - Flow through components
  - Location of the protection components