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TNO innovation for life

PLOT Showcase – Nov. 23rd 2011

Accelerated Stress Testing Electronic Packaging and Interconnects

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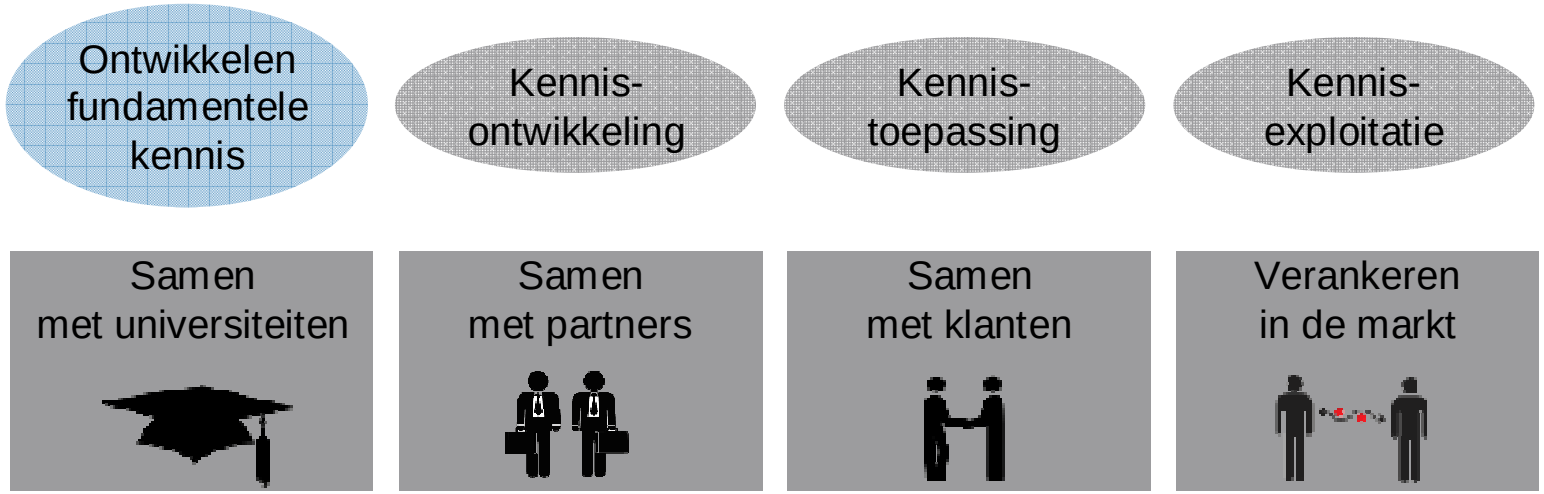
De missie van TNO

TNO verbindt mensen en kennis om innovaties te creëren die de concurrentiekracht van bedrijven en het welzijn van de samenleving duurzaam versterken.

Van idee naar innovatie:

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TNO: bij wet opgericht in 1932

Artikel 4 TNO wet

De Organisatie heeft ten doel ertoe bij te dragen dat op toepassing gericht technisch- en natuurwetenschappelijk onderzoek en daarmee te verbinden sociaal-wetenschappelijk en ander op toepassing gericht onderzoek op doelmatige wijze dienstbaar wordt gemaakt aan het algemeen belang en de daarbinnen te onderscheiden deelbelangen.

- TNO helpt bedrijven en overheden met behoefte aan specifieke R&D
- TNO is onafhankelijk van publieke of private belangen


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Expertisegebieden

- Technical Sciences
- Behavioural and Societal Sciences
- Earth, Environmental and Life Sciences

TNO Technical Sciences in Eindhoven.

Thema's:

Advisering

Contractresearch

Testen en certificeren

Licenties

Uitvoeren wettelijke taken

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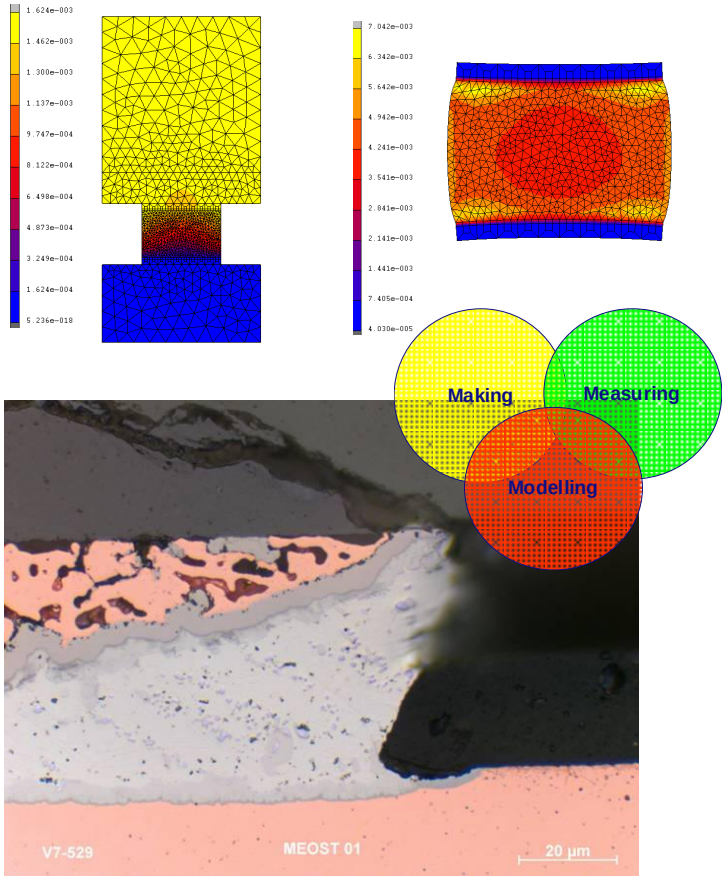
Materials for Integrated Products

- Structure and Bonding
- Performance Prediction



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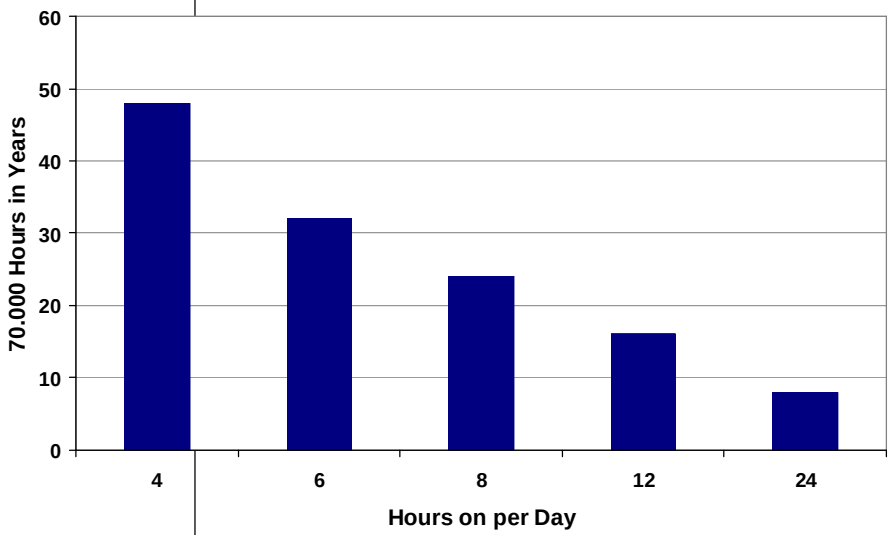
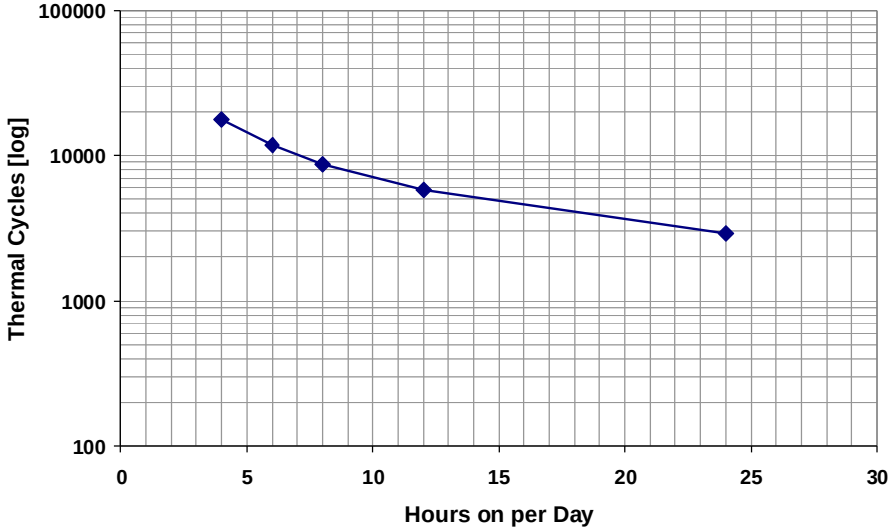
Challenges 2nd Level Interconnects LEDs

“70.000 Hour LED Lifetime” in Practice



70.000 Hours in Years.



Thermal cycles (on/off only).

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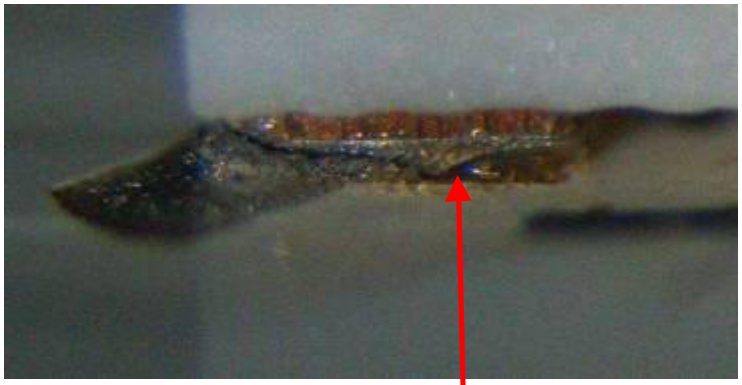
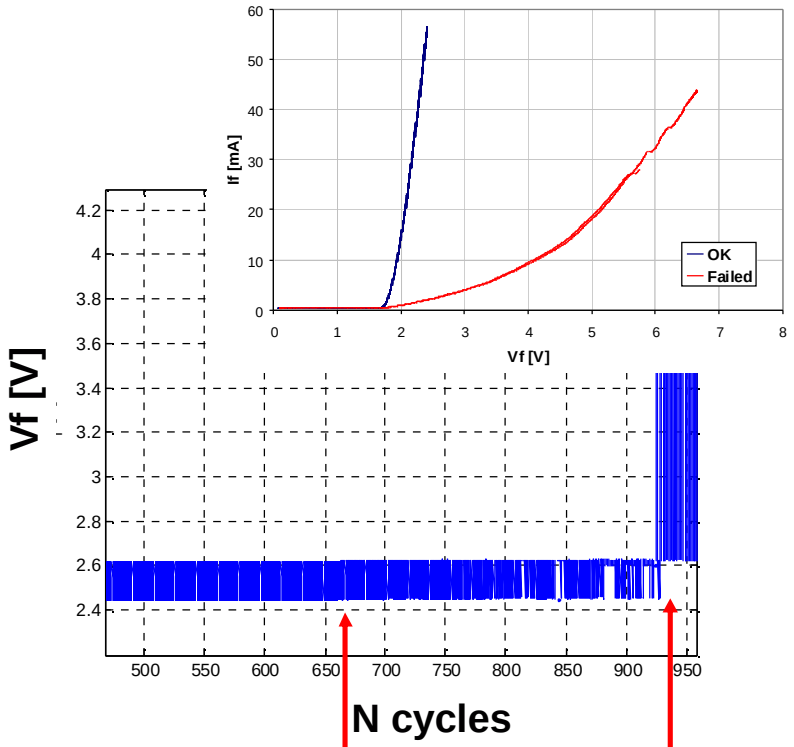
Accelerated Lifetime Testing LED Interconnects

Forward voltage as in-situ failure indicator for degradation:

- solder joints
- die-attach
- wire bonds
- ……



Crack in 2nd level solder joint HB-LED



Begin crack propagation

Open contact

Lifetime of Solar Panels

- Lifetime solar panels typically 20 to 30 years
- Panels mainly qualified by industry standard tests (e.g. IEC 61215 and 61646)

"*New approaches needed to design lifetime and reduce TTM*"

Testing and modelling with basis in physics of failure

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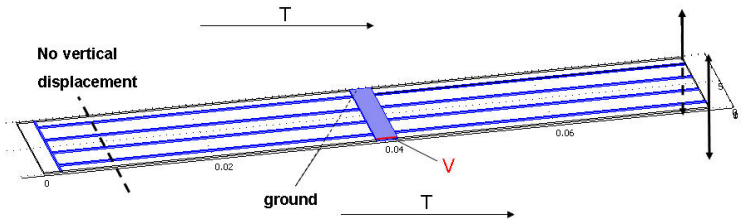
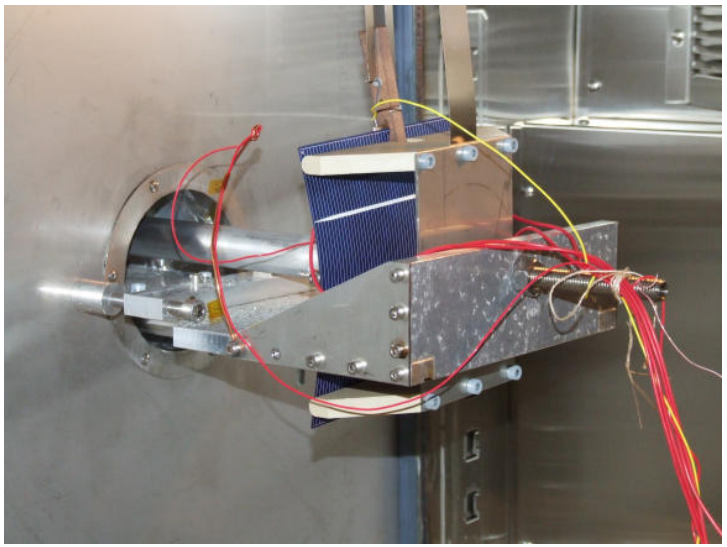
MEOST & Finite Element Modelling (FEM)

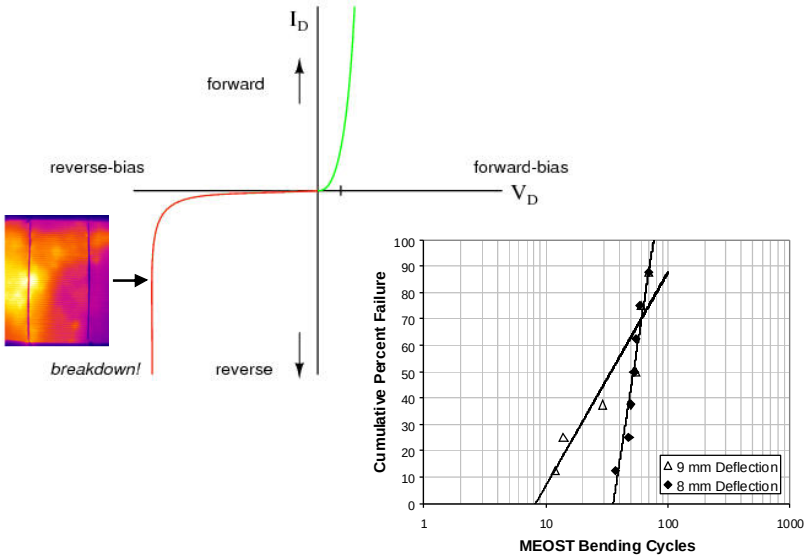
Multi-physics modelling of critical overstress test conditions

	$V_{Destruct}$	V_{MPOSL}
3p bending deflection	10.7 mm	9.10 mm
Reverse bias	22 V, 19 A	18.7 V, 16.2 A
Temperature cycling		-70 to +180 °C*

$$V_{MPOSL} = V_{Design} + [(V_{Destruct} - V_{Design}) \times 0.7]$$





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Other Examples Present Reliability Projects

- Remaining lifetime of electronics
- Performance electronics components when using new control circuitry / approach
- Investigation of newly discovered failure mode in High Brightness LED
- Performance of unusual substrate material in LED package
- Development of screening method to detect black pads on PCBs (Printed Circuit Boards)

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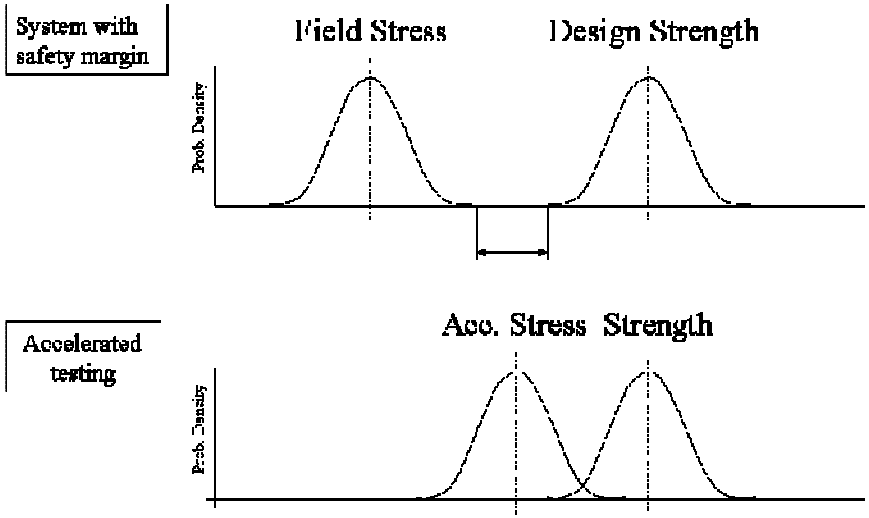
Accelerated Testing and making Inferences

Basic approach:

1) Identify dominant failure mechanism
2) Conduct accelerated tests at different levels
3) Estimate probability density function (PDF)
4) Model life-stress relations

Making Stress Strength Inferences:



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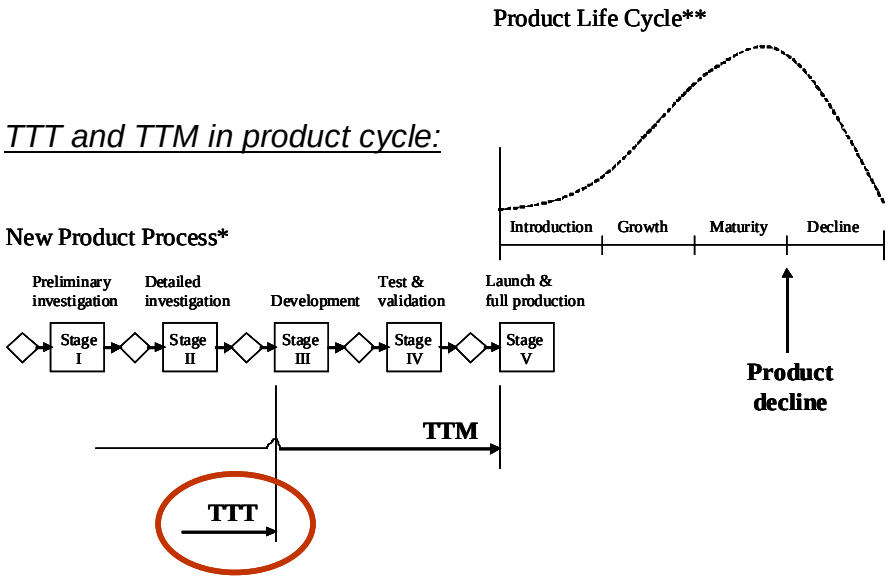
Reliability Trends

- Electronic products get more complex
- Higher reliability levels (two → single digit ppm levels equipment)
- Reduction lead times product development / validation cycles (TTM)
- Traditional ways of testing can't keep up with technology trends
- Operational conditions moving towards accelerated test levels
- Designed lifetimes

Failure levels:

No. Failure Per Device-Hours	Failure Rate	% Per 1000 Hours	PPM (Hours)	FITS	MTBF (Hour)
$1/1 \times 10^{9}$	0,000000001	0,0001	0,001	1	1×10^{9}
$1/1 \times 10^{8}$	0,00000001	0,001	0,01	10	1×10^{8}
$1/1 \times 10^{7}$	0,0000001	0,01	0,1	100	1×10^{7}
$1/1 \times 10^{6}$	0,000001	0,1	1	1000	1×10^{6}
1/100,000	0,00001	1	10	10.000	1×10^{5}
1/10,000	0,0001	10	100	100.000	1×10^{4}
1/1,000	0,001	100	1000	1.000.000	1×10^{3}

TTT and TTM in product cycle:

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Possible Strategies to further shorten Accelerated Reliability Tests

- Increasing stress / frequencies levels till beyond current accelerated test levels
- Combining test loadings (incl. usage rate acceleration)
- Increasing rate of applying loadings
- Intentionally inducing interaction effects between loadings
- Using alternative loadings (to initiate the same failure mechanism)

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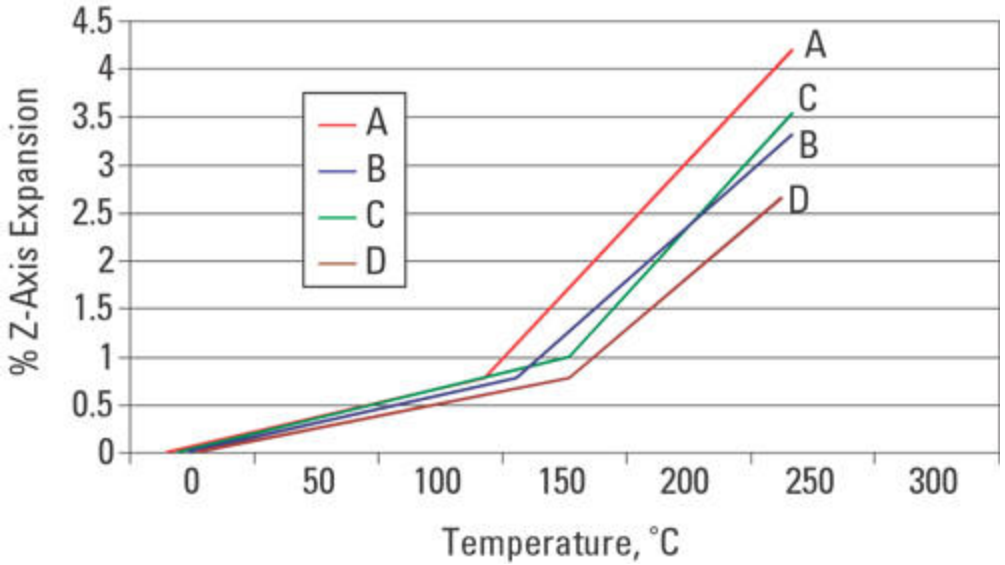
Challenges when further Accelerating Tests

- Maintaining the correlation between failure behaviour during tests and field conditions
- Avoiding complex tests and analysis methods when using multi environment tests

Example: Z-axis expansion when increasing test temperatures above the Tg of Printed Circuit Boards



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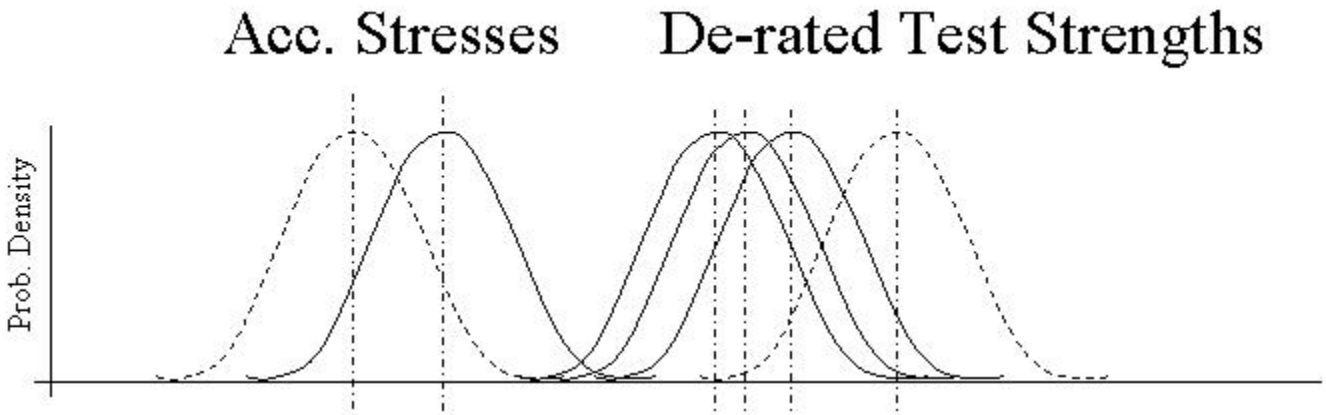
Use of De-rated Strength Testing



- Moderate multi environment stresses
- Different sensitivity levels (use of Design of Experience)
- Design optimisation and prediction with modelling techniques

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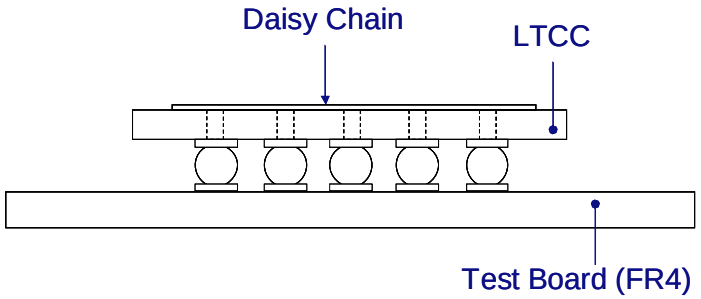
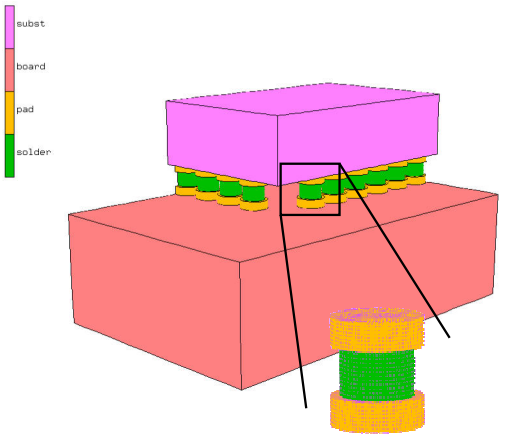
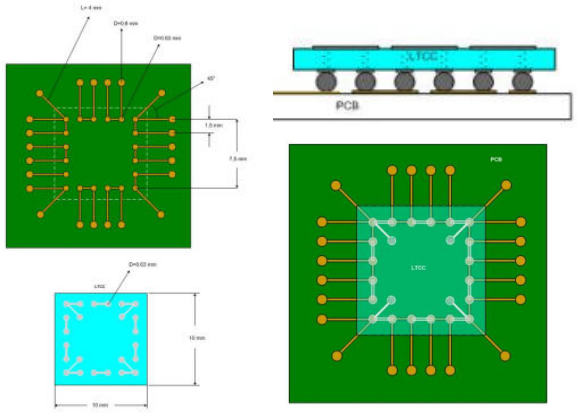
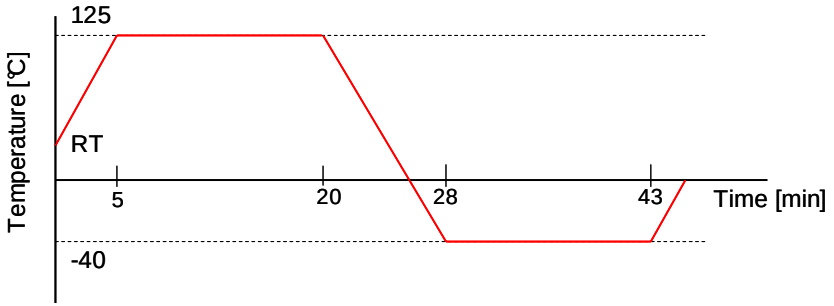
De-rated Strength Vehicle: testing 2nd Level Interconnects

LTCC Interposer on FR4 Test Board: SnAgCu v SnBi Solder Balls









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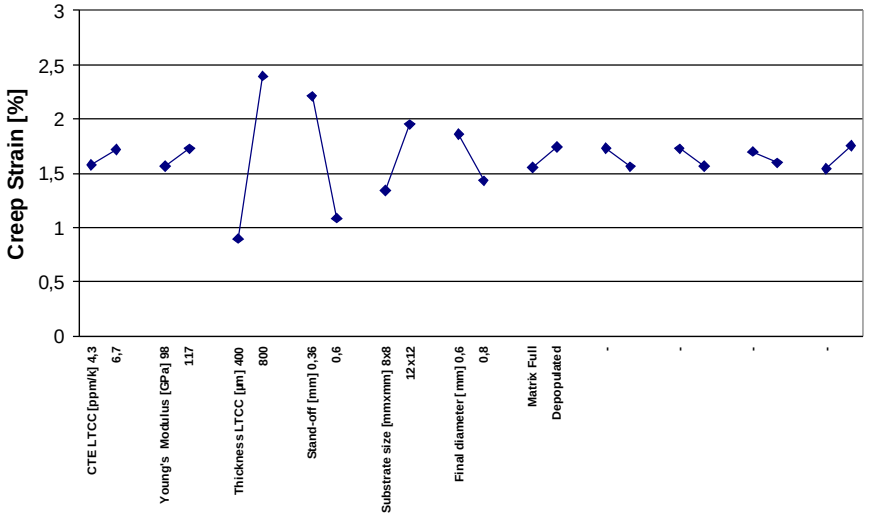
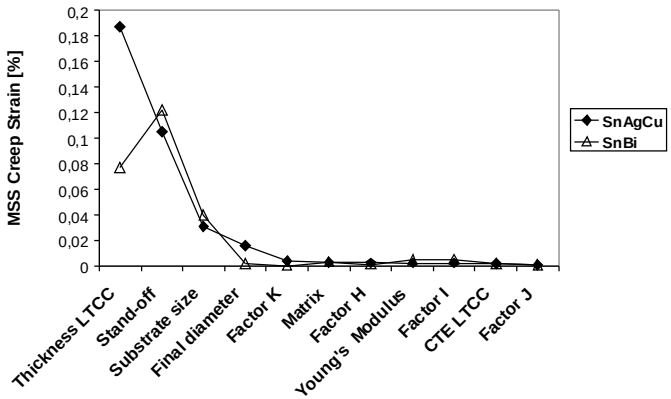
From selection significant Factors to designed Test Conditions

Design of Experiments: L12- SnAgCu

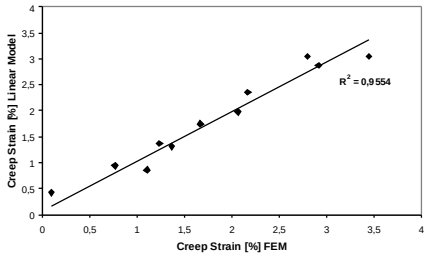


Contribution Factors: Scree



Significant Factors > De-rated Design Model: Regression Analysis

	Coefficients	*Standard Error*	*t Stat*	*P-value*	*Lower 95%*	*Upper 95%*	*Lower 95,0%*	*Upper 95,0%*
Intercept	1,643	0,823081463	1,996157213	0,086105917	-0,30327839	3,589278389	-0,303278389	3,589278389
Thickness LTCC [µm]	0,003749167	0,000411541	9,110074358	3,94115E-05	0,002776027	0,004722306	0,002776027	0,004722306
Stand-off [mm]	-4,679166667	0,685901219	-6,821924986	0,000248218	-6,30106532	-3,057268009	-6,301065324	-3,057268009
Substrate size [mm x mm]	0,151583333	0,041154073	3,683313016	0,007825366	0,054269414	0,248897253	0,054269414	0,248897253
Final diameter [mm]	-2,165	0,823081463	-2,630359322	0,033894909	-4,11127839	-0,218721611	-4,111278389	-0,218721611



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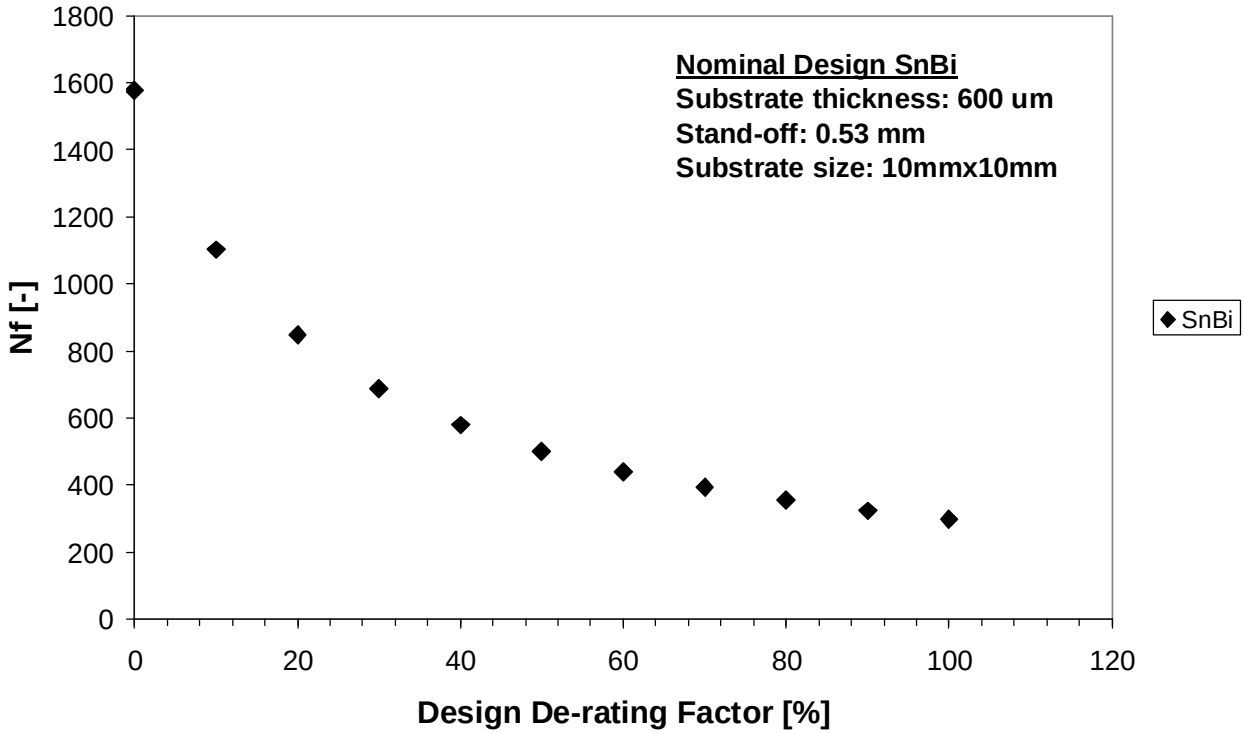
Designed Test Times: SnBi Example

- Test Cycles to Failure of De-Rated Test Strengths

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Summarising


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Thank you for your attention!


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