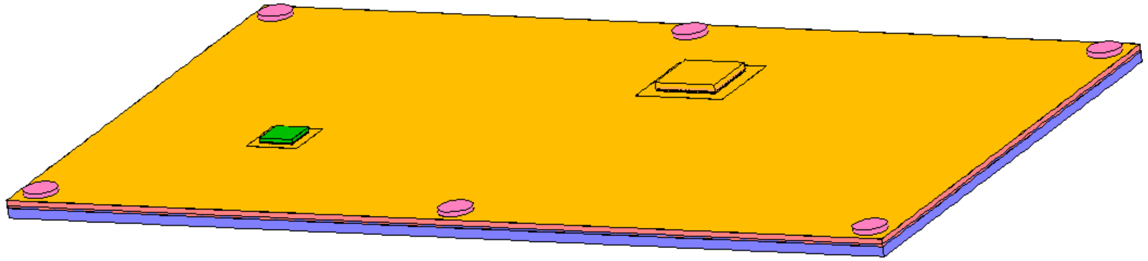
VIRTUAL TESTING OF THERMAL-MECHANICAL RELIABILITY OF ELECTRONIC SYSTEMS

PRESENTER: BART VANDEVELDE

PLOT EVENT – JABIL HASSELT

SCOPE

Can Virtual Testing be used to reduce the qualification test time by First Time Right design?



Showing the capabilities of virtual testing on a practical example

QUALIFICATION TESTING FOR ELECTRONIC SYSTEMS

RELIABILITY VS. QUALIFICATION TESTING

RELIABILITY QUALIFICATION OF ELECTRONIC SYSTEMS
BACKGROUND

Reliability qualification testing

- Reliability qualification testing is utilized to verify if a given product possesses advertised or established reliability requirements
- Reliability qualification testing is focused on the design of a product, and is also known as reliability demonstration, or design approval testing
- Typical loadings: high temperature exposure, thermal cycling, power cycling, vibration, mechanical shock

Typical failures induced in reliability qualification tests:

- Fretting wear of separable contacts
- fatigue and brittle cracking of electronic solder joints
- Fractures or permanent deformations due to high stresses;
- Loosening of fasteners
- PCB delamination
- Plated-through hole or via barrel fatigue
- Fractures in components

QUALIFICATION VS. RELIABILITY TESTING

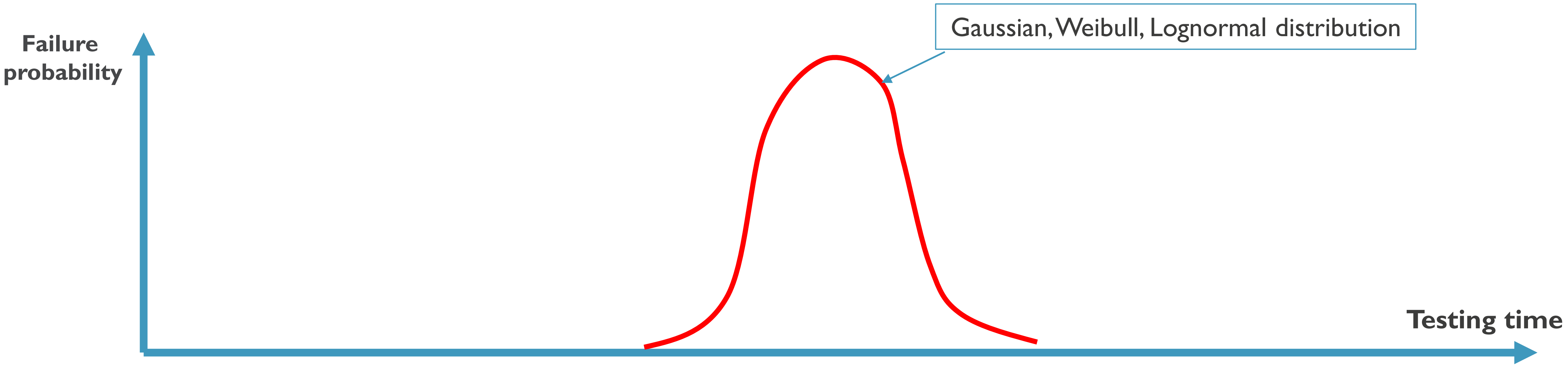
Qualification Testing

- Process of demonstrating that a product is capable of meeting specified requirements. The process is defined in standards and/or by the customer
- Application driven
- Mostly succession of different tests
- Testing time pre-defined
  - E.g.: 500 hours at 150°C, followed by 200 temperature cycles 0 to 100°C
- Outcome: pass or no-pass

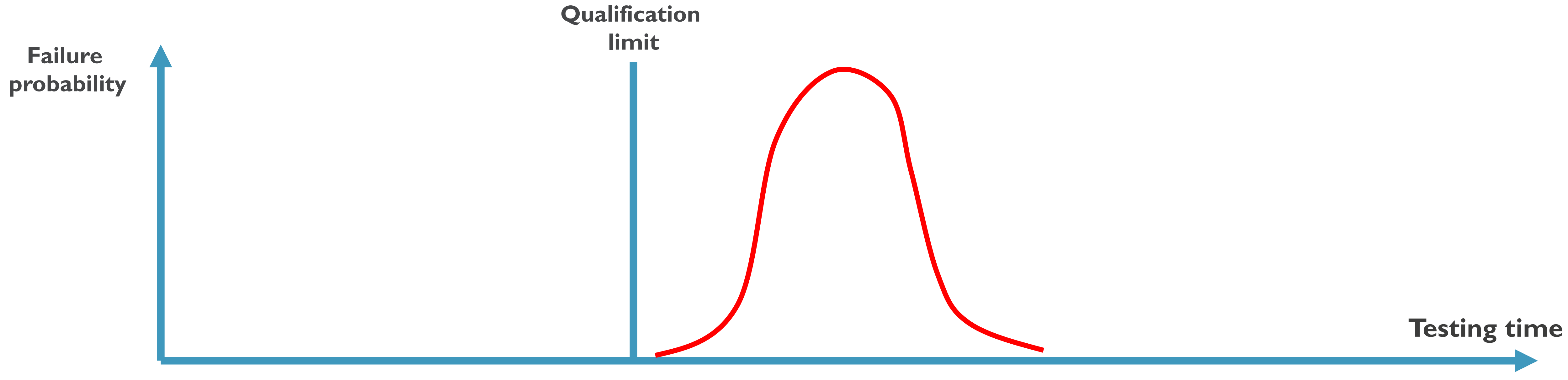
Reliability Testing

- For a statistical relevant number of products, perform stress testing according to conditions specified by standards and/or customer till products fail
- Mission profile driven
- Focused on one test condition
- Testing till most products failed
  - E.g. thermal ageing at 150°C till **63%** of products fail
- Outcome: failure probability over time

FAILURE PROBABILITY OVER TIME
EXTRACTED FROM RELIABILITY TESTING



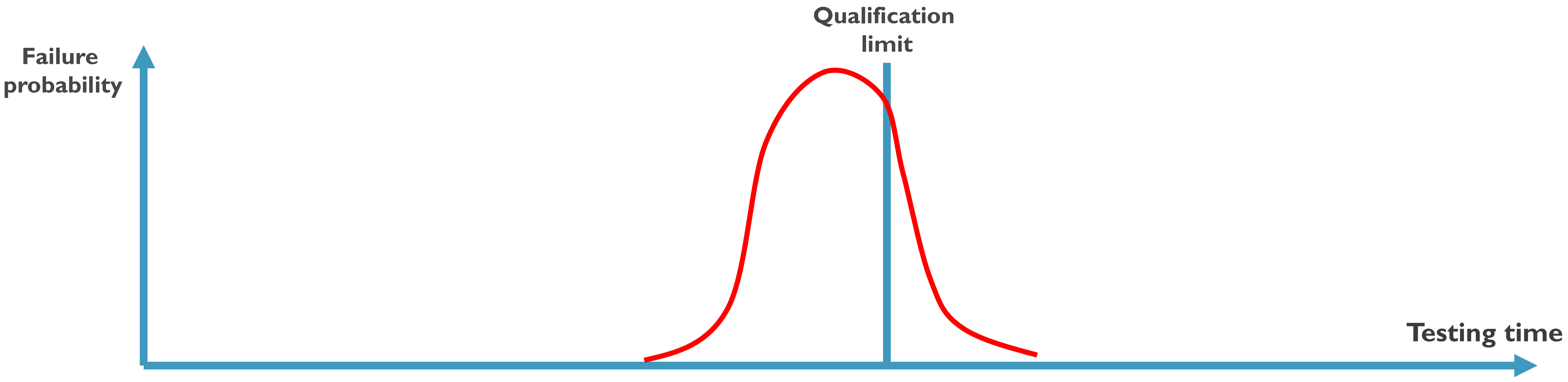
FAILURE PROBABILITY OVER TIME
LINK TO QUALIFICATION



High probability that product will **pass** the qualification test

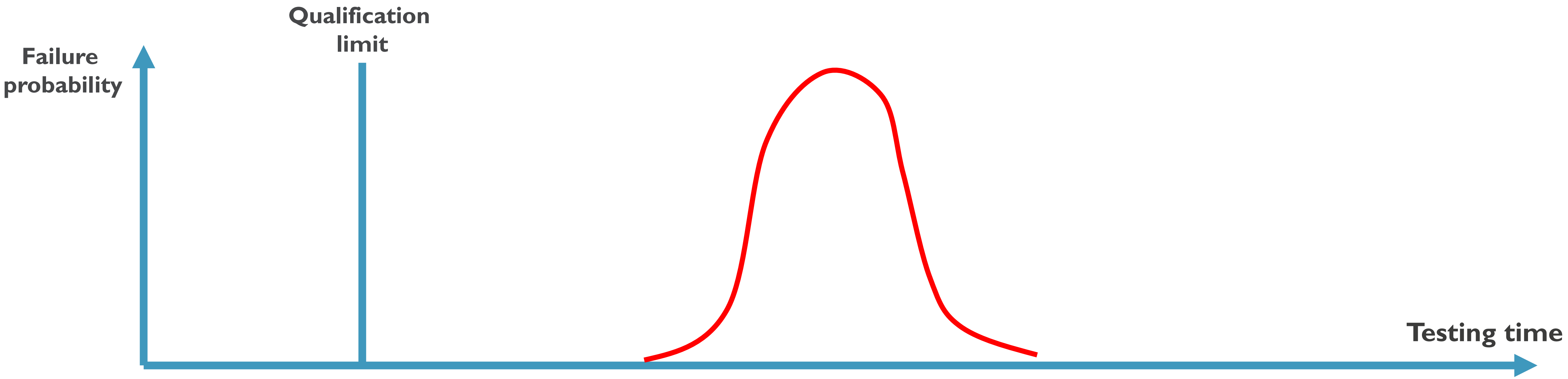
FAILURE PROBABILITY OVER TIME

LINK TO QUALIFICATION



High probability that product will **fail** the qualification test

FAILURE PROBABILITY OVER TIME
LINK TO QUALIFICATION



High probability that product will **pass** the qualification test.
BUT, the product is overdesigned from reliability perspective

QUALIFICATION TESTING STANDARDS @ PCB LEVEL
OVERVIEW

Test Item	Test Condition
Temperature Cycle Test	JESD22-A104, -40°C to 125°C, 1 cycle/h
Mechanical Shock Test	JESD22-B110 Condition F2
Vibration Test	JESD22-B103
Bend Test (DT & Mobile)	IPC-9702
Cyclic Bend Test (Handheld Products)	JESD22-B113
Drop Test (Handheld Products)-NVIP Board Design	JESD22-B111 Condition B
Bend Test (Handheld Products)	Customer Specific

QUALIFICATION TESTING STANDARDS @ PBA LEVEL

CUSTOMER SPECIFIED REQUIREMENTS

RFMD	RFSA2524 Qualification Report	Page 2 of 2

Qualification Tests

Test Name	Test Standard and Conditions	# Samples x # Lots	Test Results		
Temperature Characterization	JESD86 +25°C, -40°C, +85°C	2 x 3 lots	Pass		
High Temperature Operating Life	JESD22-A108 125°C, 1000 hours	77 x 3 lots	Pass		
Steady State Temperature Humidity Bias Life Test	JESD22-A101 +85°C, 85%RH, 500 hours Preconditioning per JESD22-A113 MSL3	24 x 3 lots	Pass		
ESD Human Body Model	JESD22-A114	3 x 1 lot	Pass 1000V	Class 1C	
ESD Charged-Device Model	JESD22-C101	3 x 1 lot	Pass 1000V	Class IV	
IC Latch Up	JESD78 Class I : +25°C Level A : ±100 mA	6x 1 lot	Pass		
Moisture Sensitivity Level Classification	J-STD-20 MSL3 30°C, 60% RH, 192 Hour Soak 3x Reflow at 260°C	25 x 3 lots	Pass	MSL3	260°C
Temperature Cycling	JESD22-A104 Test Condition G : -40°C to +125°C 500 cycles Preconditioning per JESD22-A113 MSL3	25 x 3 lots	Pass		
Temperature Cycling on Board	JESD22-A104 Test Condition G : -40°C to +125°C 500 cycles Preconditioning per JESD22-A113 MSL3	22 x 3 lots	Pass		
High Temperature Storage Life	JESD22-A103 150°C, 1000 Hours	22 x 3 lots	Pass		
Die Shear	MIL-STD-883, Method 2019 minimum 671 g, 972 g	10 x 3 lots	Pass		
Ball Shear	JESD22-B116 minimum 15 g, 20g	10 x 3 lots	Pass		
Bond Pull	MIL-STD-883, Method 2011 minimum 3 g	10 x 3 lots	Pass		
Solderability	JESD22-B102 Condition C : 8 Hour Steam Precondition Pb-Free Process Method 1 : Dip and Look	22 x 3 lots	Pass		
Conclusion	**This product has passed the RFMD Qualification Requirements for production.**				

Temperature Cycling on Board	JESD22-A104 Test Condition G : -40°C to +125°C 500 cycles Preconditioning per JESD22-A113 MSL3	22 x 3 lots	Pass

VIRTUAL TESTING METHODOLOGY

VIRTUAL TESTING – PROTOTYPING – POF BASED SIMULATION

THERMAL, MECHANICAL & THERMO-MECHANICAL ANALYSIS

Virtual prototyping:

- Numerical analysis technique where a geometric representation of a component or system is discretized into more basic shapes (finite elements in FEM; finite volumes in CFD)
- A loading of the system can be simulated and the impact on the structure can be calculated

CHALLENGES WITH VIRTUAL PROTOTYPING

- Accurate material properties:
  - Electronic system > 100 different materials
  - Regular introduction of new materials
  - Datasheets provided limited info → additional measurements needed
- Representative loading conditions
- Modelling of a complete system is impossible, even with advanced CPU → simplifications needed
- Still a way to go for acceptance for virtual prototyping in electronics

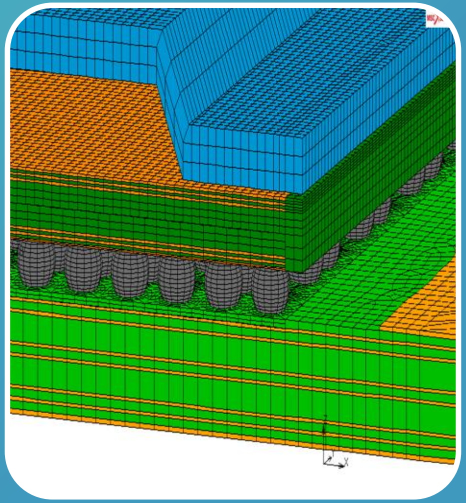
"Everyone believes the test results except the tester;
Nobody believes the simulation results except the simulator"

CHALLENGES WITH FINITE ELEMENT MODELLING (2)

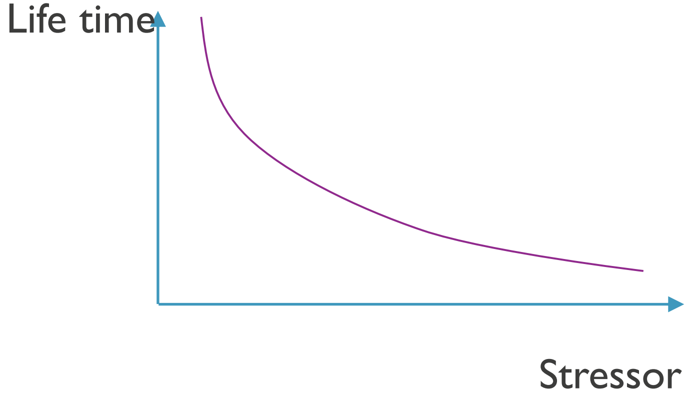
EMPIRICAL MODELS

Virtual prototyping

Physical parameters:
temperature, stress, strains, deformation

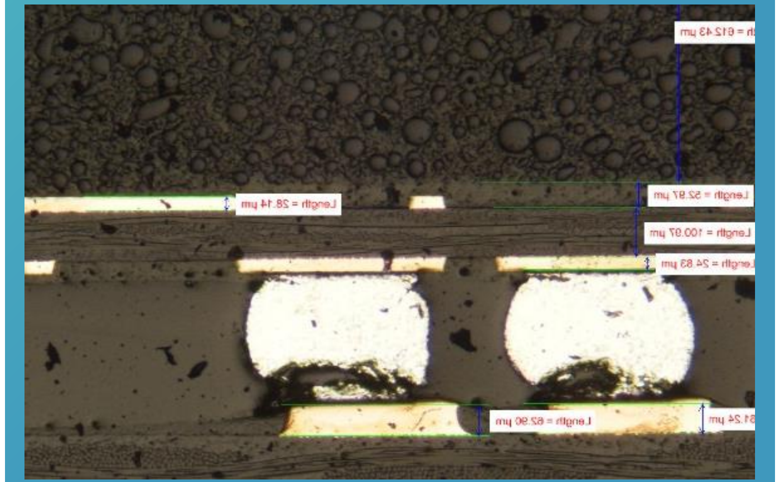


Physics Of Failure
empirical models



Reliability

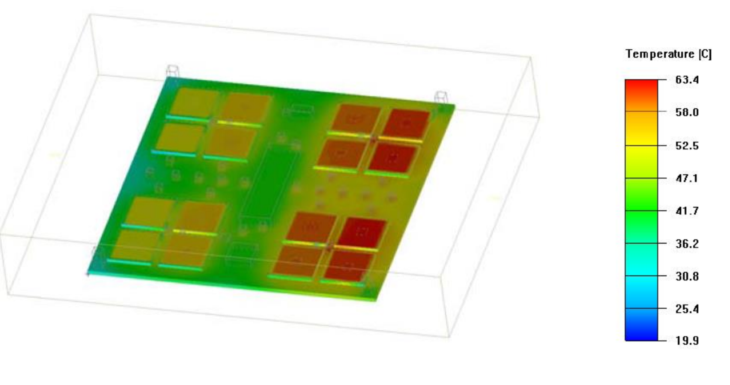
Life time of system/product
Reliability probability function
Any risk for fractures/damage?



SYSTEM LEVEL SIMULATION

Thermal modelling

- Simulation of temperature dissipation at PBA level due to power dissipation at different components



- Tools: CFD, FEM, engineering tools

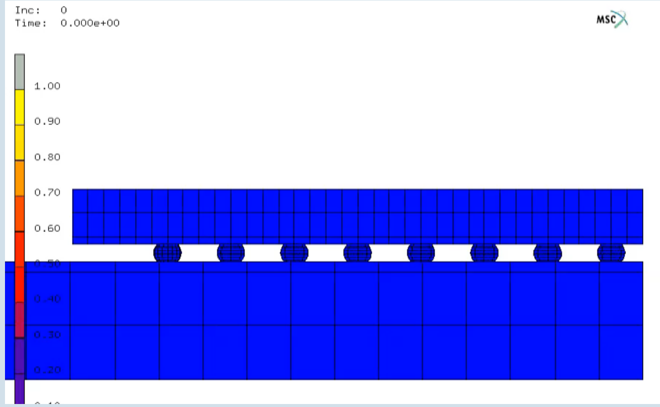
Mechanical modelling

- Simulation of vibration and shocks

- Tools: FEM, engineering tools

Thermo-mechanical Modelling

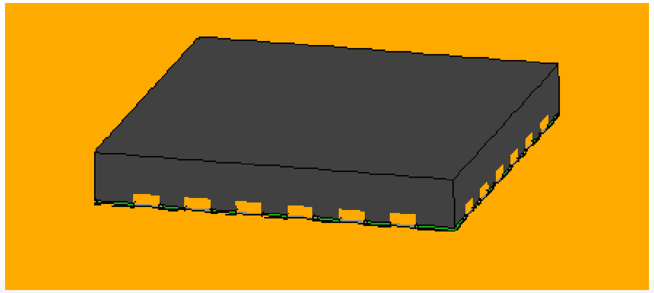
- Multi-physics simulation of isothermal and power cycling, and combined thermal/vibration cycling

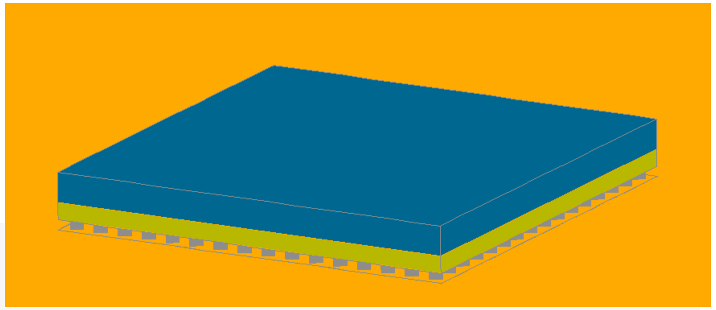


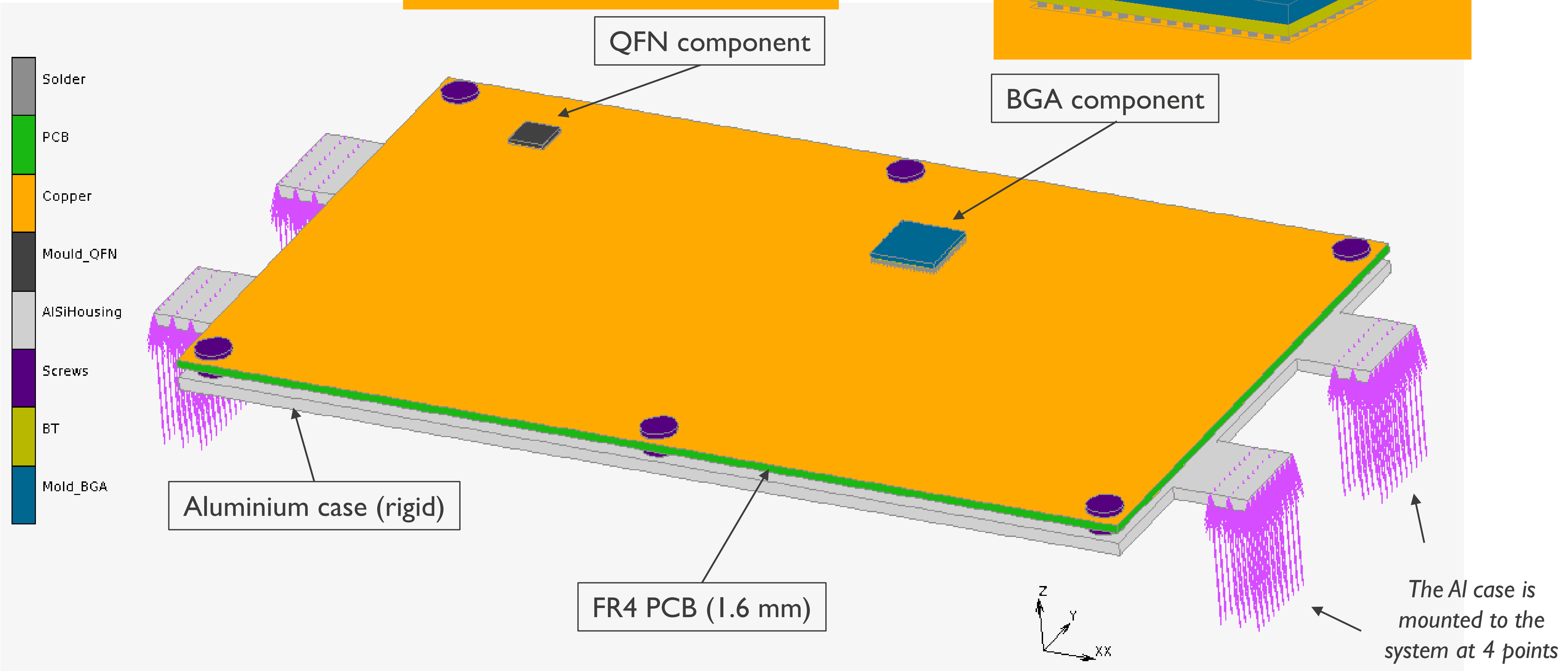
- Tools: FEM, engineering tools

EXAMPLE CASE STUDY

EXAMPLE CASE





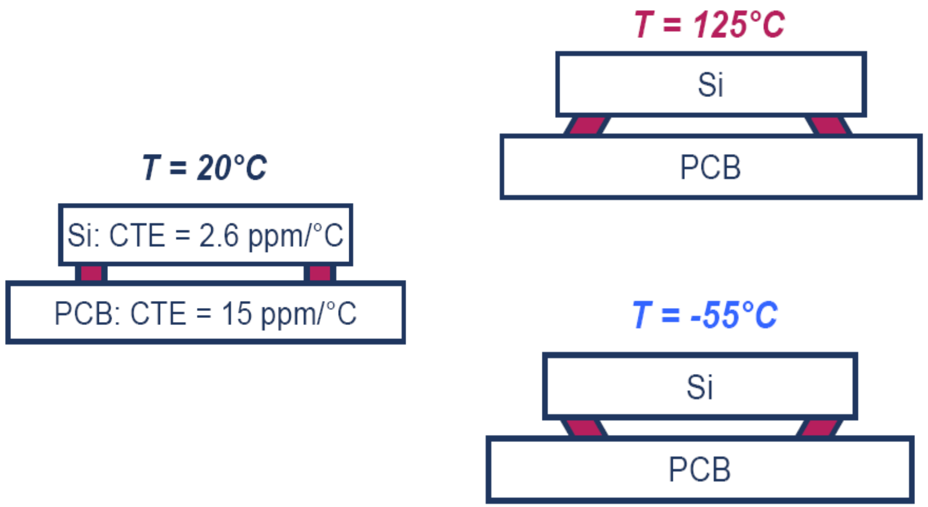


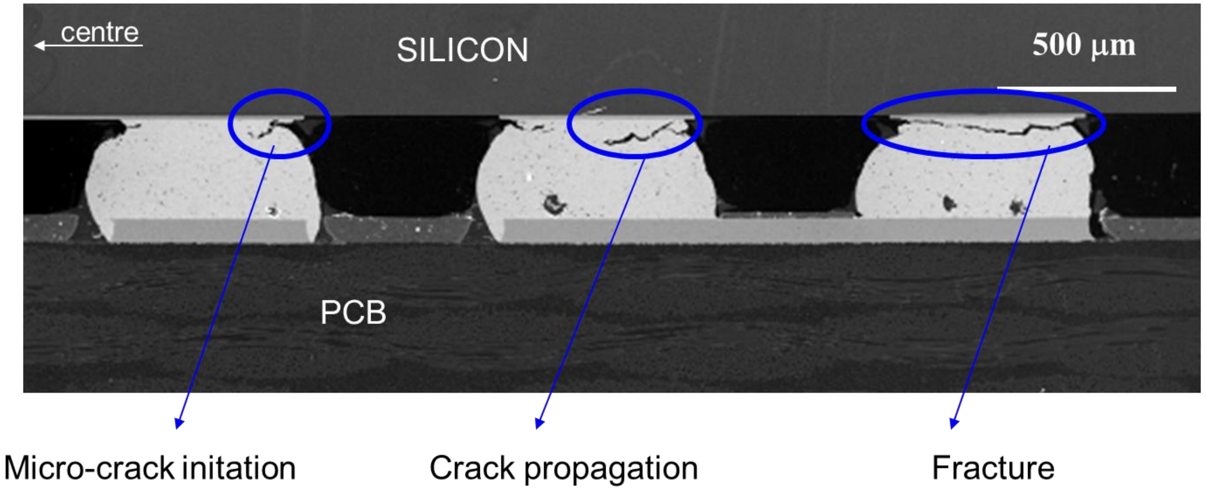
SIMULATION OF THERMAL CYCLING

-40°C TO +125°C THERMAL CYCLING, PASS 1000 CYCLES

THERMAL CYCLING

- **Qualification test**: -40°C to +125°C thermal cycling, pass 1000 cycles
- **Expected induced failure mechanism**:
  - solder joint fatigue





  - Plated Through Hole via's:
- **Virtual test**: FEM based simulation for solder joint & cEDM tool for via fatigue failure

VIRTUAL TESTING OF SOLDER FATIGUE INTERCONNECT FAILURES

Selection of critical components

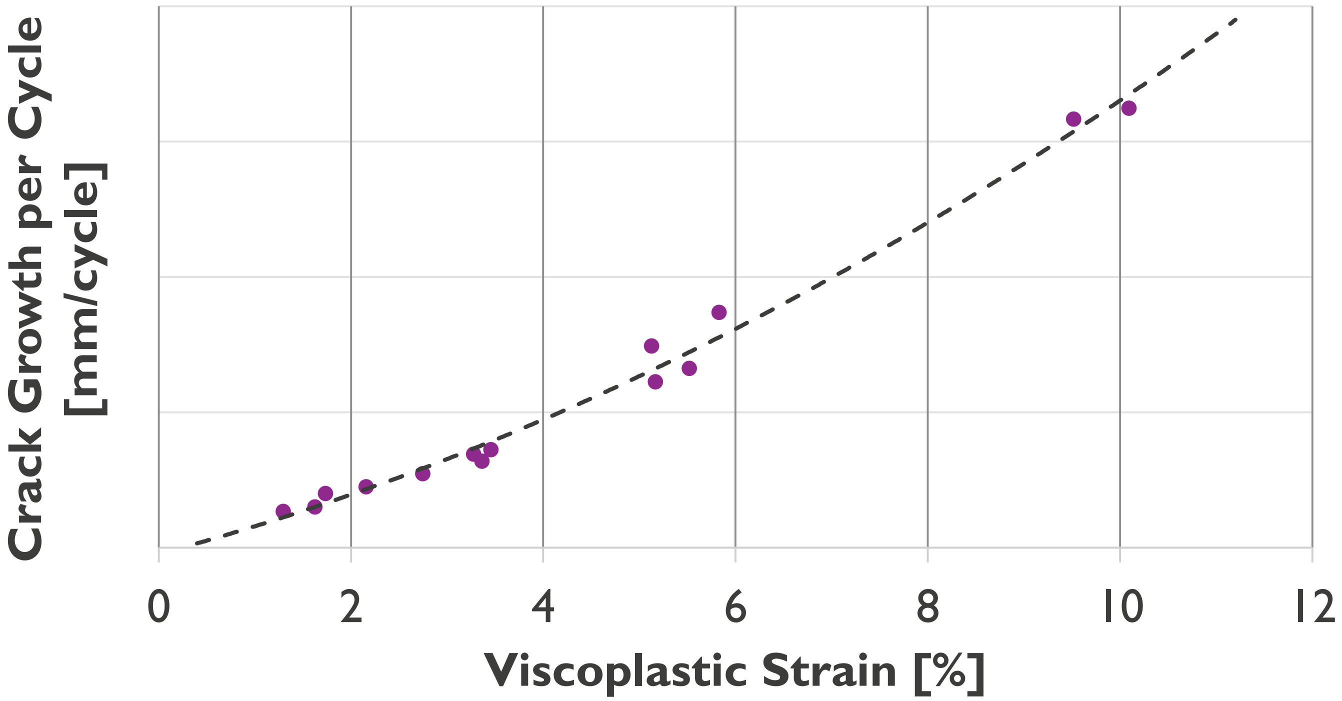
- Based on analytical models, engineering tools or experience
- Typical components sensitive to solder fatigue:
  - Large BGA (> 20 mm)
  - QFN (≥ 5mm)
  - Large SMD (2010, 2512)
  - Chip scale package
  - High power LED

- Be aware that qualification results provided by component suppliers are no guarantee for your application PCB

Temperature Cycling on Board	JESD22-A104 Test Condition G : -40°C to +125°C 1000 cycles Preconditioning per JESD22-A113 MSL3	22 x 3 lots	Pass

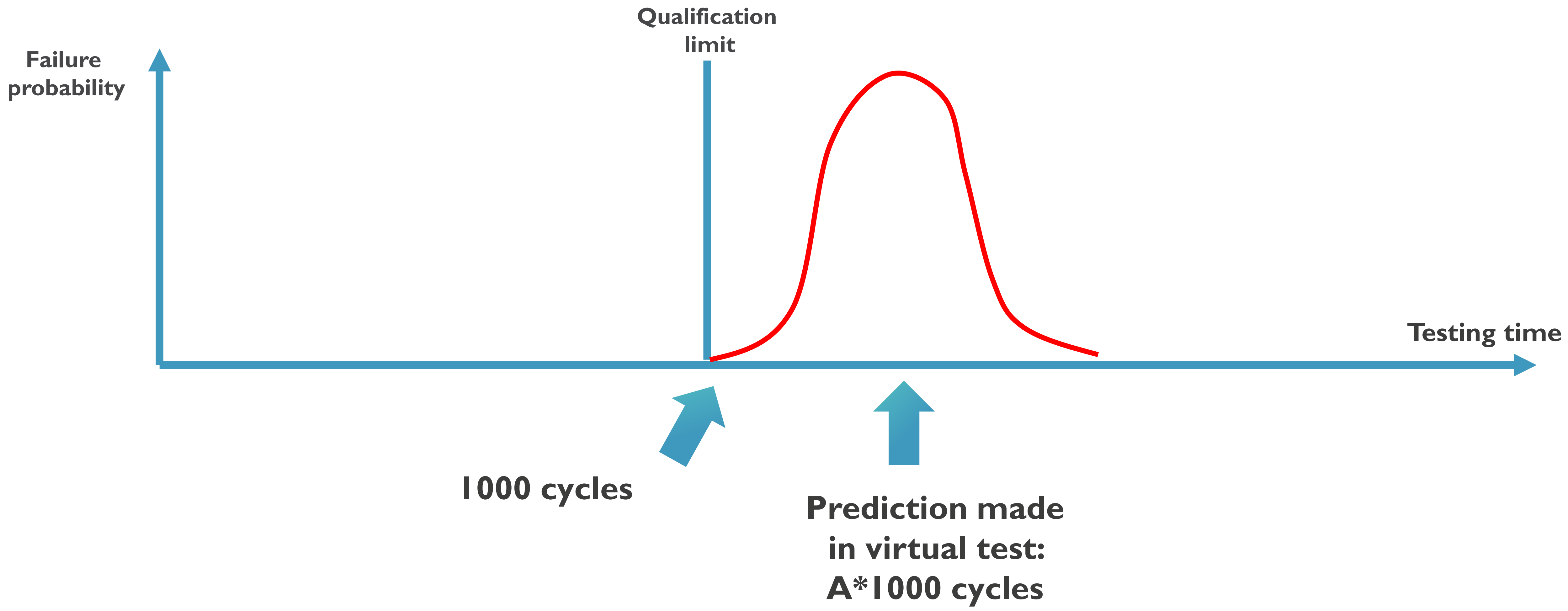
LIFE TIME ESTIMATION OF SOLDER JOINTS BASED ON EMPIRICAL CRACK PROPAGATION MODEL

- Empirical model defines how much the crack propagates in each temperature cycle



This model allows to cope with large area solder joints which takes many cycles till full fracture

DIFFERENCE BETWEEN QUALIFICATION TARGET AND LIFE TIME PREDICTION

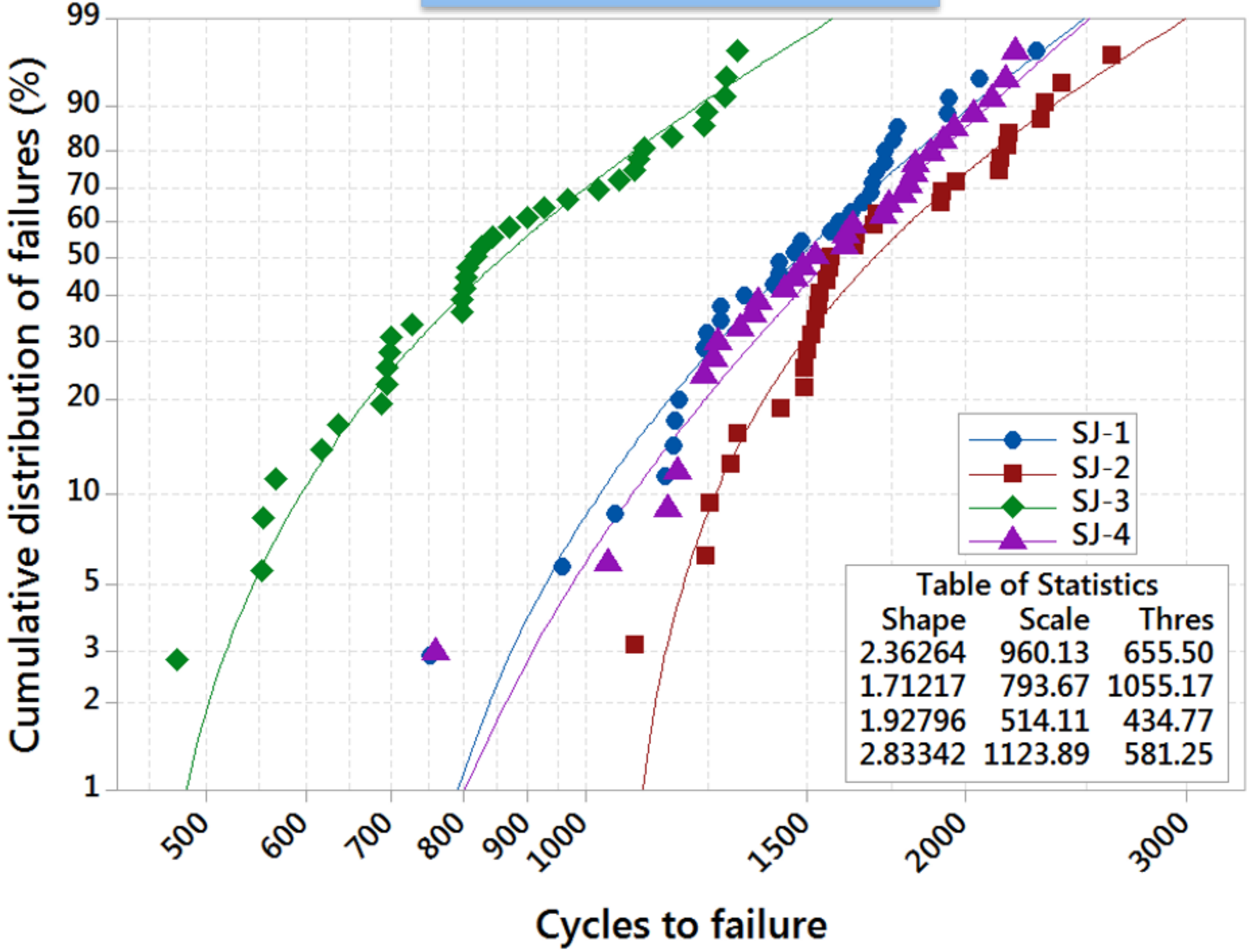


We need to have a minimum life time prediction higher than the 1000 cycles in order to pass the qualification test

DETERMINING THE SAFETY MARGIN A FOR SOLDER FATIGUE

RELIABILITY DATA FROM ACCELERATED THERMAL CYCLING TESTING

Three parameter Weibull

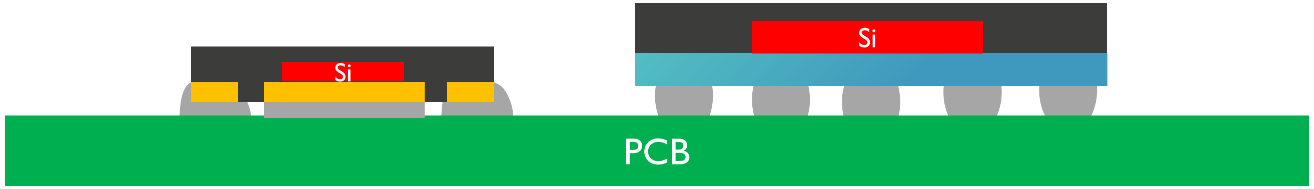


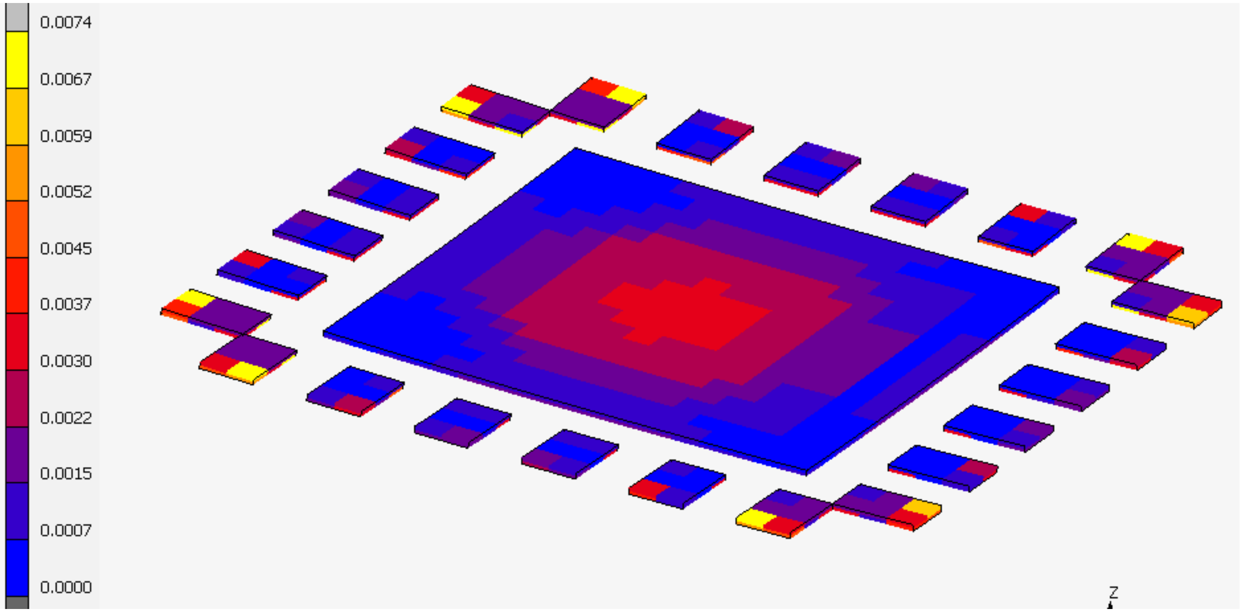
#	Failure Free Time	$N_{63\%}$	A
SJ-1	656	1616	2.5
SJ-2	1055	1849	1.8
SJ-3	435	949	2.2
SJ-4	581	1705	2.9

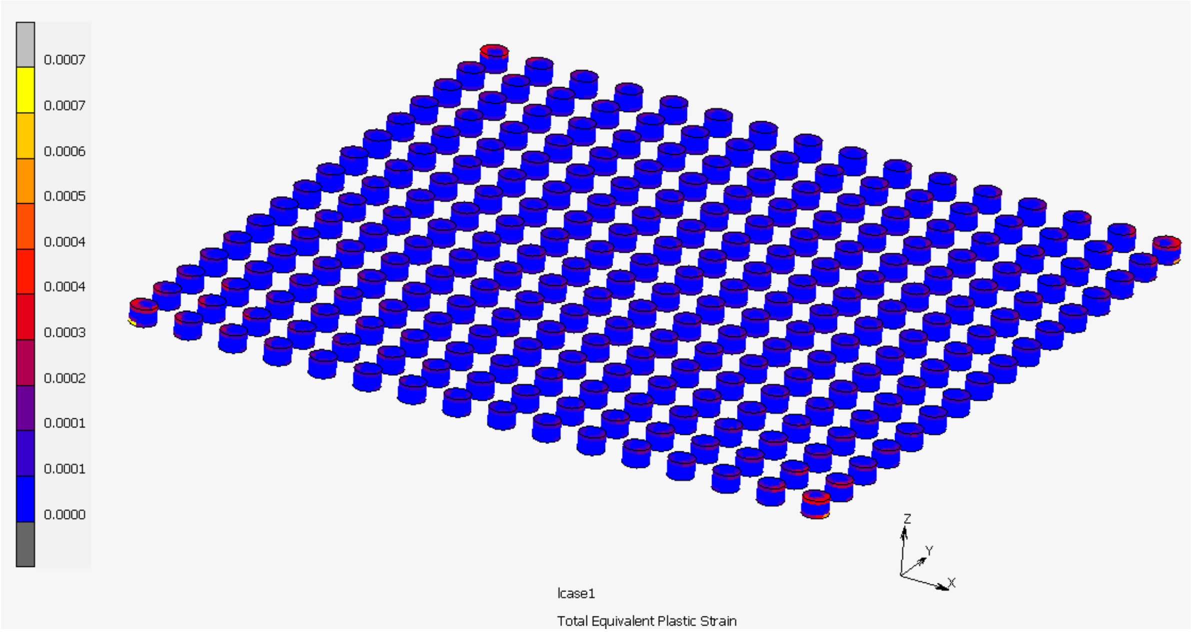
Safety margin A = **3**

THERMAL CYCLING OF **COMPONENTS ON STANDARD 1.6MM BOARD**

REFERS TO THE TYPICAL QUALIFICATION DONE BY COMPONENT SUPPLIERS





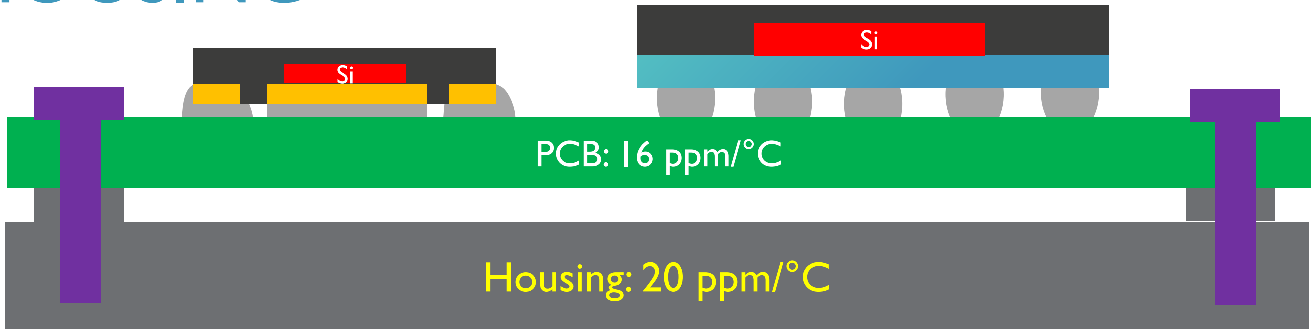


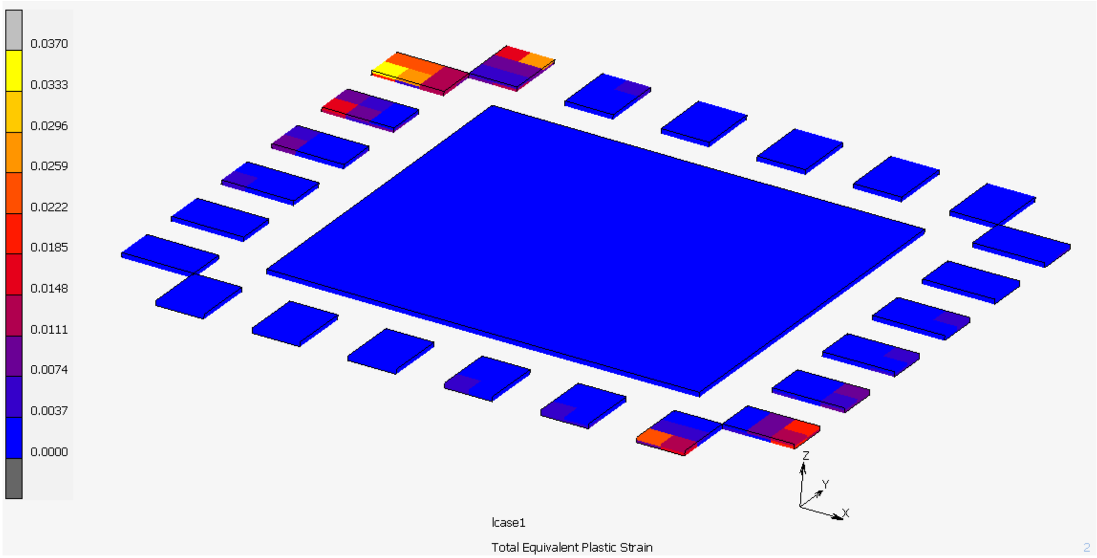
N63% = 3930 cycles to failure

N63% = >10000 cycles to failure

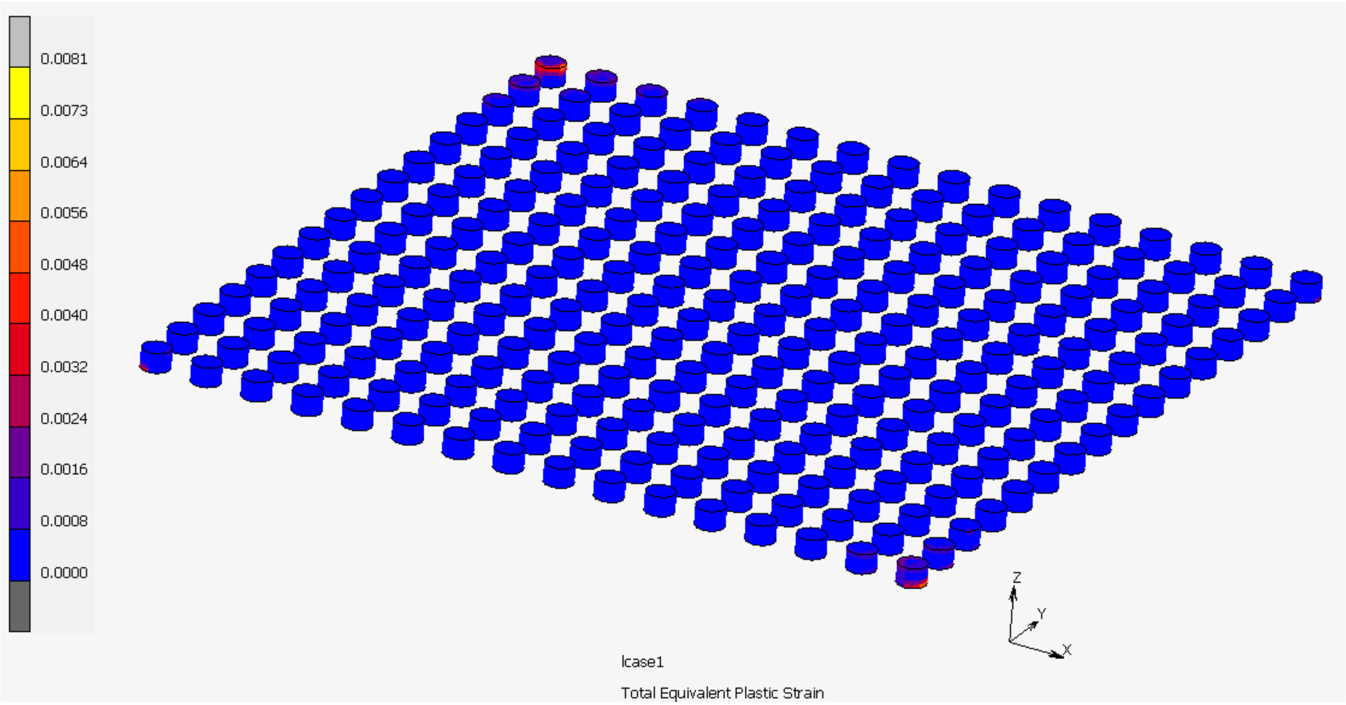
Temperature Cycling on Board	JESD22-A104 Test Condition G : -40°C to +125°C 500 cycles Preconditioning per JESD22-A113 MSL3	22 x 3 lots	Pass

THERMAL CYCLING OF PRODUCT = APPLICATION BOARD MOUNTED IN HOUSING





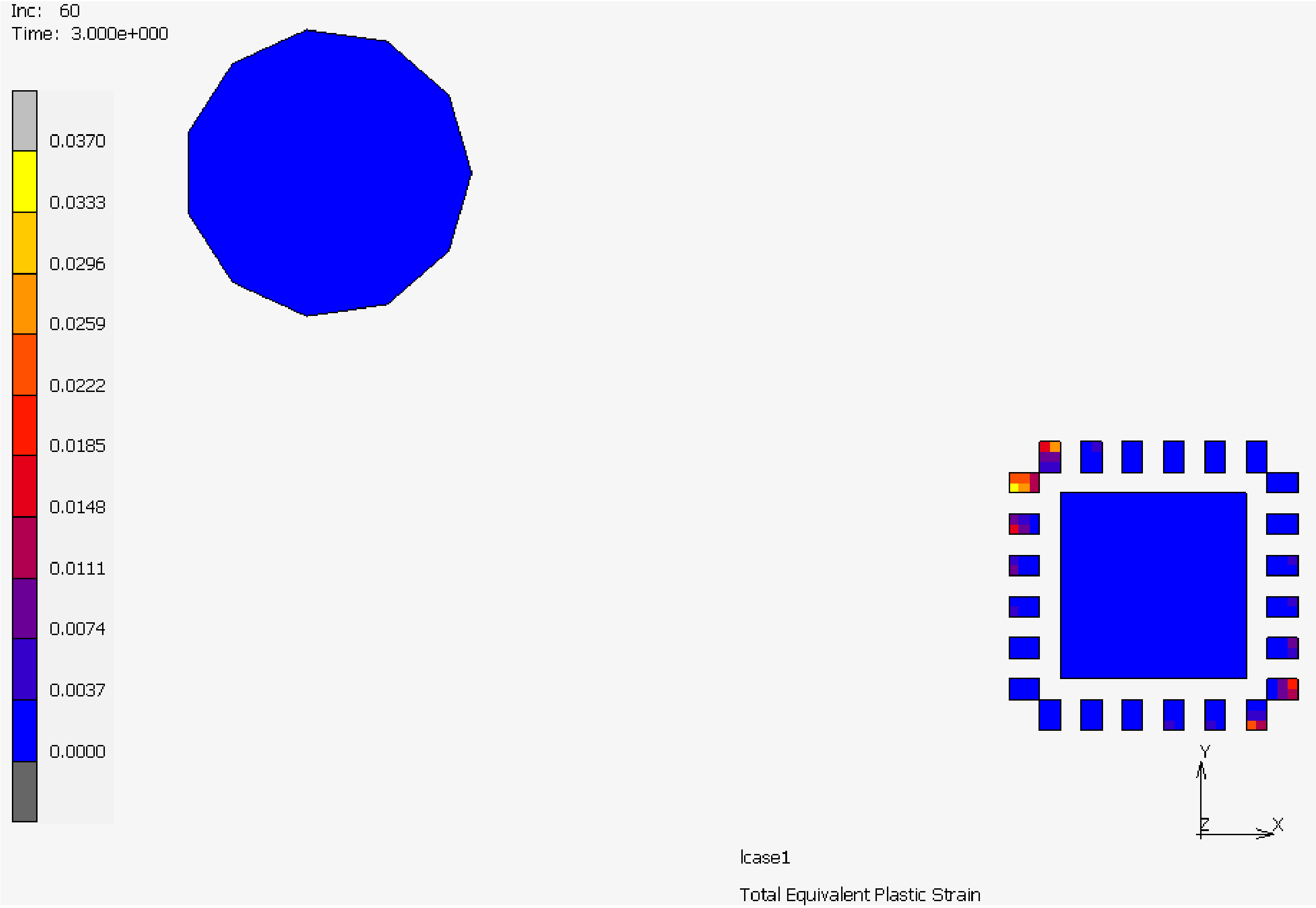
N63% = 1140 cycles to failure



N63% = 3600 cycles to failure

THERMAL CYCLING

INELASTIC STRAIN PER CYCLE IN QFN SOLDER JOINTS

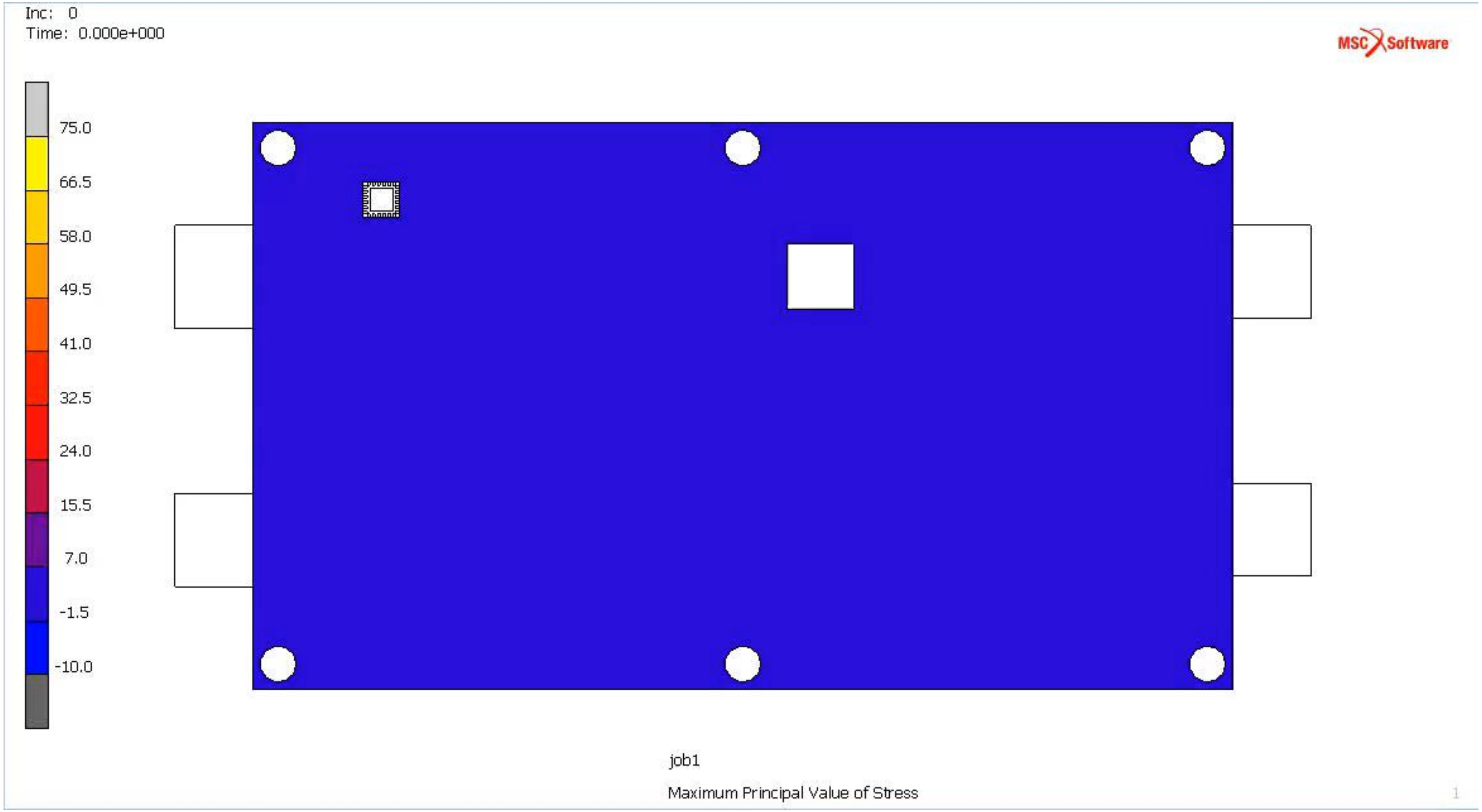


Strain per cycle: 3.7%

N63% = 1140 cycles

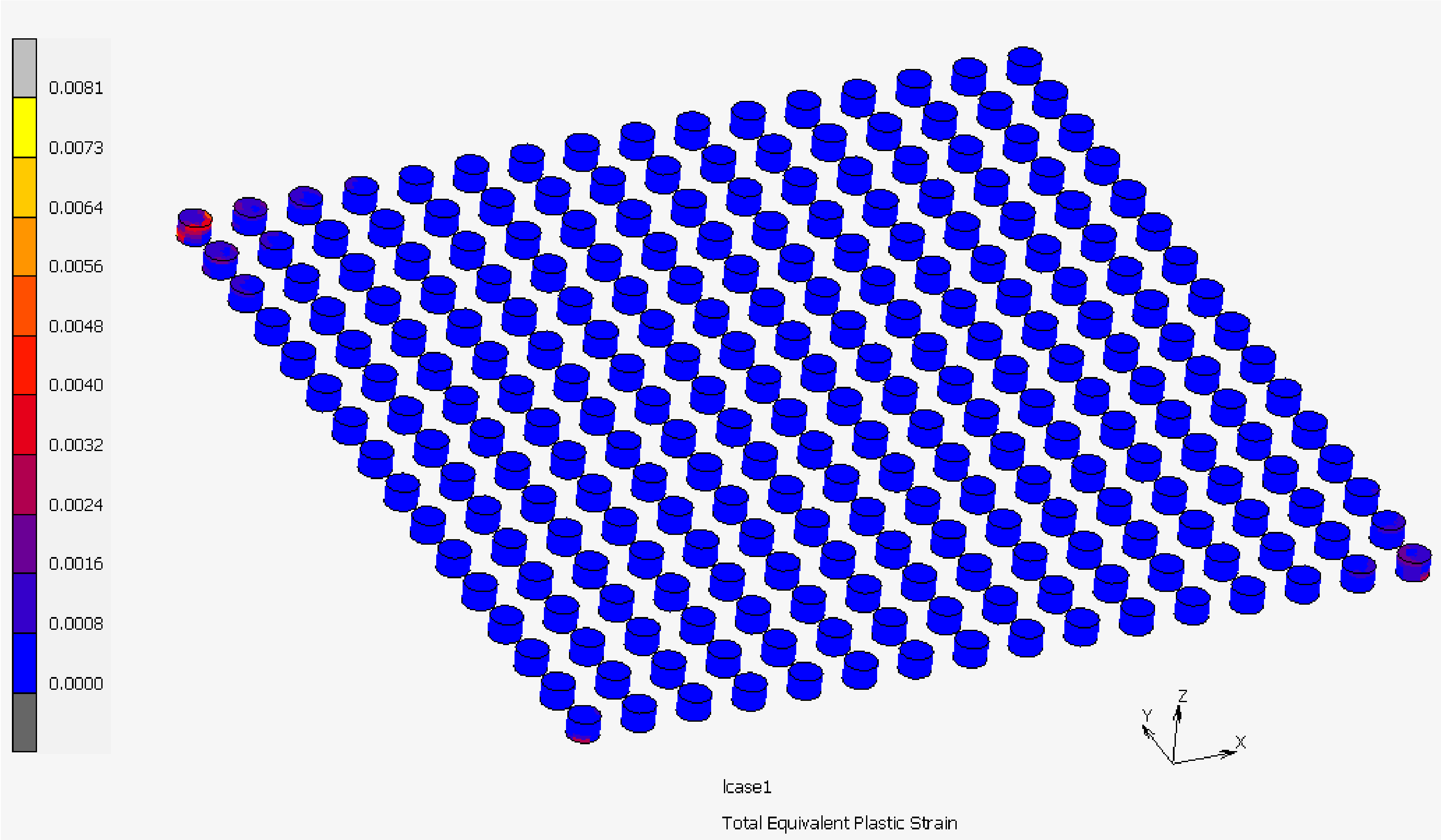
THERMAL CYCLING

STRESS EVOLUTION IN THE PCB



THERMAL CYCLING

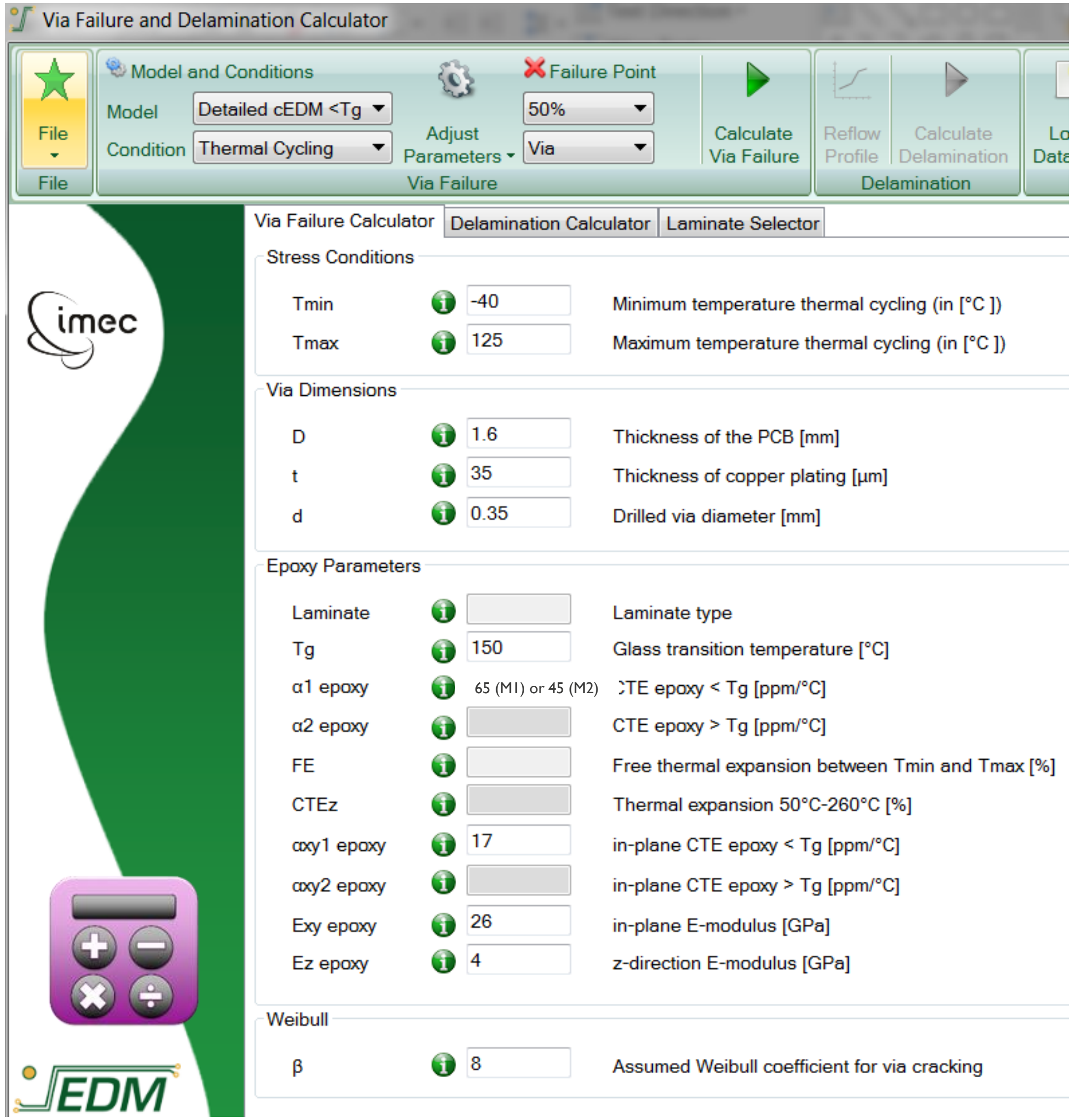
INELASTIC STRAIN PER CYCLE IN BGA SOLDER JOINTS

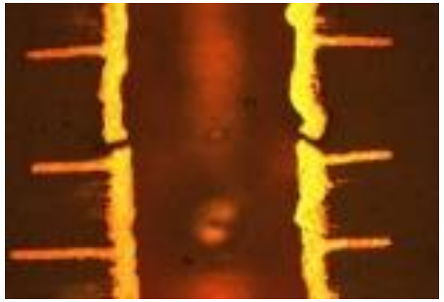


Strain per cycle: 0.81%

N63% = 3600 cycles

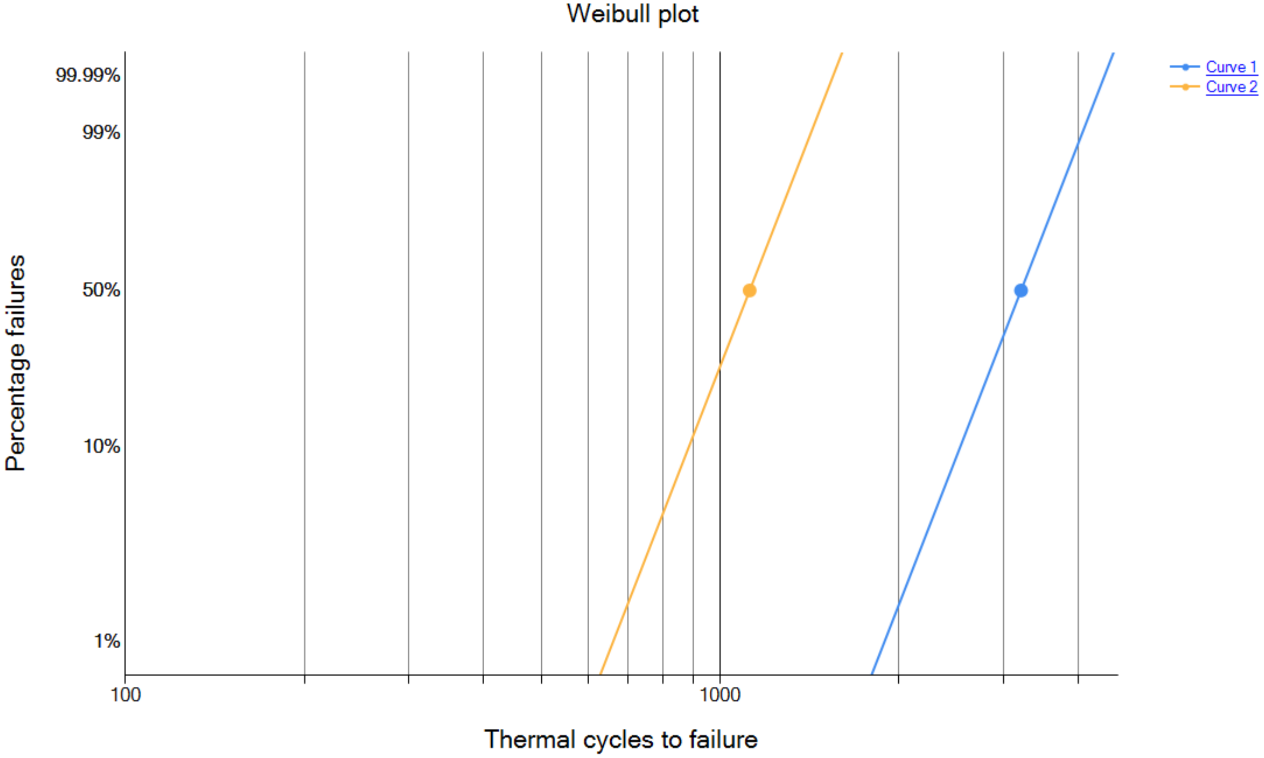
PLATED THROUGH HOLE VIA'S





FR4 material 1

FR4 material 2



SIMULATION OF VIBRATION LOADINGS

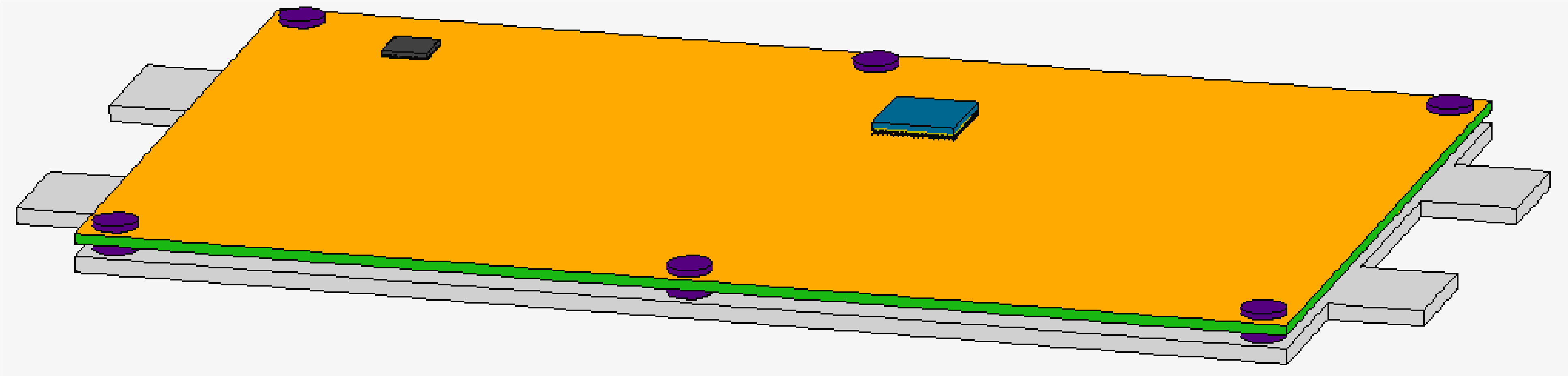
NO NATURAL EIGEN FREQUENCIES BELOW 200HZ

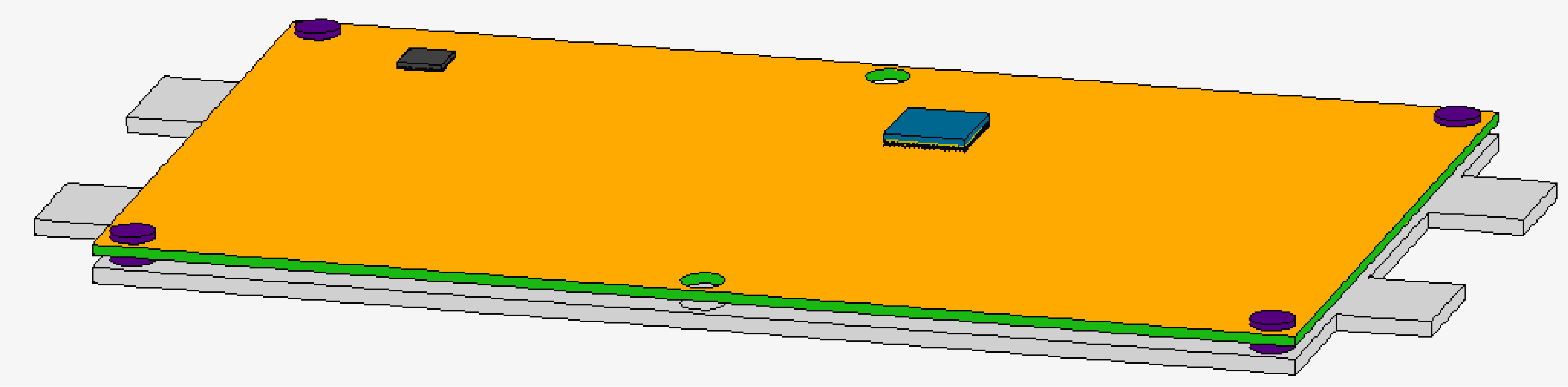
MODAL ANALYSIS TO FIND THE EIGEN FREQUENCIES

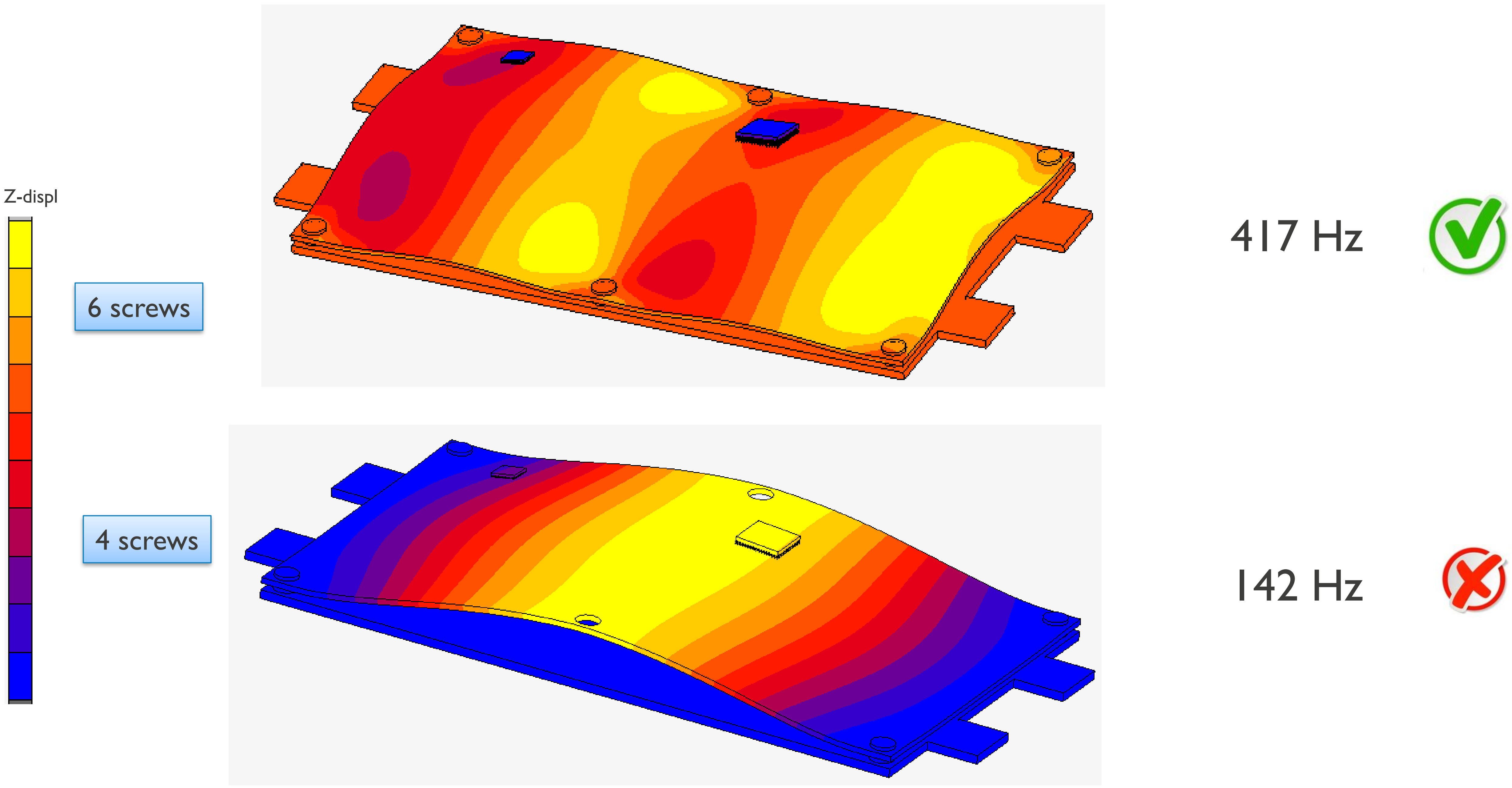
Modal analysis = Defining the first three natural frequencies

Good practice:

- First, to be avoided that natural frequency is agitated by surrounding environment
- Increase the first natural frequency of the circuit board, which will decrease the board displacement and curvature. In general, higher natural frequencies of the system result in low displacements and a greater resistance to vibration loads.
- Increasing the natural frequencies can be accomplished by stiffening the PBA, decreasing the weight of the PBA, or by changing the way the PBA is supported in the electronic box.



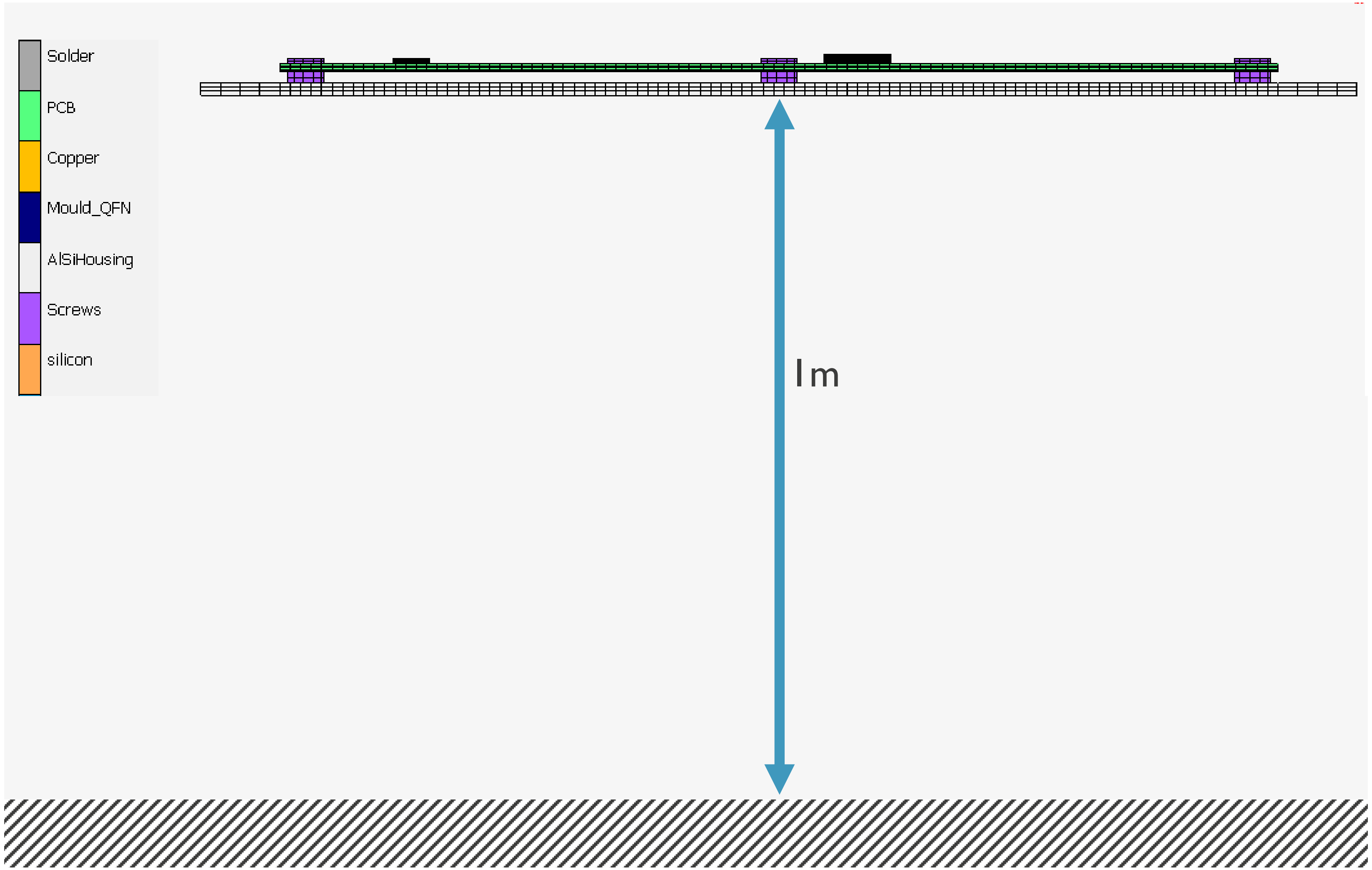



Z-displ
6 screws
4 screws
417 Hz
142 Hz

SIMULATION OF SHOCK TESTS

1 M DROP

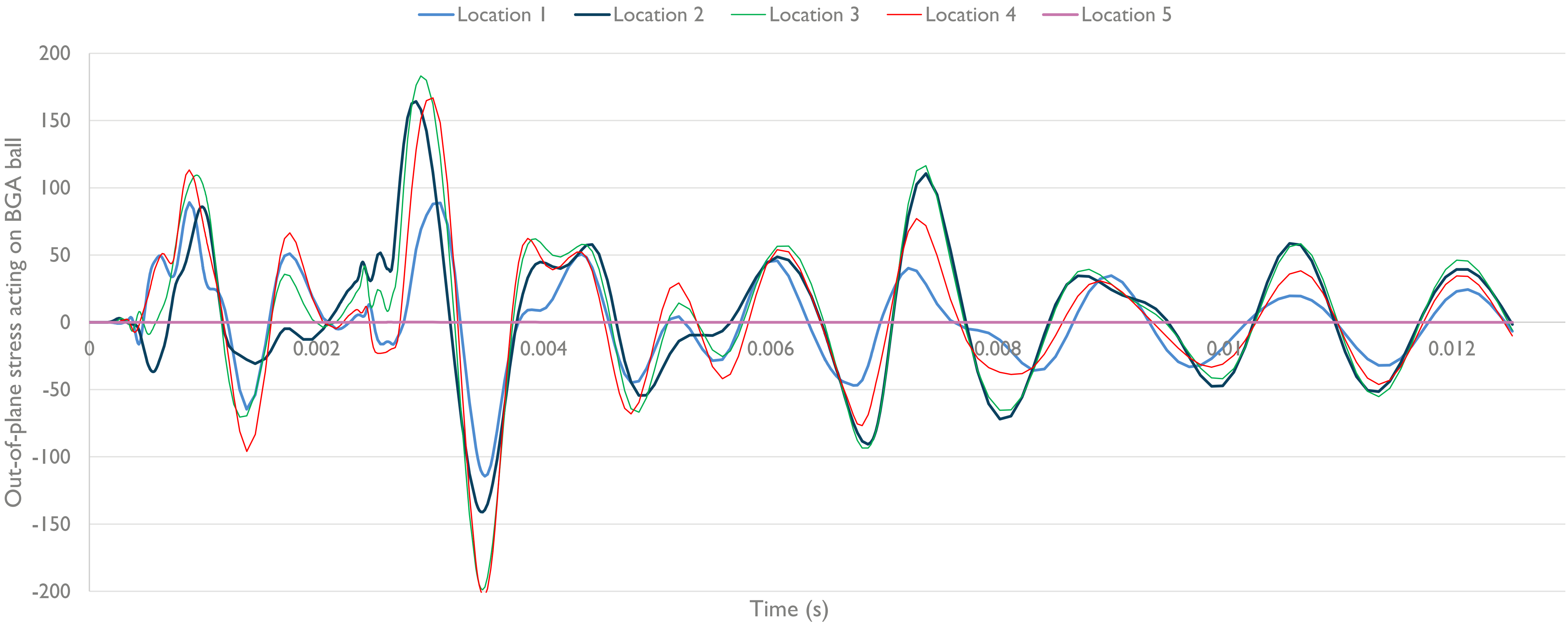
REPRESENTATION OF 1M DROP TEST



Sample has a velocity of **4.4 m/s** when it touches the ground

RESULTS

STRESS IN THE **SOLDER JOINTS** IN THE FOUR CORNER LOCATIONS + CENTER OF THE BGA

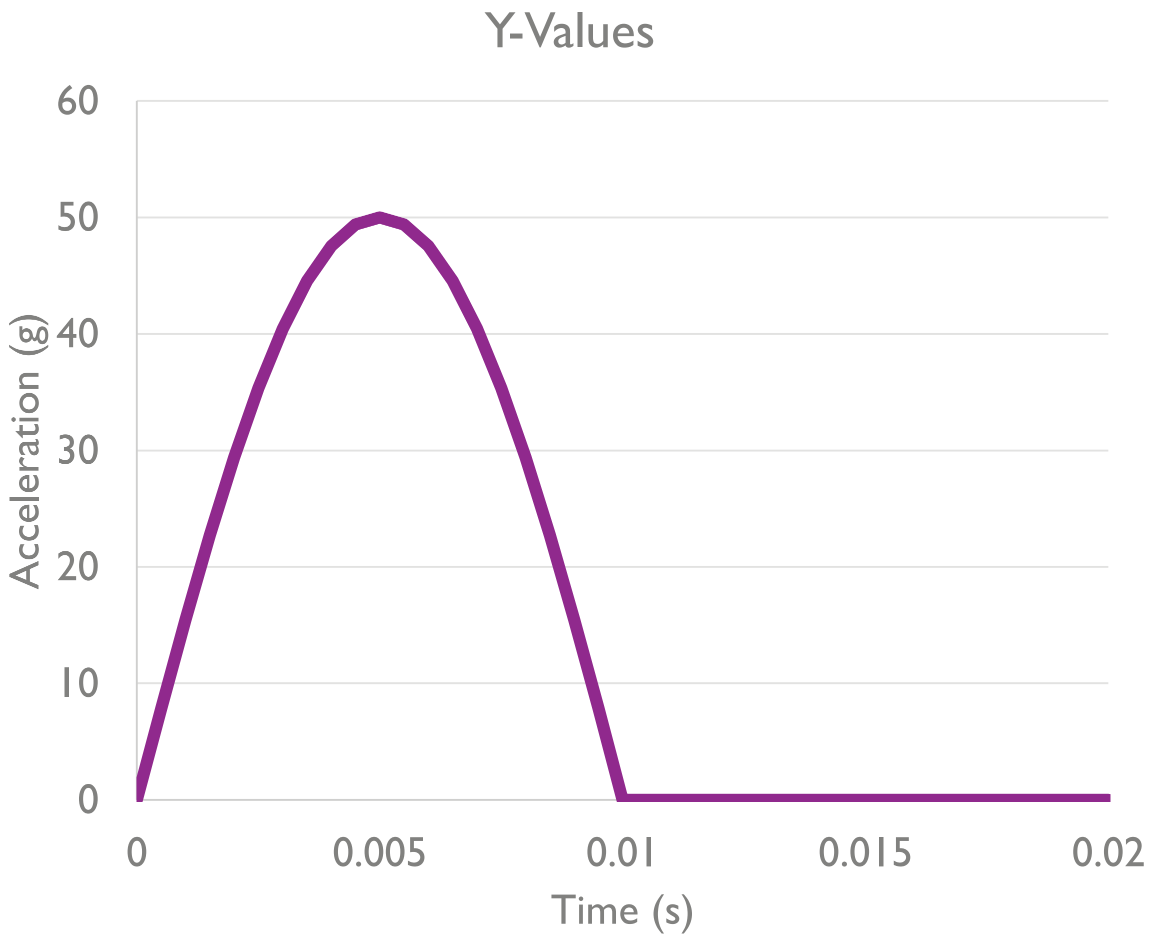


SIMULATION OF SHOCK TEST

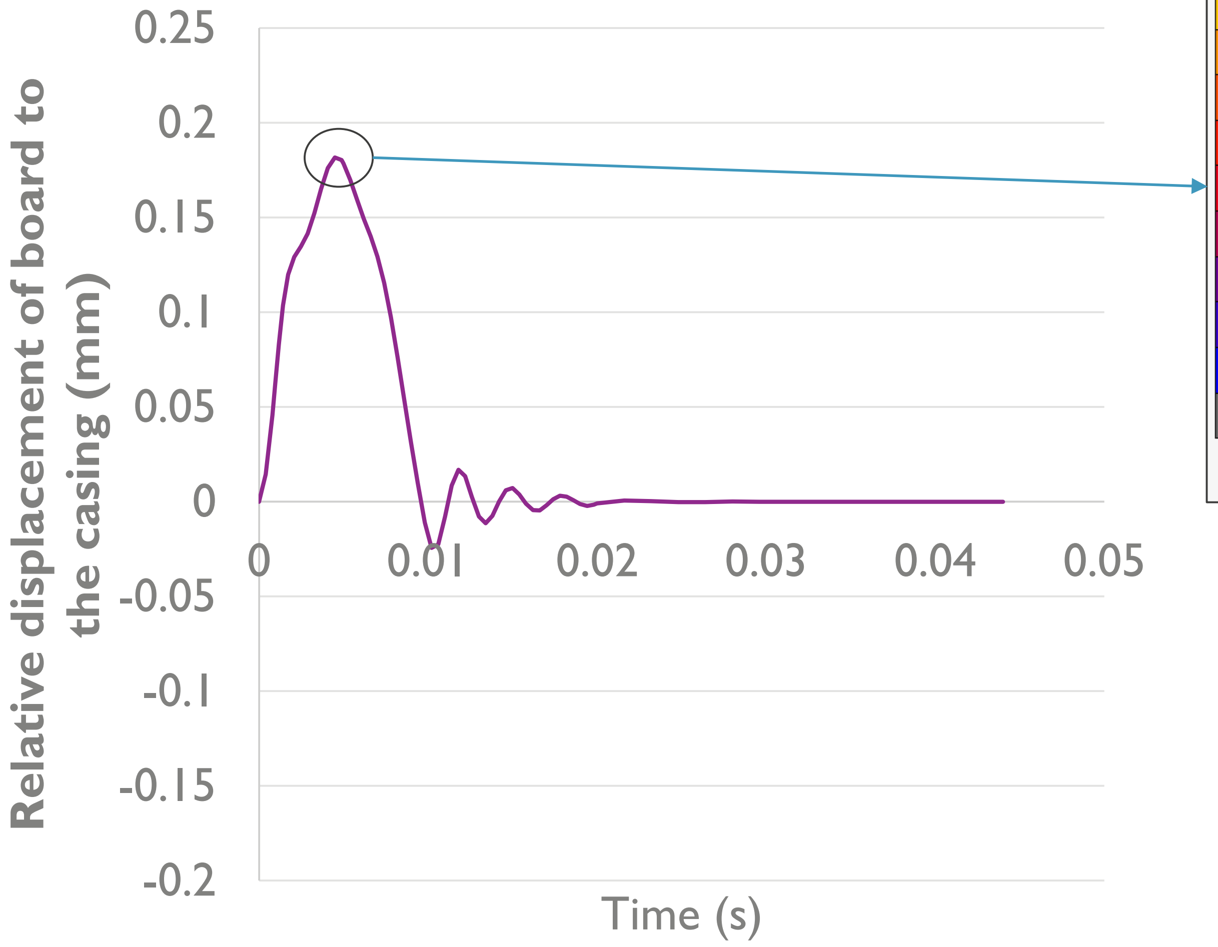
50G FOR 10 MILLISECONDS
100 SHOCKS

LOAD DESCRIPTION

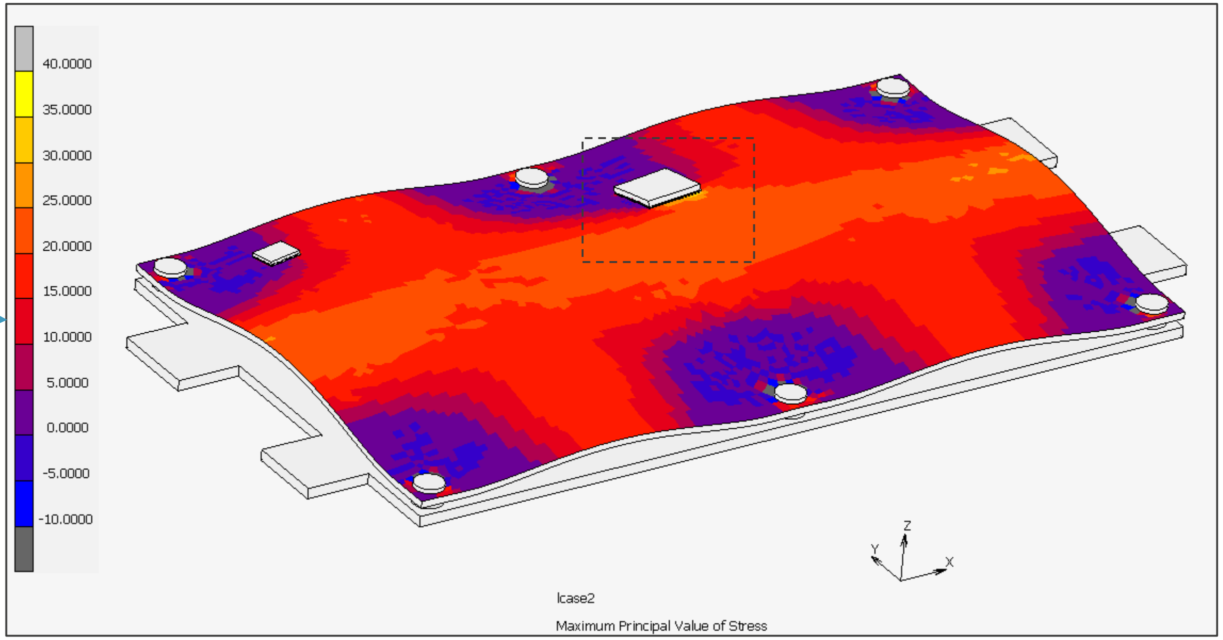
HALF SINE SHOCK: 50 G OVER 10 MSEC



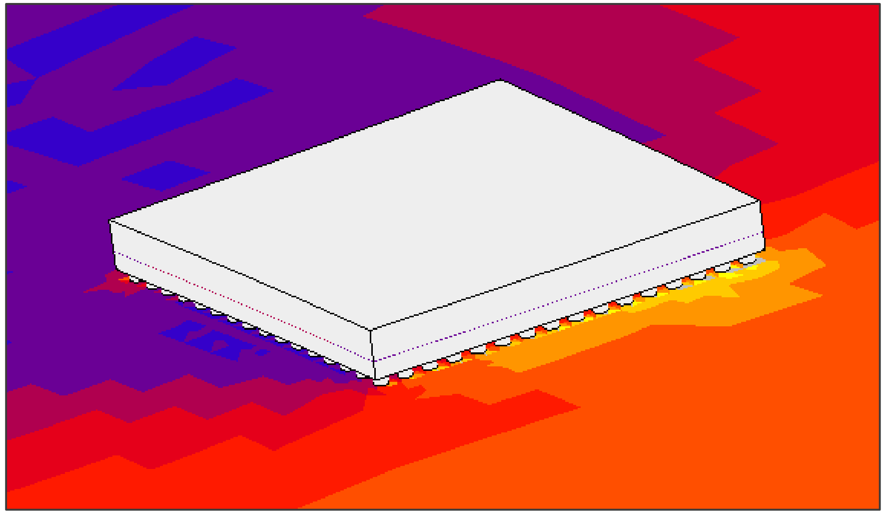
- A product shock response analysis is performed on each board to determine its displacement and maximum strain due to the shock pulses.
- The product shock survivability assessment compares the maximum displacement and strain to an empirically-based maximum allowable out-of-plane displacement and acceptable board strain.
- The results are given in likelihood of failure.

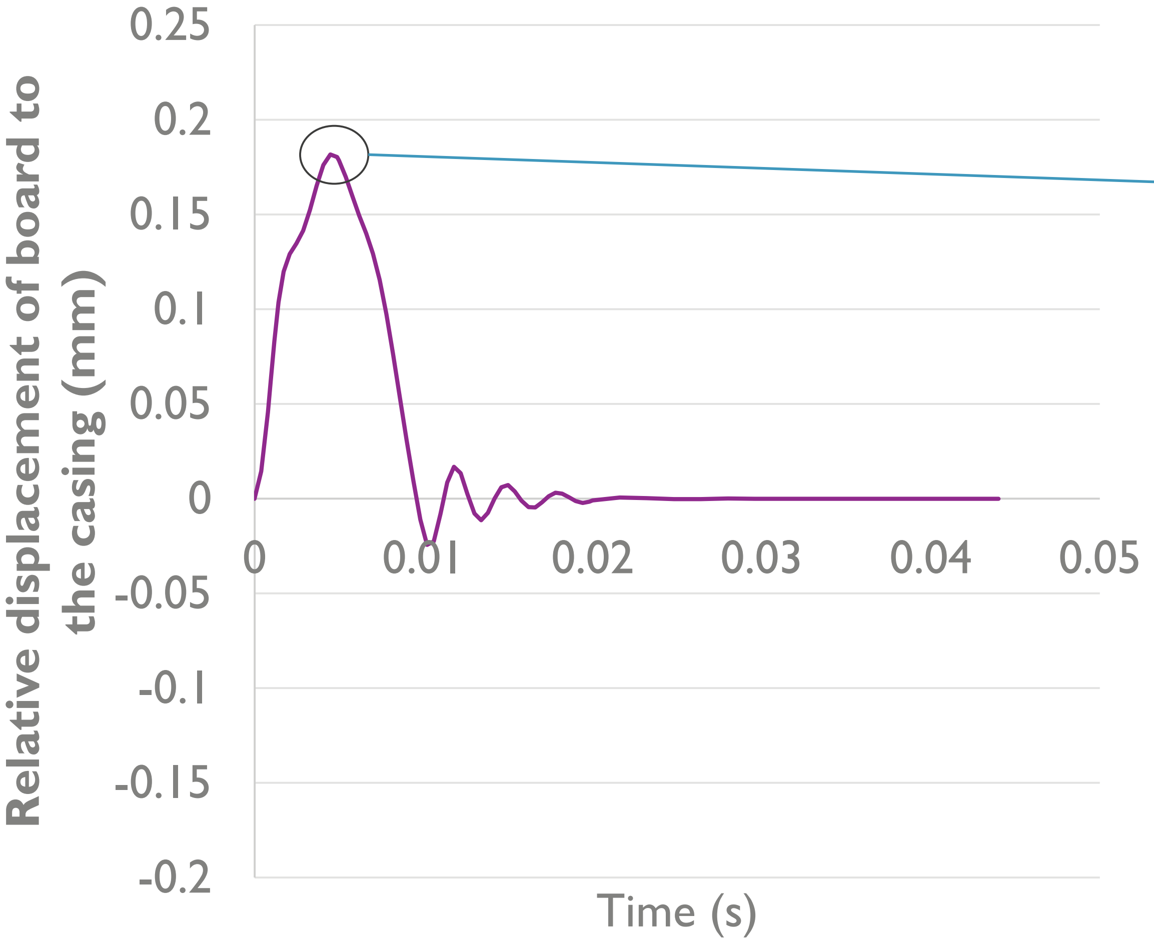


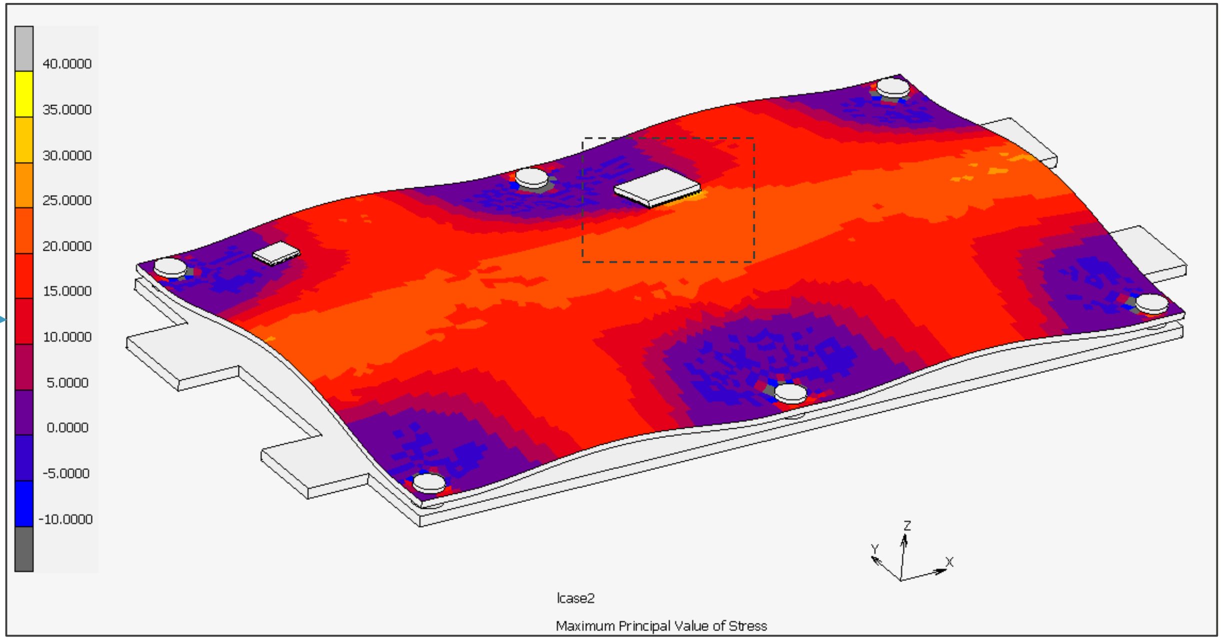
Relative displacement of board to the casing (mm)
0.25
0.2
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-0.2
0
0.01
0.02
0.03
0.04
0.05
Time (s)



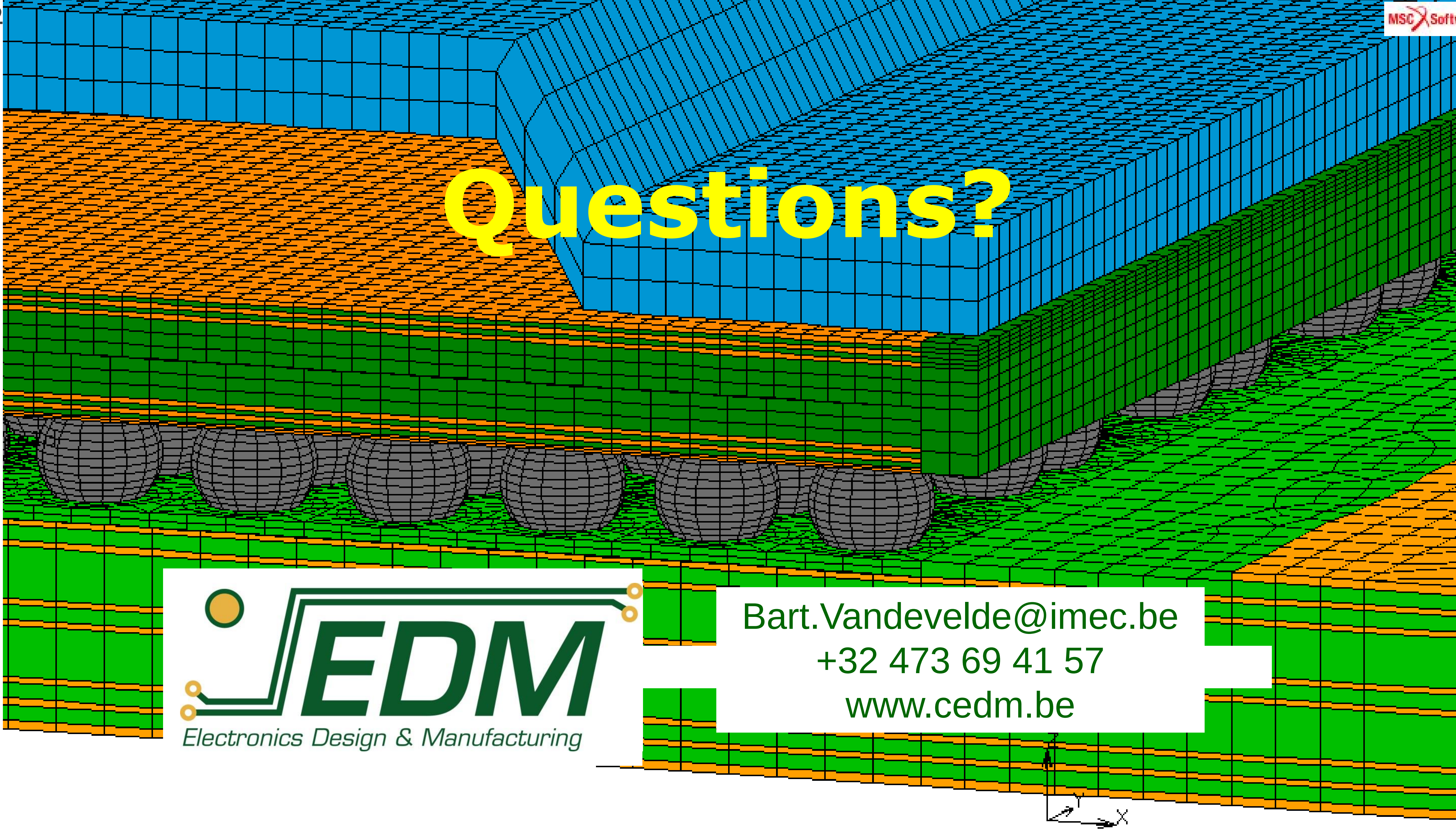
40.0000
35.0000
30.0000
25.0000
20.0000
15.0000
10.0000
5.0000
0.0000
-5.0000
-10.0000
Z
Y
X
lcase2
Maximum Principal Value of Stress







Almost **zero plastic deformation** in solder joints
→ Components will easily pass this test



Questions?

CEDM
Electronics Design & Manufacturing

Bart.Vandevelde@imec.be
+32 473 69 41 57
www.cedm.be