Wearables & IOT – The next challenge

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2nd June 2015

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Outline

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- Introduction
- Aesthetics and Packaging
- Battery Life and Power Consumption
- Security
- Summary

Cambridge Silicon Radio – *“15 years delivering low power solutions to the consumer and automotive markets.”*

Imaging

Automotive Infotainment

Bluetooth® Smart

Voice & Music

Indoor Location

Five Platforms for Growth

Segments

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Peripherals

- Fixed Purpose
- Always ON, targeted experience
- Connectivity : BT/BTLE
- Battery Life : ~7days
- RTOS based
- Architecture-ARM Cortex-M
- Highly integrated signal processing



Wearable computing devices

- Multipurpose
- High Performance/rich user experience
- Drive for memory requirements
- Multimedia Rich –graphics, audio etc.
- Battery Life : Everyday
- Multiple connectivity
- Full OS
- Architecture – ARM Cortex-A9
- Highly integrated SOCs

The Well Connected Man [& Woman ☺]

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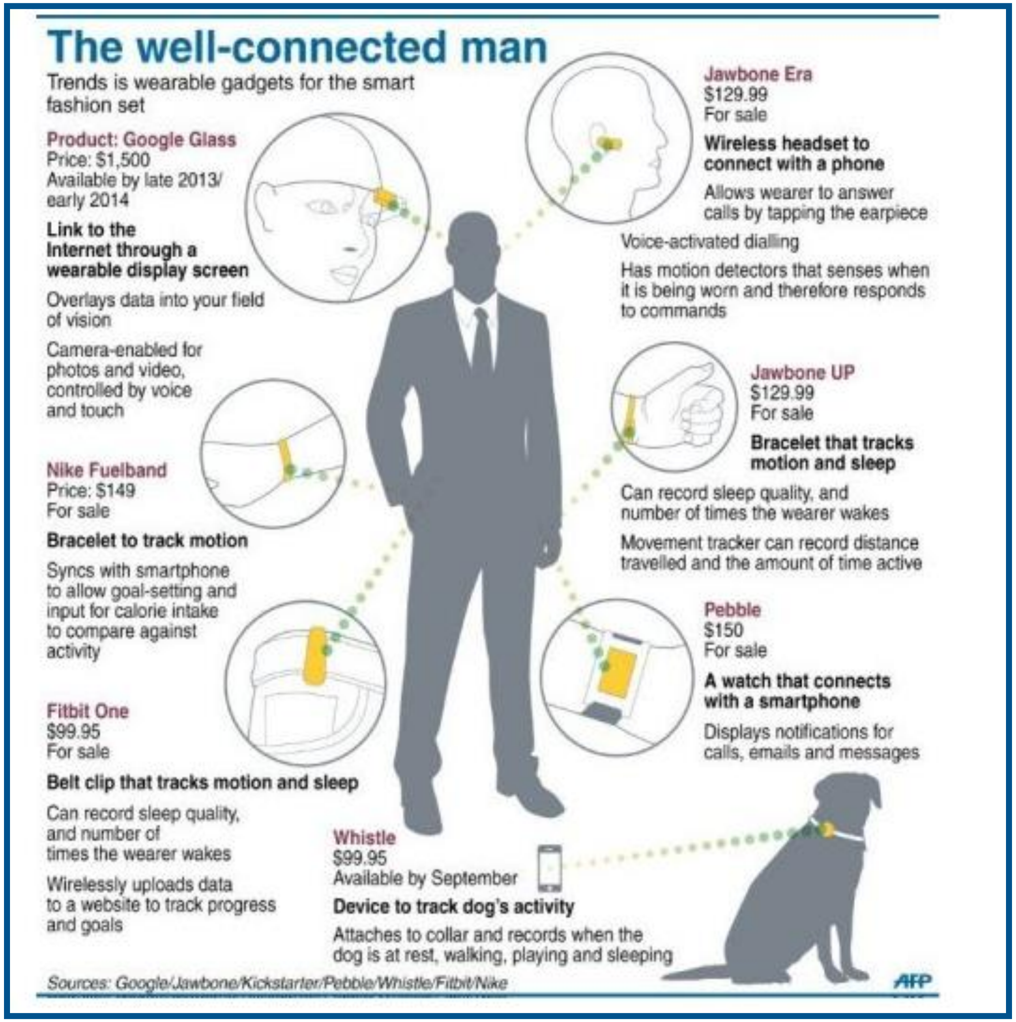
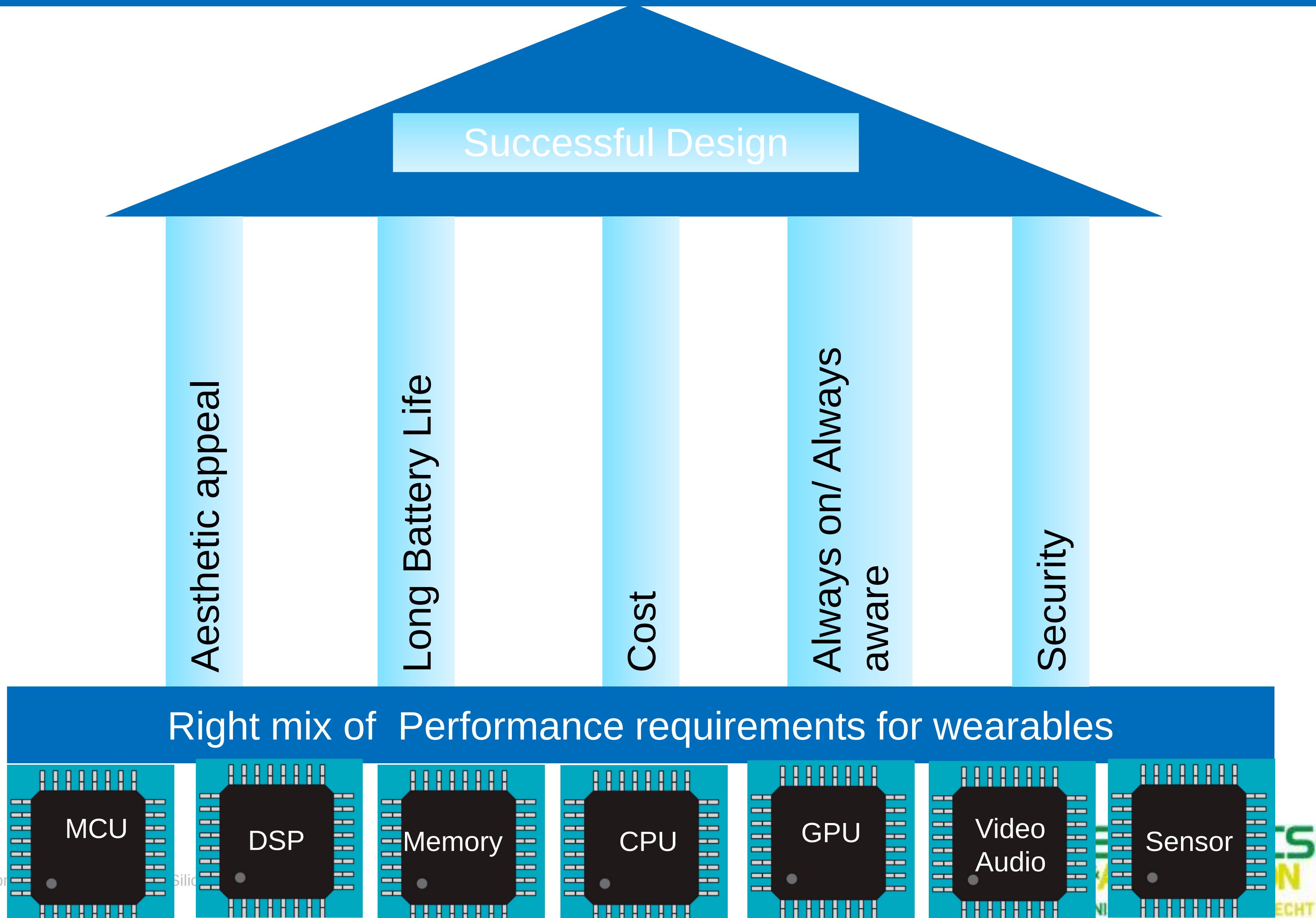


Wearable Computing Device Shipments by Category (Millions)

	2013	2014	2015
Wearable Cameras	6.64	13.61	15.81
Smart Glasses	0.01	2.13	10.57
Smart Watches	1.23	7.44	24.92
Healthcare	13.45	22.59	34.25
Sports/Activity Trackers	32.46	42.64	57.42
Wearable 3D Motion Trackers	N/A	0.87	2.00
Smart Clothing	0.03	0.72	1.24
Totals:	**53.90**	**90.00**	**164.20**

Source: Data from ABI Research World Market Forecast: 2013 to 2019

Pillars for successful wearable design



An example: MOBILE PHONE EVOLUTION

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The show off 80s | Must have 90s | The millennium smart era

10kg 1kg 800g 495g 500g 164g 133g 129g

£3k £2k £800 £539

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Wearables usage and design considerations

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User Usage

- 24/7
- Environment used in
- Wearables close to body
- Constantly ON
- Privacy protection

Design factors to consider

- Small form factor-sleek , thin, light
- Thermal aspect – need to be comfortable to the body
- Power management
- Privacy/security measures

Package technology

Si and process technology

IP offerings

Aesthetic Appeal & Packaging-

IF IT’S UGLY IT IS NOT WEARABLE

Package Technology

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- Component package
  - Thickness and footprint

- MEMS & Sensor package
  - One device, One process, One product
  - Package technology primarily dominate the final body size

- System in Package
  - Integration of above two package

Component Package

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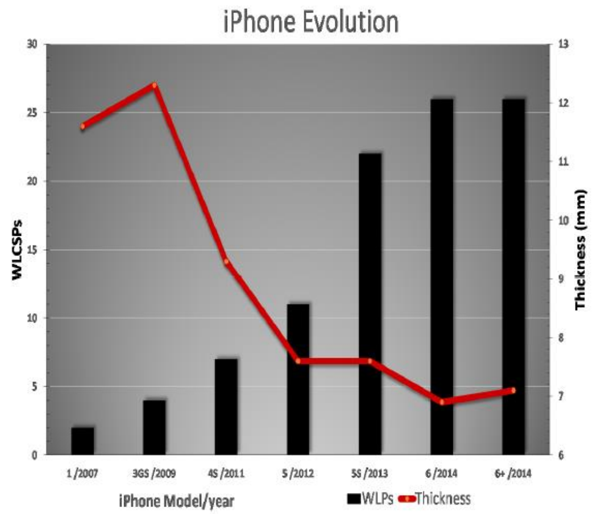
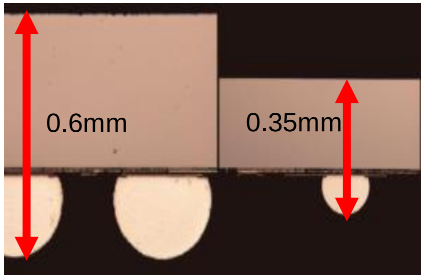
- Thin package technologies
  - WLCSP, QFN

iPhone 1 2007 2 WLPs | iPhone 3GS 2009 4 WLPs | iPhone 4S 2011 7 WLPs | iPhone 5 2013 11+ WLPs | iPhone 5S 2013 22 WLPs | iPhone 6 2014 26+ WLPs | iPhone 6 Plus 2014 26+ WLPs

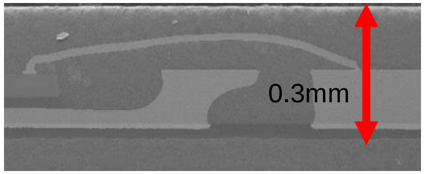


Source: TechSearch International, Inc., adapted from TPSS.



WLCSP

CSR production > 10yrs



QFN

Source: ASECL

Component Package

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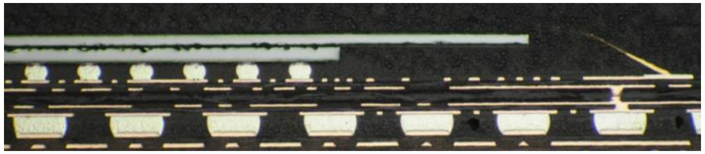
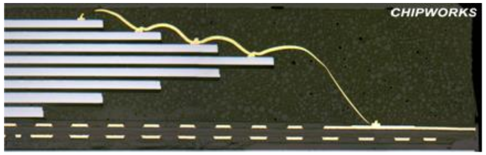
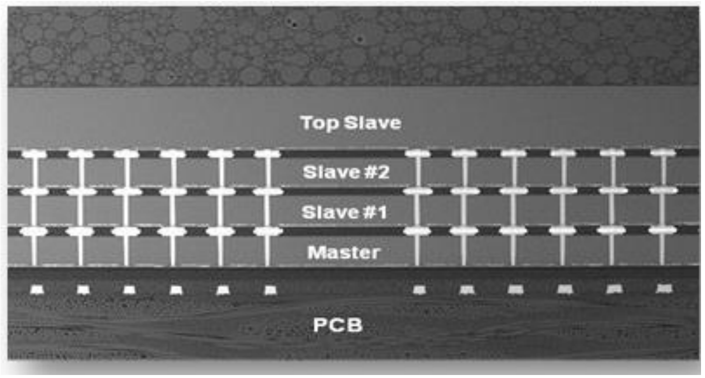
- Small footprint package technologies
  - Higher “Silicon density” in the package (die size/package size)
- Example of silicon density
  - WLCSP = 1
  - CSP package = 0.8 ~ 1
  - 2 dies stack CSP package = 1.6 ~ 2



Memory die stack on top of process



Samsung’s 8 Flash die stack



Samsung’s 3D STV technology

MEMS & Sensor Package

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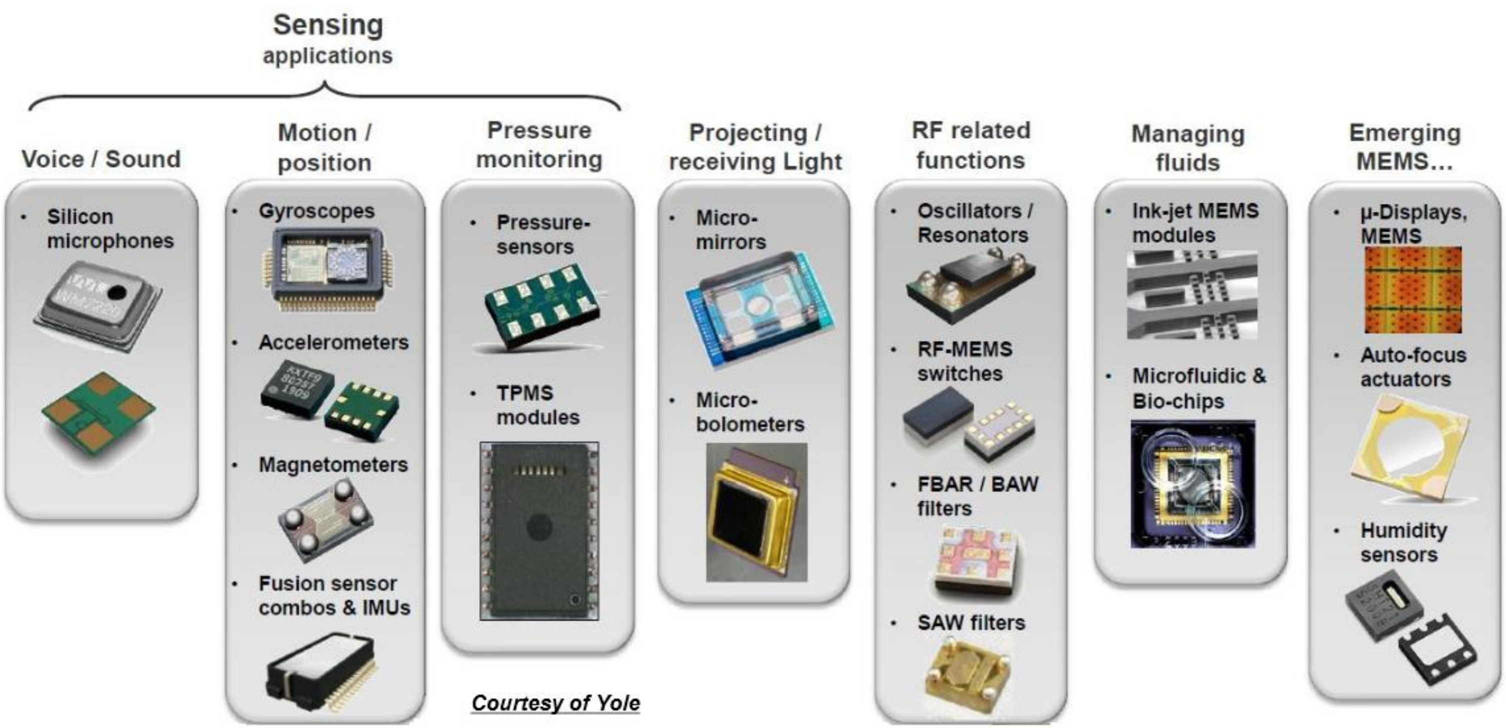
- Diversified & non-standardized package solution required
  - Problem: “One device, One process, One product”



MEMS & Sensor Package

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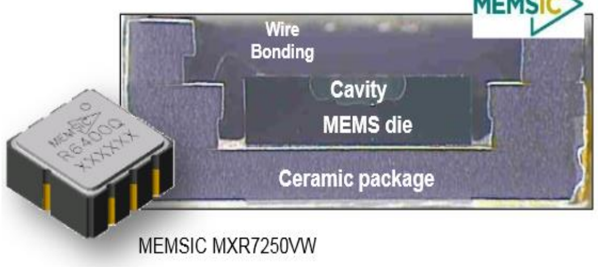
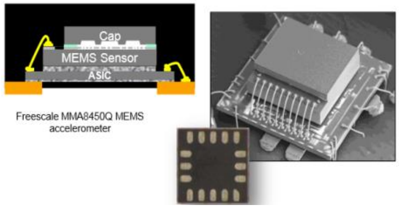
- Package technology primarily dominate the final body size

  Ex: Accelerometer package size reduction

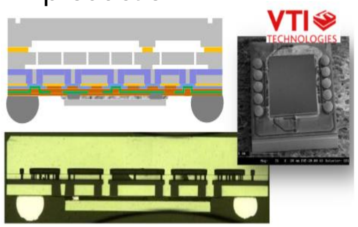
Ceramic package



Die stack in QFN package



First true 3D WLCSP package in production



Courtesy of System Plus Consulting

System in Package

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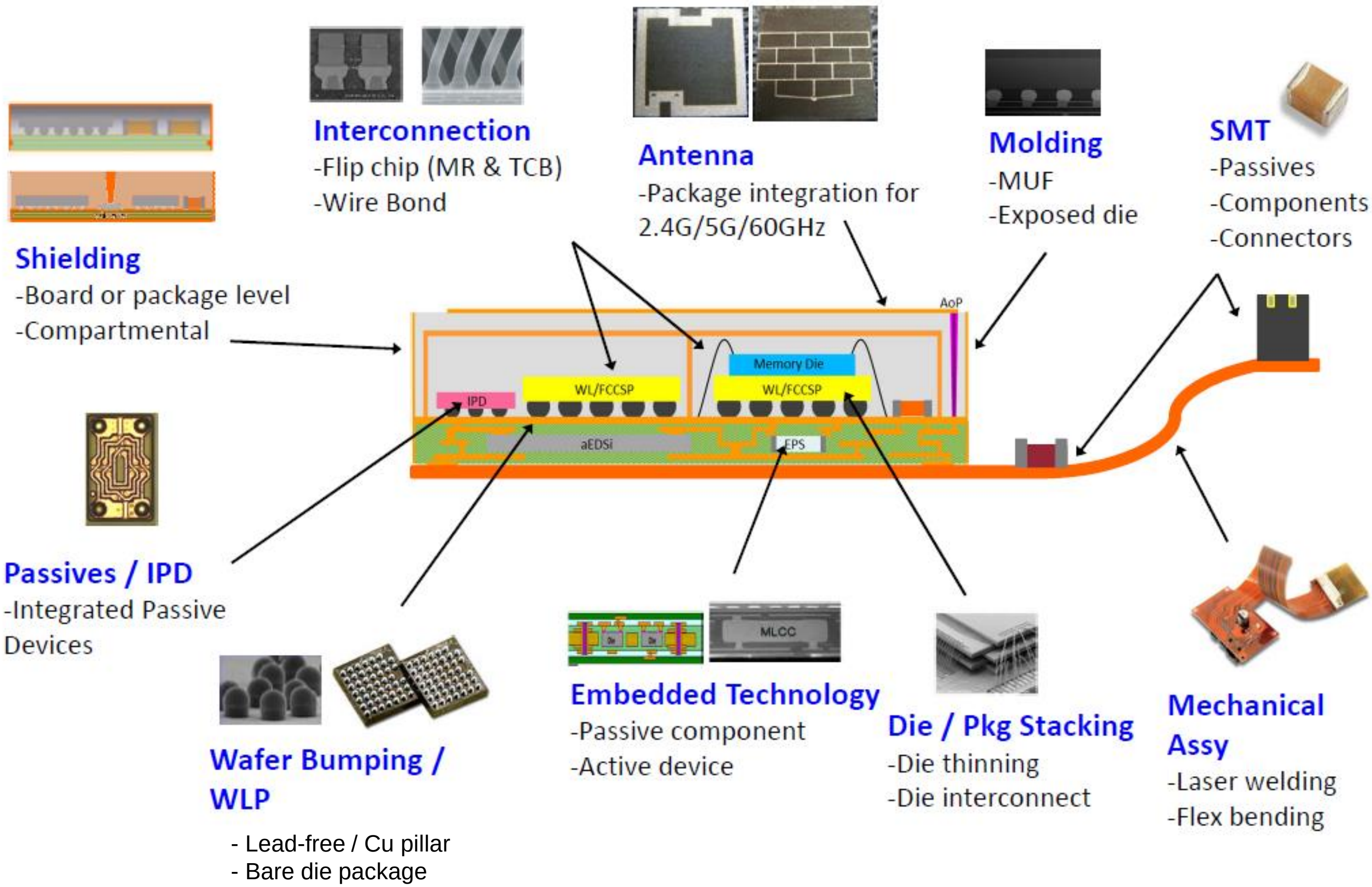
- Enabling technologies



Courtesy of ASE

System in Package

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- EX: Apple Watch S1 SiP
  - 8 layers microvia substrate with 50um L/S, and 360um thickness
  - Many packages, primarily CSP and numerous passives
    - All have a mounted height of 400um or less
  - Advanced EMI shielding technology to reduce the SiP body size
  - The entire package mounted height is 550um

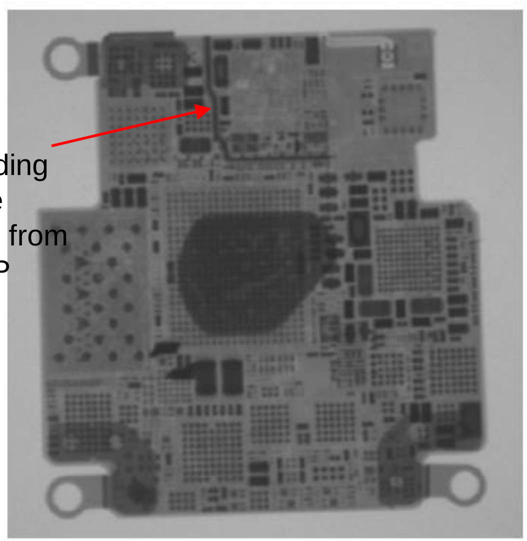
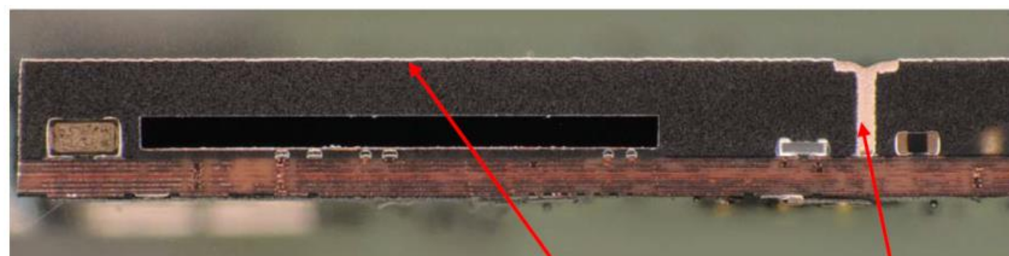


Photo source: Prismark/Binghamton University



Source: Prismark

In Summary on Packaging …

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- Components – drivers are form factor and height
- Same careabouts in MEMS technology with the additional challenge that there are multiple package types
- A great variety of SIP offerings but these are likely to shrink as the market matures and finds its way

- The backstory to all of these is the cost curve
- This will come from volume and never “reinventing the wheel”

Battery Life
& Power consumption

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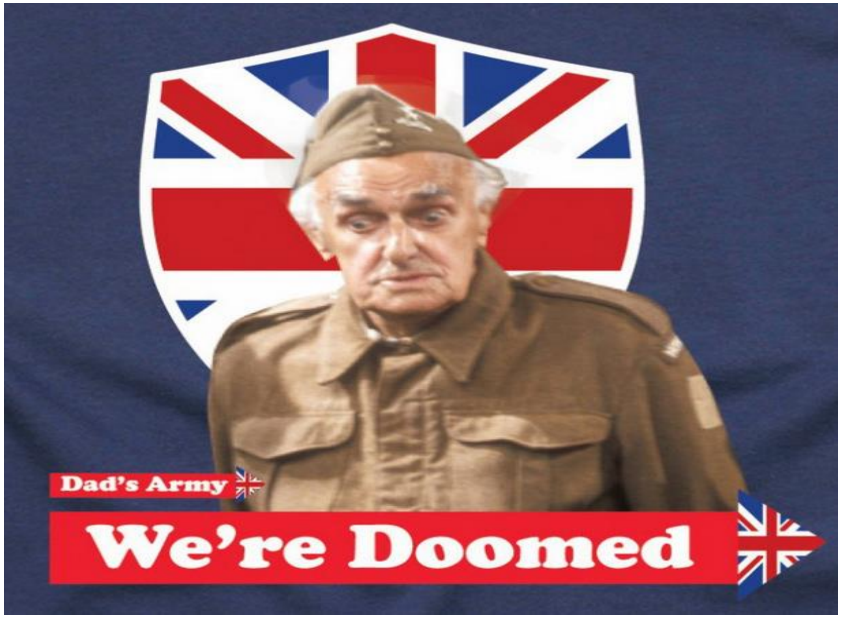
- RF connectivity during ON state are always power hungry
- Increased demand in memory space on chip (ie more RAM) give burden on batteries life
- Always ON sensors and display units consume lots of power

- Battery technology didn't evolve as quickly as we like to …

SO?



THE NEED FOR BATTERY AND CHARGING INNOVATION

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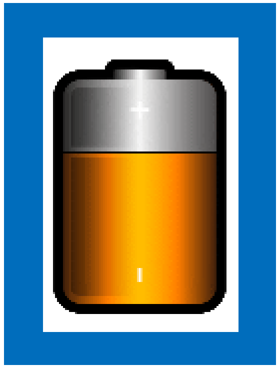

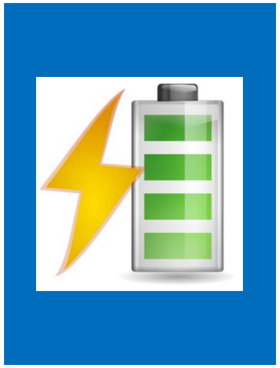

- **Today: Li-Ion technology. The battery size ~50% of the total footprint today.**
- **Density/capacity of battery ~ 300mAH. Restricted density. Need constant charging for high end wearables – user experience compromised**
- **New technology in batteries?**
  - **Silicone Anode**
  - **Ge nonowire**
  - **Carbon flouride-for LP application wearables**

- **Today: Wired Micro USB charger**
- **New technology in charging?**
  - **RF wireless energy harvesting**
  - **Photovoltaic**

Don’t expect changes to battery and charging technology overnight…..
So can we do something innovative from design aspect of component level?

What can we do to save power?

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- Clever radio architecture can significantly reduce the active power
- Reduce the operational voltage of the system
  - Operate as many blocks as possible at a lower voltage
  - An integrated power supply is needed so that the voltage can be dynamically adjusted
- Frequency reduction
  - Operate the chip at lower frequencies, gives a linear reduction in dynamic power
- Use transistors with lowest available leakage in the process
- Avoid external components that waste power
  - External Li-Ion regulators for example reduce overall system efficiency
- etc.

This section focuses on Process Technology Improvements

Transistor Leakage Across Nodes

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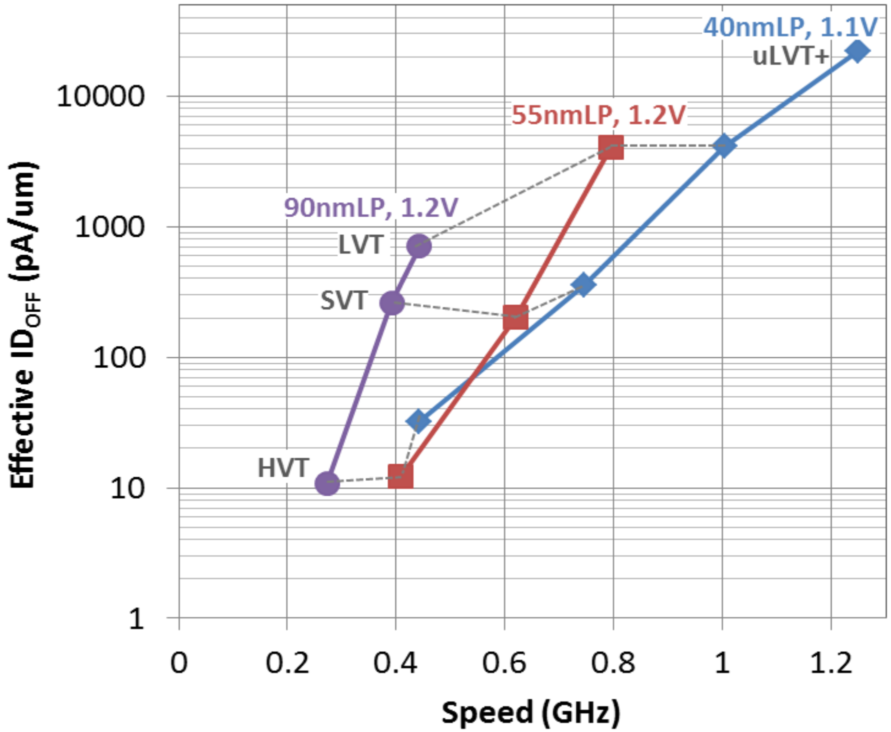

- Advanced CMOS transistors are optimized for higher speed and lower active power but the lowest achievable leakage is usually higher than the previous node
- Battery life is key for BT Smart as chips spend much time in standby, making leakage reduction essential
- 40ULP was conceived based on the requirements

Pocket or Halo Implants

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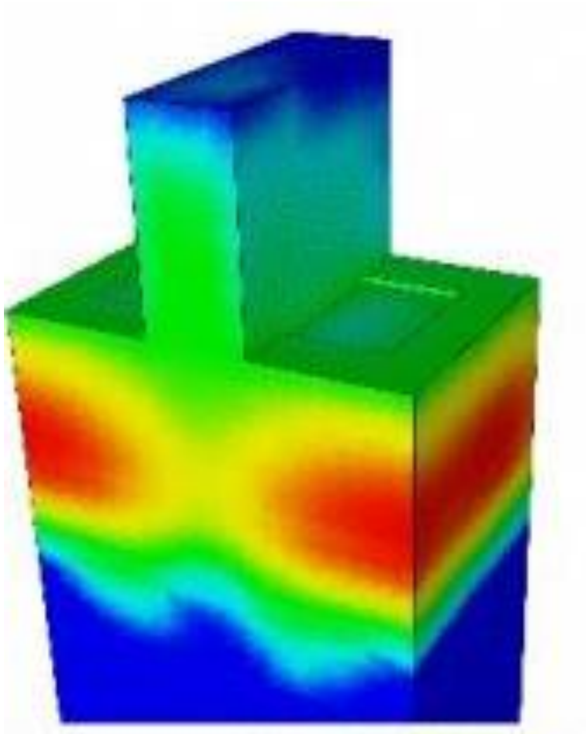
- Pocket or Halo implants are used to control the transistor threshold voltage, Vt
- They are implanted at a steep angle (37 to 45 degrees) to get dopant under the polysilicon gate
- They are key to improving the transistor off state performance whilst not compromising its performance when turned on



Technology Nodes Compared

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I_{OFF} (pA/um)	55LP 1.2V (C60)	40LP 1.1V (C50)	40ULP 1.1V (C50)
NMOS	24	33	11
PMOS	4.4	9	4

- 40ULP will achieve lower off-state leakage than 55LP
- VDD reduction is the only way to further reduce standby power


password
SECURITY

IOT-The connected era of everything

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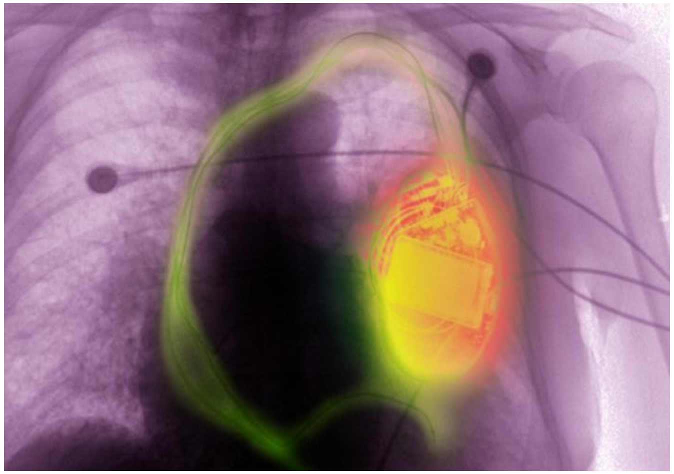

- Connection of things to internet
- Vulnerable to cyberattack

WHAT CAN WE EXPECT TO LOSE?
IS IT WORTHWHILE TO HACK?

Security motivations for IoT eco-system

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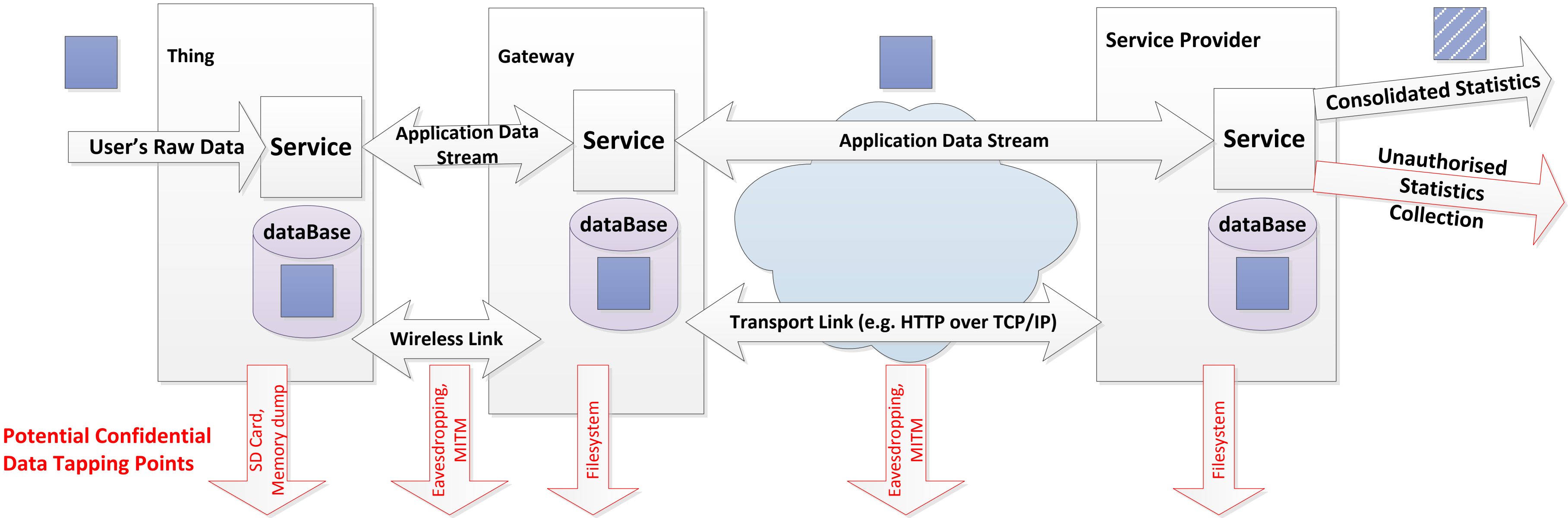
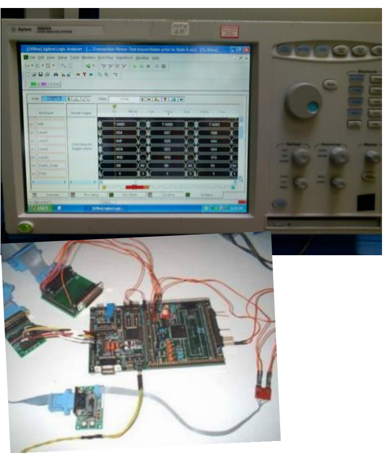


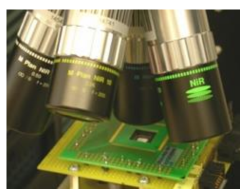
- Many opportunities for attacks!
- Securing Communication Channels – just part of the solution.
- Security is hard and needs hardware support

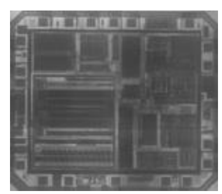
The section looks at hardware authentication and encryption

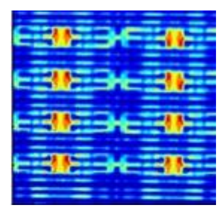
What The HACK?



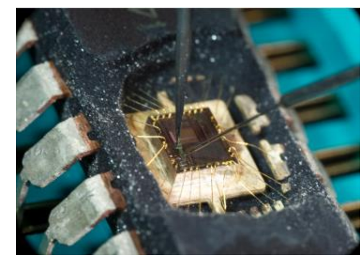
Non invasive attack
(glitch, clock, power attack)







Semi invasive attack
(NIR imaging, Laser imaging, fault injection)



Invasive attack
(decap, deprocessing, SEM, microprobing, FIB)

Si Manufacturing Variations

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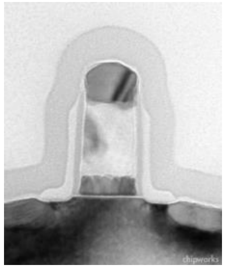
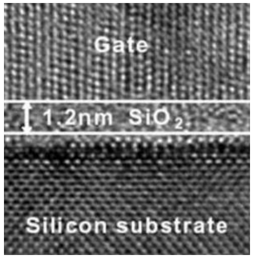
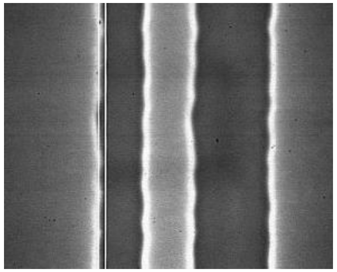


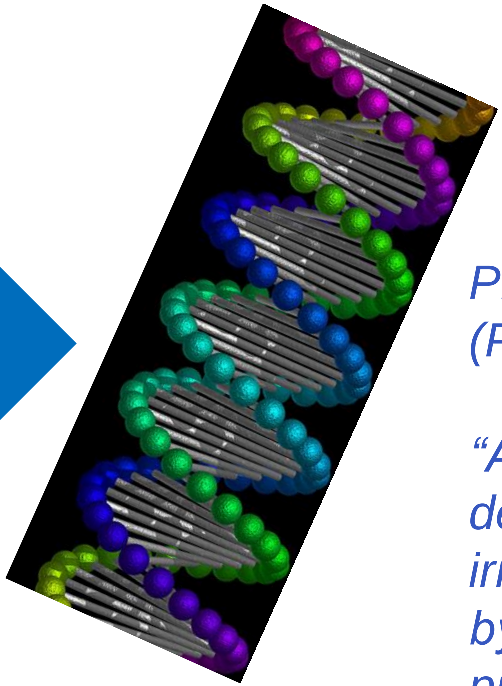
Random dopant fluctuation



Gate oxide thickness



Line edge roughness…



- *Nothing is deterministic anymore.*
- *Can we use this variation to create an unique DNA of every single chip?*

Physically Unclonable Function (PUF):

"A function whose execution depends on inaccessible and irreproducible variations caused by Silicon's manufacturing process. This serves as the generation of keys – basis of the whole root of trust and security aspects."

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Silicon PUF
and the Hardware Root of Trust Goal

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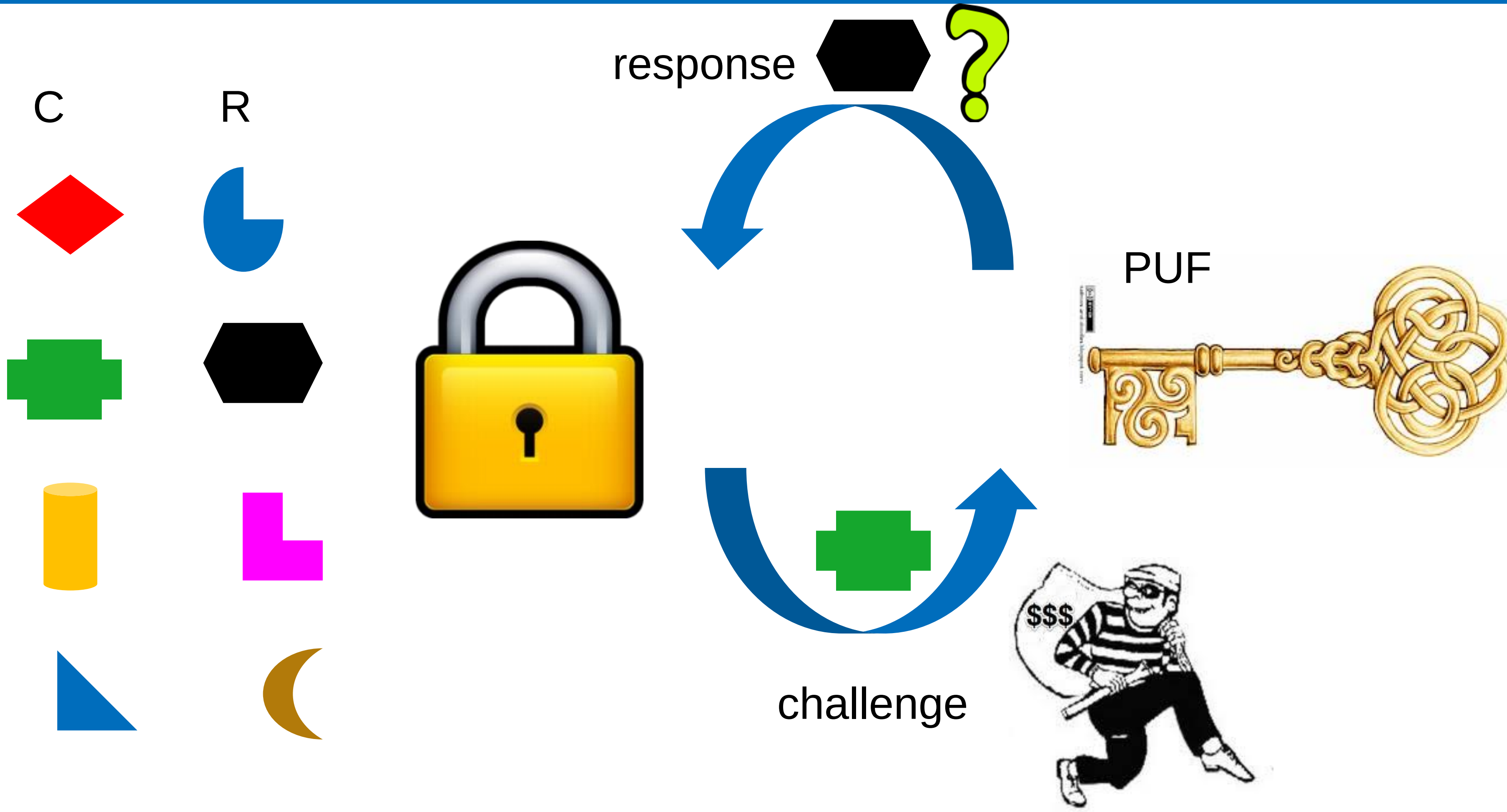

Features - Tamper and Side Channel Attack resistant, Hard to Reverse Engineer, Reliable, and low Cost.

Security is essential

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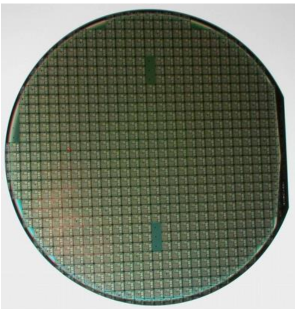

Write once public unique id per chip at manufacturer
- **ID accessible by FW/Apps layers**
- **This ID will associate to a unique key set**

Unique pair of private/public key per chip (Root Key Set)
- **Embedded in every single chip by manufacturer**

Root Identity Module using RKS to securely sign/encrypt/decrypt ID and config data

Root of Trust: privileged FW execution to sign ROM/RAM fw and apps and use RIM to sign and safely store signatures

ID identifies chip's public key

Unique Key Set
To sign in/Encrypt/Decrypt

Root ID module used to sign and store FW signatures

Comparison of NVM vs PUF

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Technology	Advantages	Disadvantages
NVM	• Erasable • Testable • Reliable • Low overheads	• Easy to reverse engineer • Require secure access path • Need special process step-> cost
PUF	• Difficult to reverse engineer • Inherently generated key • No special process step	• Not erasable • Not testable

- **<u>In Summary</u>**
- Wearables are evolving and revolutionizing our engagement with ourselves and the world around us.
- We have identified the important factors
  - Aesthetics
  - Power Consumption
  - Cost
  - Always On and Awareness
  - Security
- These all present challenges to consider as we move forward.

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