How to validate your FPGA design using real-world stimuli

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Agenda

- Typical FPGA Design
- NIs approach to FPGA
  - Brief intro into platform based approach
  - RIO architecture
- Case Studies
Typical Custom FPGA Design with I/O

Clocking structure (MMCM’s, constraints)

ADC/DAC Interfaces (I/O Timing, FIFOs)

DMA and Registers (I/O Timing, FIFOs)

DRAM Interface (I/O Timing, FIFOs)

DRAM, SRAM, EEPROM

Digital I/O

Front End Configuration

IP / Algorithms

Typical Custom FPGA Design with I/O

Clocking

ADC

DAC

Analog Engineer

Domain Expert

Digital Engineer

Software Engineer

Mechanical Engineer

PCI Express
NI FPGA

Clocking structure (MMCM's, constraints)

ADC/DAC Interfaces (I/O Timing, FIFOs)

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DRAM Interface (I/O Timing, FIFOs)

DRAM, SRAM, EEPROM

Front End Configuration

Digital I/O

ADC

DAC

NI I/O

LabVIEW FPGA

NI FPGA

Domain Expert
The NI Approach

We call this the LabVIEW Reconfigurable I/O (RIO) architecture.

Highly Productive LabVIEW Graphical Programming Environment for Programming Host, FPGA, I/O, and Bus Interfaces
Why program with LabVIEW FPGA?

Top 3 Reasons to Use LabVIEW FPGA

1. Graphical System Design
2. IP Libraries and HDL Code Reuse
3. Rapid Algorithm Development
Programming FPGAs with LabVIEW

Program with LabVIEW FPGA
- Develop, simulate, debug, compile and deploy through LabVIEW
- Familiar LabVIEW programming elements
- Integrate external FPGA IP

High-Performance Features
- High-throughput math functions
- Advanced timing control with Single Cycle Timed-Loops
- Access to optimized DSP Cores

Access to IO and Peripherals
- FlexRIO Adapter Module IO
- High bandwidth streaming over High Speed Serial or DMA
- Random access read/write to DRAM
Programming FPGAs with LabVIEW

Focus on your algorithms, not infrastructure

Clock Constraints  I/O Signals  Signal Processing  Functions

Controls from CPU  Intuitive Flow Control

DMA over PCIe

LabVIEW FPGA IP Commonly used with FlexRIO

10 Gigabit Ethernet UDP
3-Phase PLL
Accumulator
Area measurements
Bayer decoding
Binary morphology

Edge detection
Equalization
Exponential
FFT
Filtering
FIR compiler
Fixed-point filter design

Persistence display
PFT channelizer
PID
Pipeline frequency transform
(PFT)
Polar to X/Y conversion
Power level trigger

Writing
Element
Input Valid
Ready for Input

Fixed-Point to Integer Cast

Generate
Control
Utilities
High Throughput
I/O-RMS
Mean, Var, Std
Analog Period

Discrete delay
Discrete normalized integrator
D/A
Matrix transpose
Mean, Var, Std deviation
Memory IDL
Moving average
N channel DDC
Natural log
Noise generation
Normalized square
Notch filter

VITA-49 data packing
Waveform generation
Waveform match trigger
Waveform math
X/Y to polar conversion
Xilinx Aurora
Zero crossing
Zero order hold
Z-Transform delay

Focus on your algorithms, not infrastructure

Save time with extensive libraries of FPGA IP
## Embedded Hardware Options

**Board-Level and Packaged Controllers**
- Single-Board RIO
- CompactRIO

**Expansion I/O**
- MXI-Express RIO
- Ethernet RIO
- EtherCAT RIO
- Wireless

**For the Highest-Performance Applications**

### PXI and PC-based Devices
- PXI: RF, MI, and FlexRIO

- >1 MS/s Analog
- >10 MHz Digital
FlexRIO for PXI System Architecture

I/O
- FlexRIO Adapter Module
- Interchangeable I/O
- Analog, Digital, RF
- Custom I/O with MDK

FPGA
- FlexRIO FPGA Module
- Kintex-7 FPGA
- Up to 2 GB of DRAM
- PCIe Gen 2 x 8

Processor
- PXI Platform
- Embedded Controllers
- Synchronization
- Data streaming
- Power/cooling
FAM Architectures: Basic Analog Input

Analog Signal

16-bit ADC

Logic

16-bit ADC

Analog Signal
Concurrent Design and Test

- **Design**
  - System Design
  - Component Design

- **Test**
  - System Test
  - Component Test

Pathways:
- **Verification/Validation**
- **Prototype**:
  - NI 5791R FlexRIO SDR

Tools:
- NI 5644R VST
1. On-FPGA Measurements and Stimulus Generation

- **Real-Time and Continuous**
  - DUT

- Higher Test Throughput
- Hardware Re-Use and Future-Proofing
- New, Innovative Tests

*Lower Total Cost of Test*
Instrument Driver **FPGA Extensions**

The *compatibility* of industry-standard instrument drivers

The *flexibility* of the LabVIEW RIO architecture

**Instrument Driver** *FPGA Extensions*
Developing the World’s First Real-Time 3D OCT Medical Imaging System

“We leveraged the flexibility and scalability of the PXI platform and NI FlexRIO to develop the world’s first real-time 3D OCT imaging system.”

- To achieve 3D imaging capabilities, the two FPGAs in the system computed more than 700,000 512-point FFTs every second.
- Achieved high channel density, high-throughput data transfer, tight synchronization, and peer-to-peer data streams between FPGA modules.

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•http://sine.ni.com/cs/app/doc/p/id/cs-13387/