NextGIn Technology

Vertical Conductive Structures

A new Interconnect Technique

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Agenda

- The need for an alternative PCB technology
- Introduction of VeCS
- Technology comparison
- Cost comparison
- State of VeCS technology
- Application notes
- Transparent layer transition

The need for an alternative PCB technology

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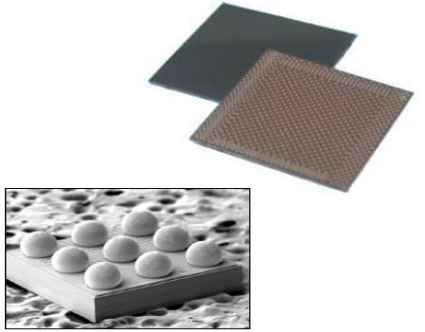
Grid arrays driving complexity

Advanced BGA

Enhanced Cooling

Multichip (memory, IO, etc.)



Chip Scale Packaging

Source: Ravi Mahajan, Intel Corporation

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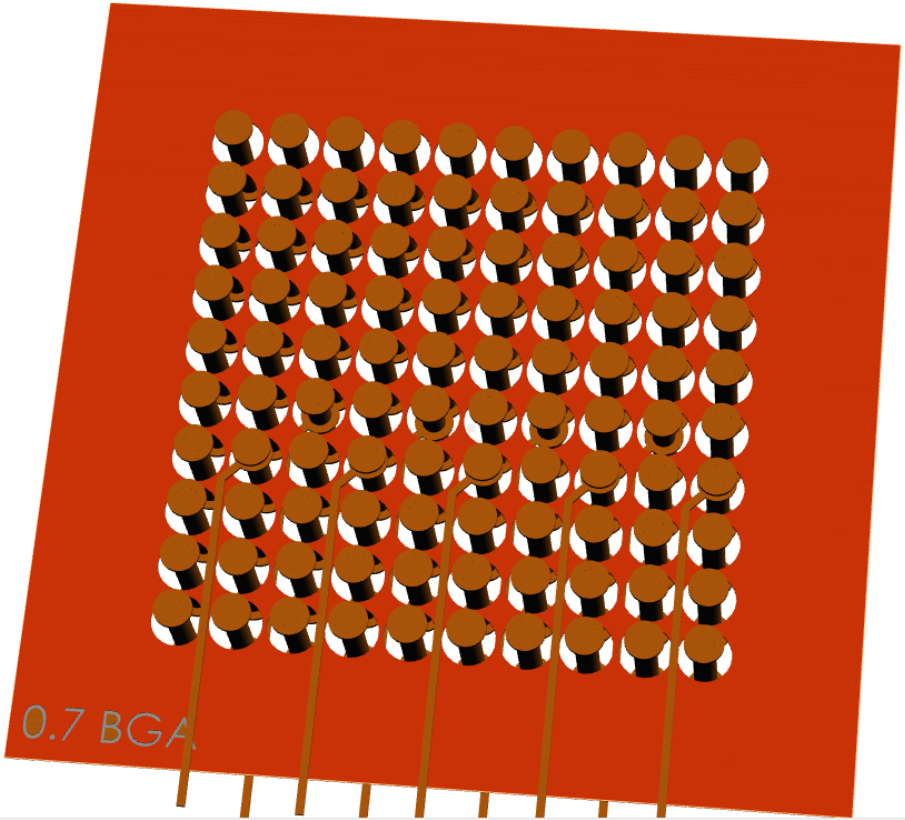
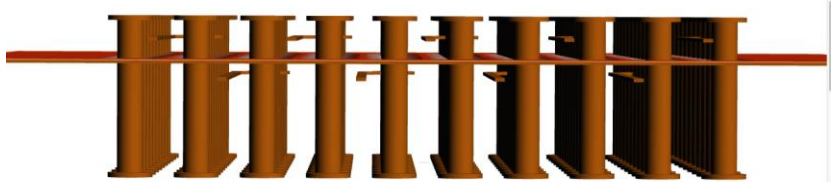
Limitation of current technology

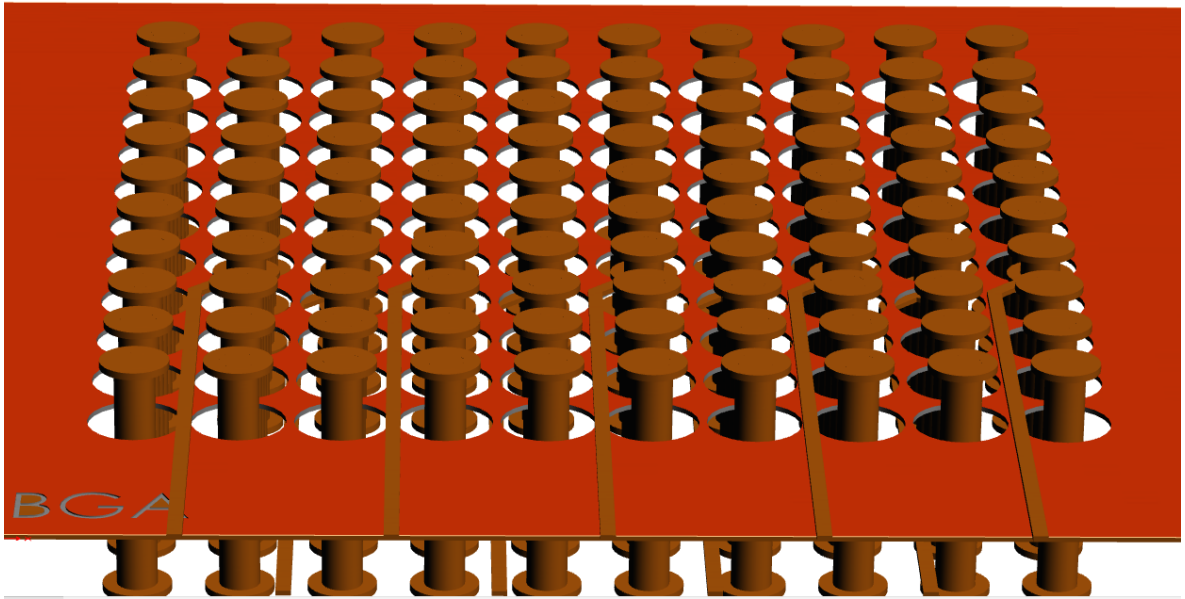


- Sub 1.0mm pitch BGA type packages are difficult to route.
- Layer counts are going up
- High speed signals require point to point routing requiring extra layers.
- High speed is analogue to power hungry applications.

Side *view* of routing channels



Limitation of current technology



- Current routing channels has limited capability below 1.0mm pitch
- Power planes are cut up reducing efficiency.
- No signal reference due to cut up planes.

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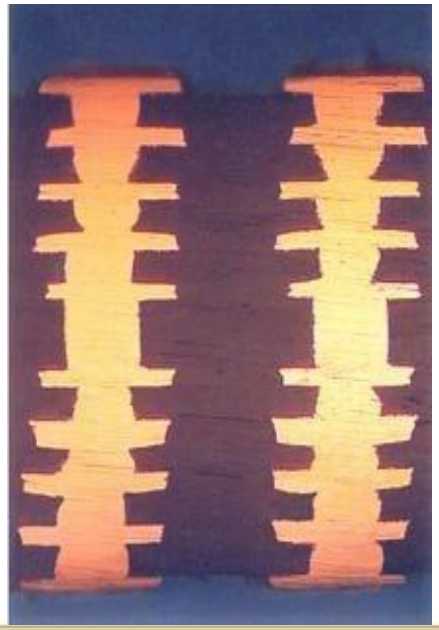
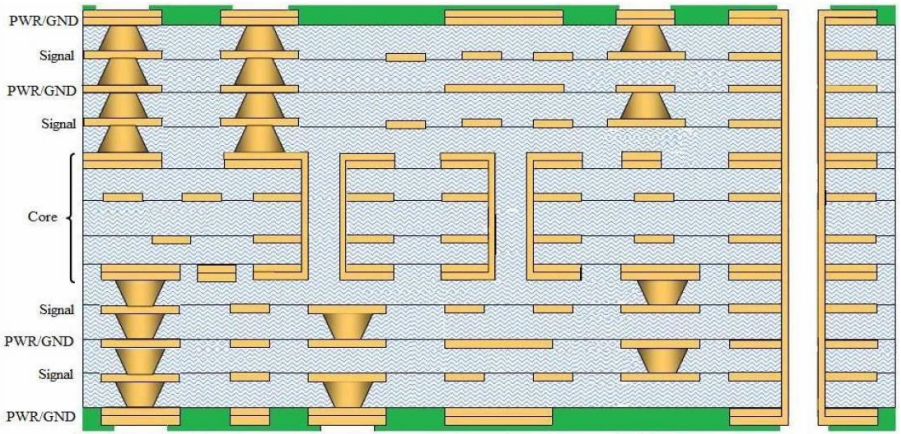
PCB technology legging behind

- Through hole technology is limited and take to much space. Holes cannot be placed closer.
- Sequential build-ups are a good but expensive solution. Yield is dropping when complexity increases.





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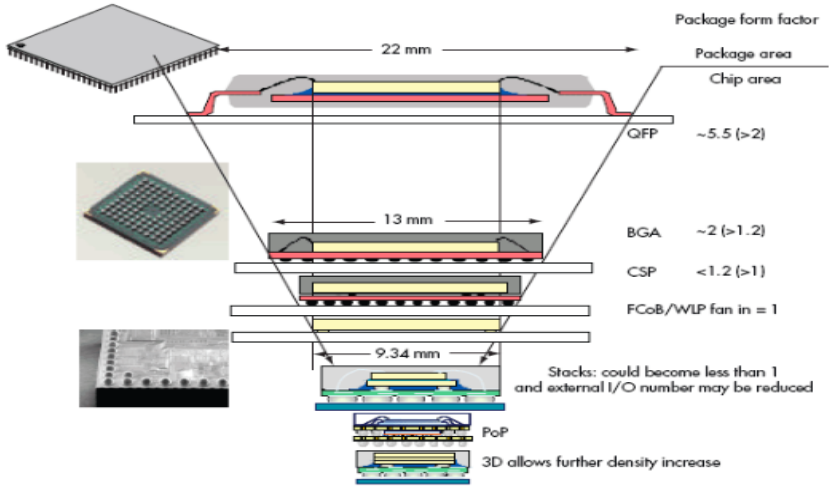
Slow down of smaller pitch packages

- Trend towards 0.8mm for Data/Tele-com and computing
  - Routing channel is becoming to small to rout (differential) 0,1mm track and gap.
  - Power distribution into core of package is difficult and expensive. Many heavy copper planes required.

Conclusion :

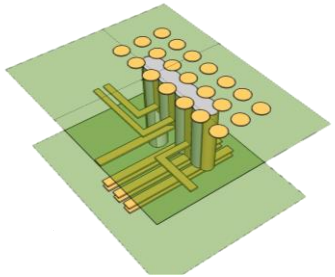
- PCB Technology is not keeping up with package trends
- PCB's prices will rise due
  - layer count increase,
  - Sequential builds
  - to yield loss and
  - Push for package complexity



Introduction to VeCS

What is VeCS

- VeCS stands for “Vertical Conductive Structure”
- A traditional through hole or blind hole is too big and too disturbing in terms of SI.
  - VCS creates a higher density of connections to the internal layers and with less distortion of the signal.
  - Less cutting in the power & ground planes for a better current carrying capacity and better reference plane for the striplines.
- VeCS is patent pending and can be licensed via NextGIn technologies.
- The technology can be build by any medium to advanced board shop after training and licensing. No direct new capital equipment is required.



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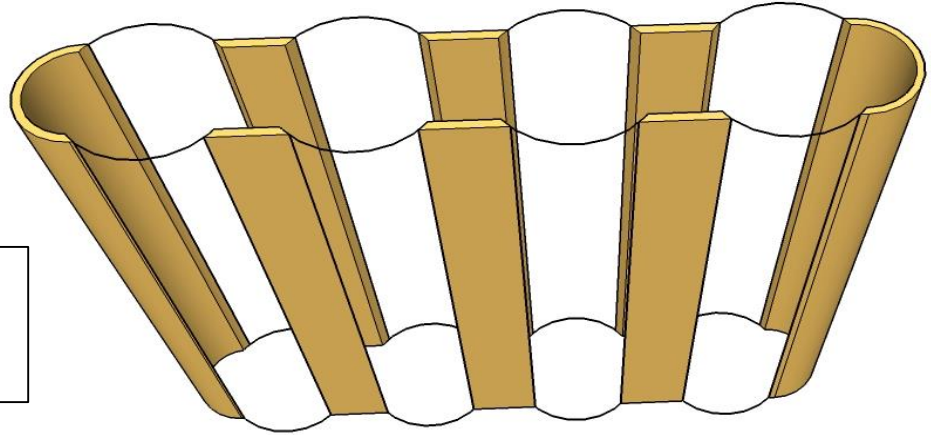
VeCS Principles

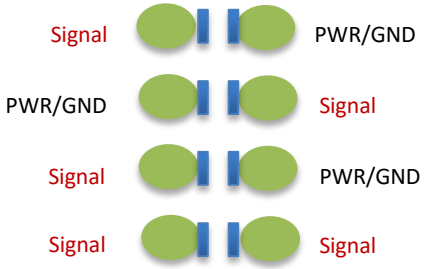
The hole is replaced by a vertical trace or half a sphere.
Preferred is the vertical trace from a signal integrity performance.



Structure can be filled and over-plated depending application

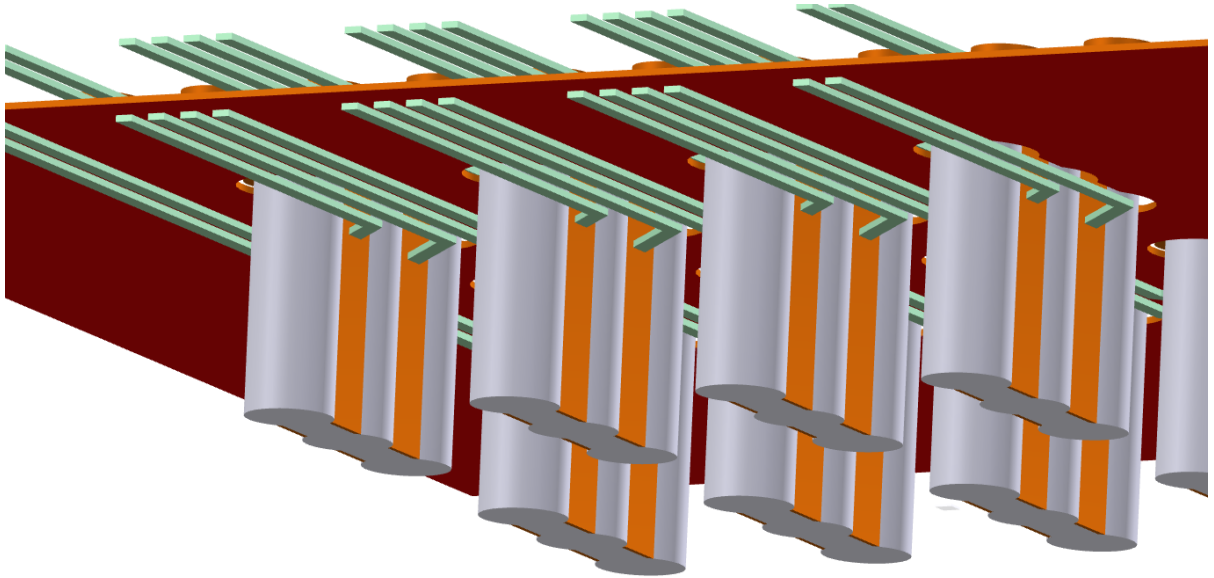
- More vertical connections per surface area
- No CAF path between vertical traces
- Coupling and Broad side coupling
- Thicker dielectrics, wider traces

Example Pin-assignment

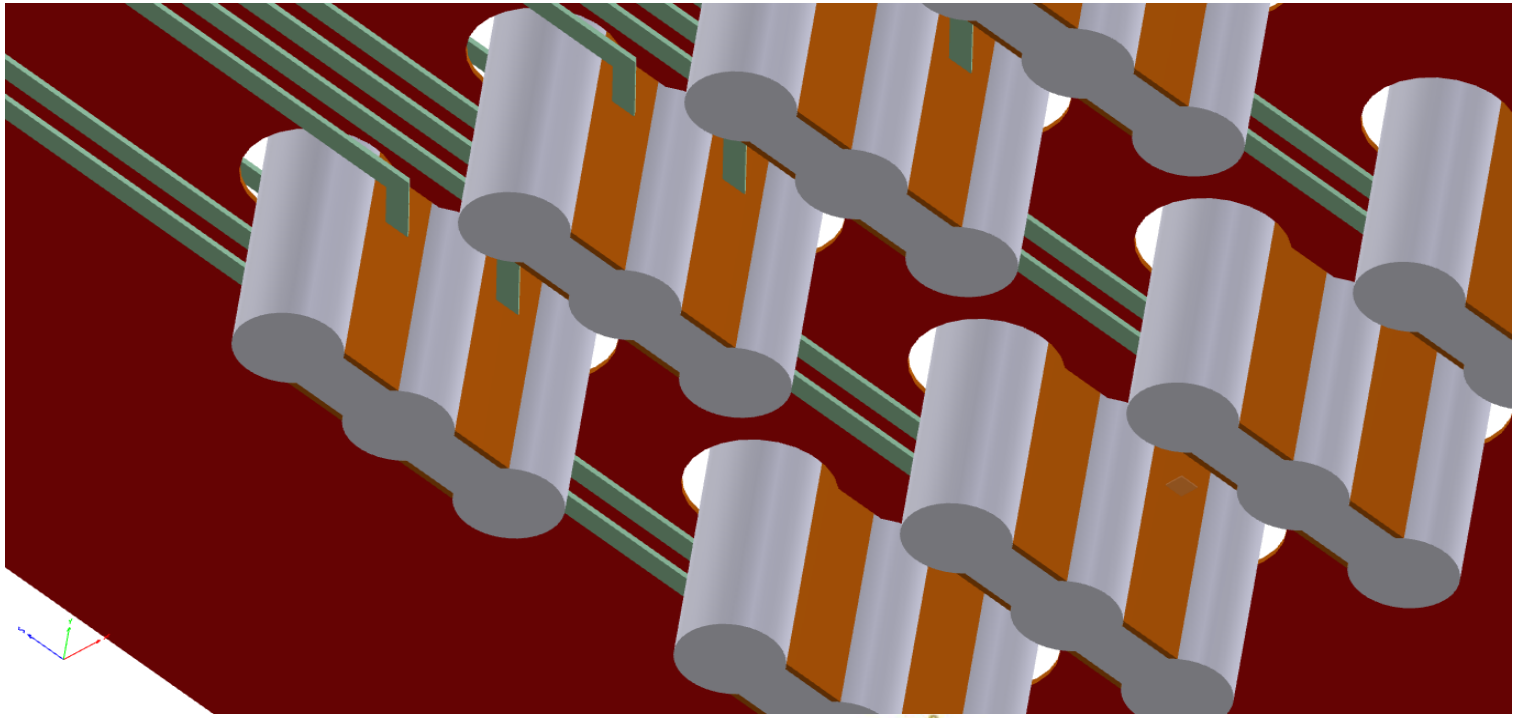


VeCS and routability

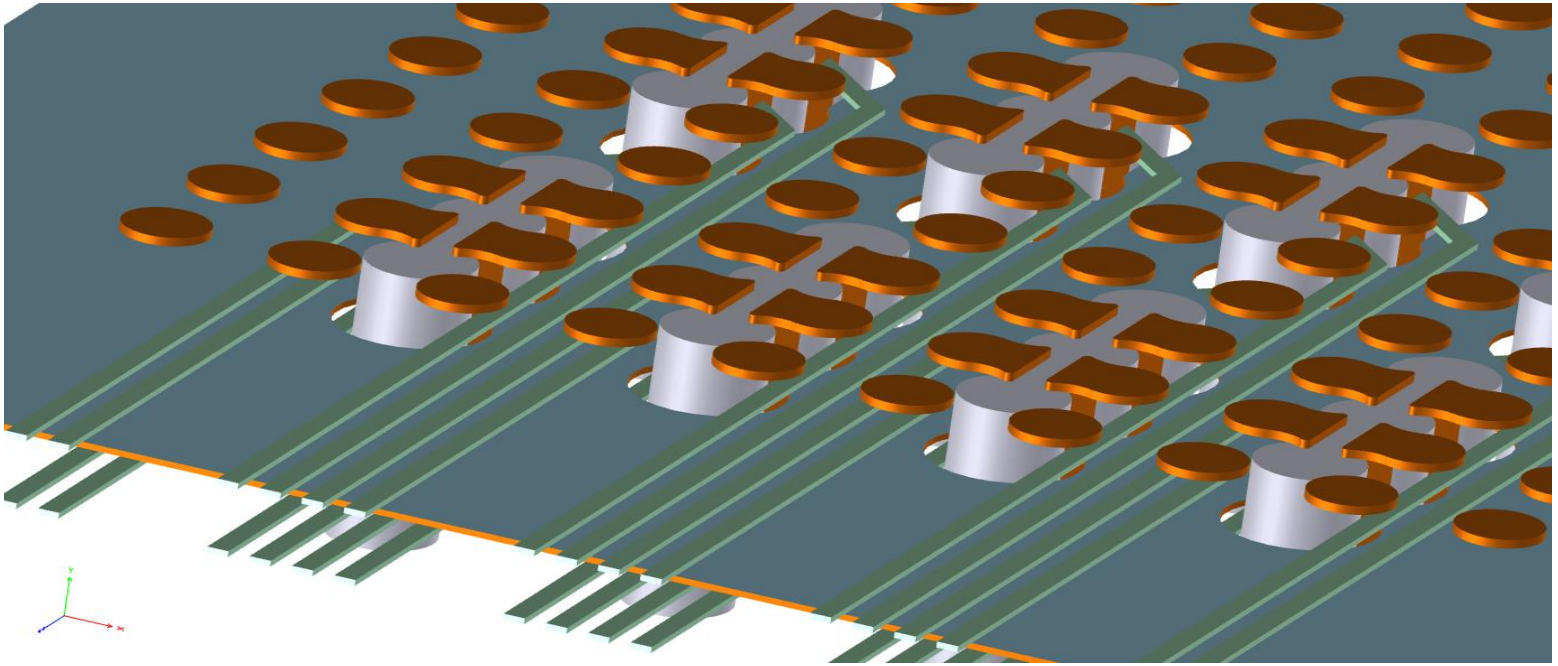
- VeCS uses special formed cavities that can connect to multiple internal layers using less space then vias or microvias resulting in wider router channels under Area Array Components like BGA's



VeCS and routability



Traditional channels disappears



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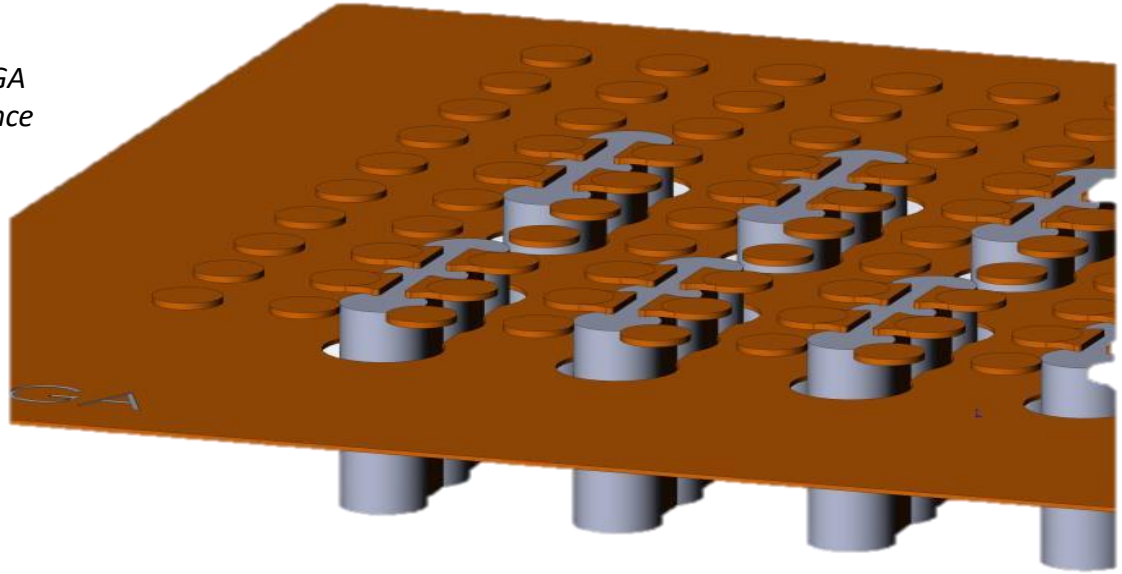
VeCS effect on planes

- Planes are becoming more and more important, traditional planes under BGA are cut up to small slivers of copper.

Example shows a plane under a 0.7mm pitch BGA with VeCS. A much more solid plane and reference compared to traditional via technology.



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Technology Comparison
VeCS vs. conventionial through hole

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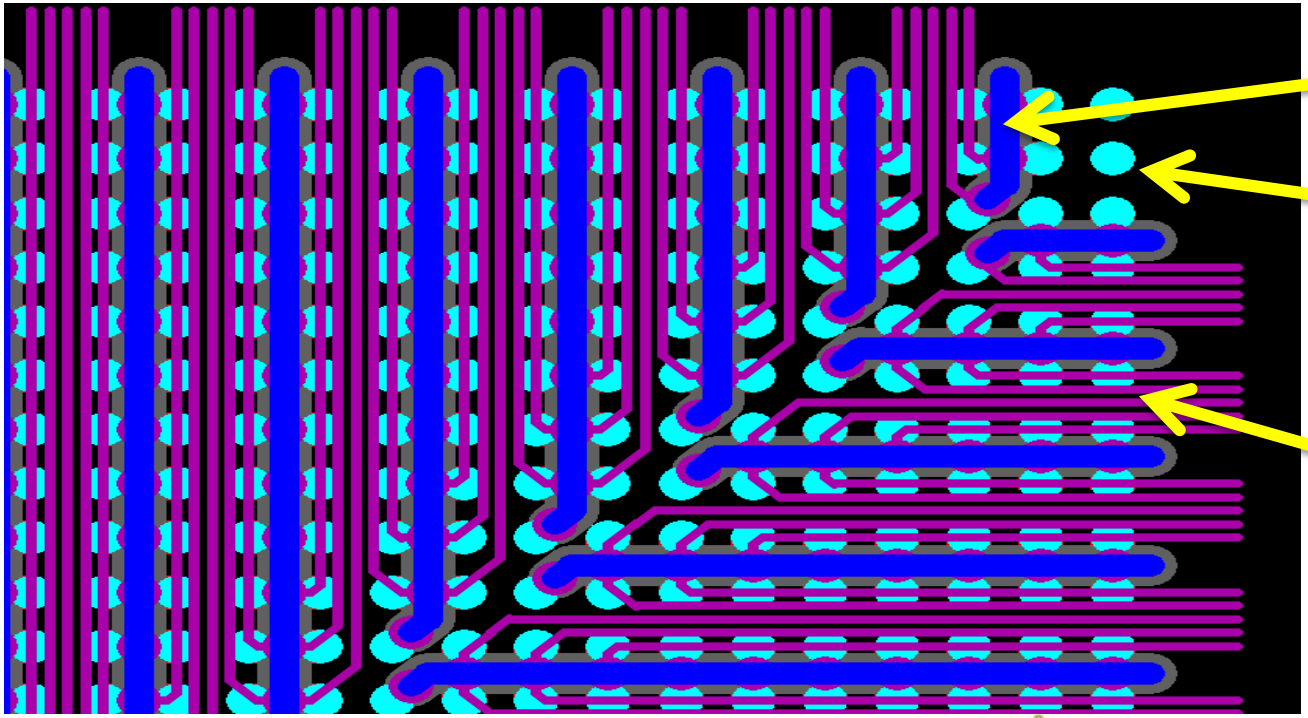
VeCS in design 0.8mm array

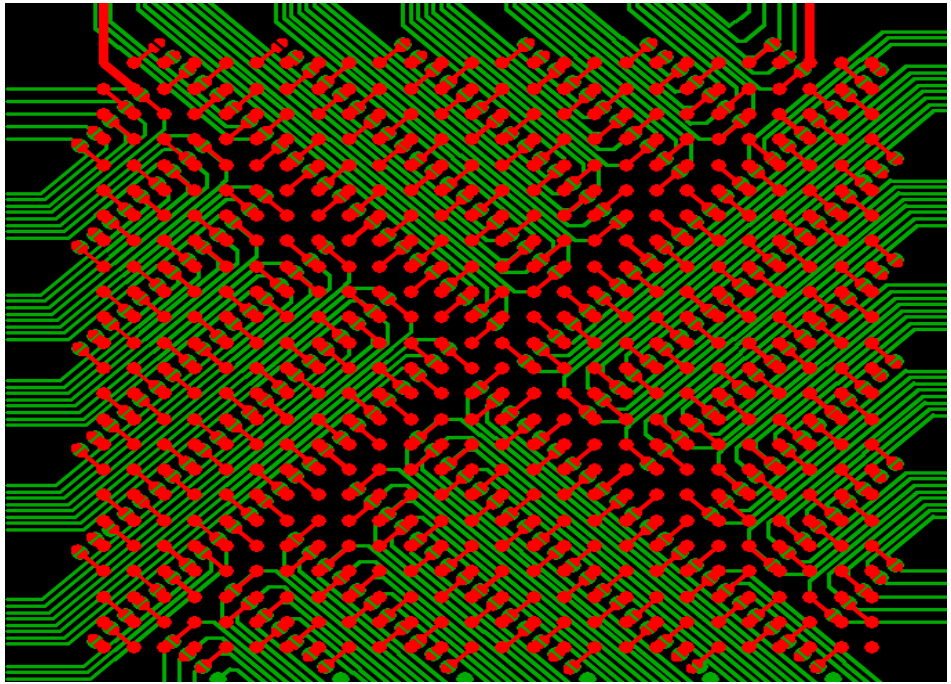


VeCS slot

BGA pad

Routing channel width is twice the device pitch.

Diagonal slot placement



- Increase of routing channel by 2x Sqrt(2).
  - 1,0mm = 2,82mm
  - 0,5mm = 1,41mm –pad size
- More signals per channel or more spaces between traces.
- More solid power/GND copper into the packages.

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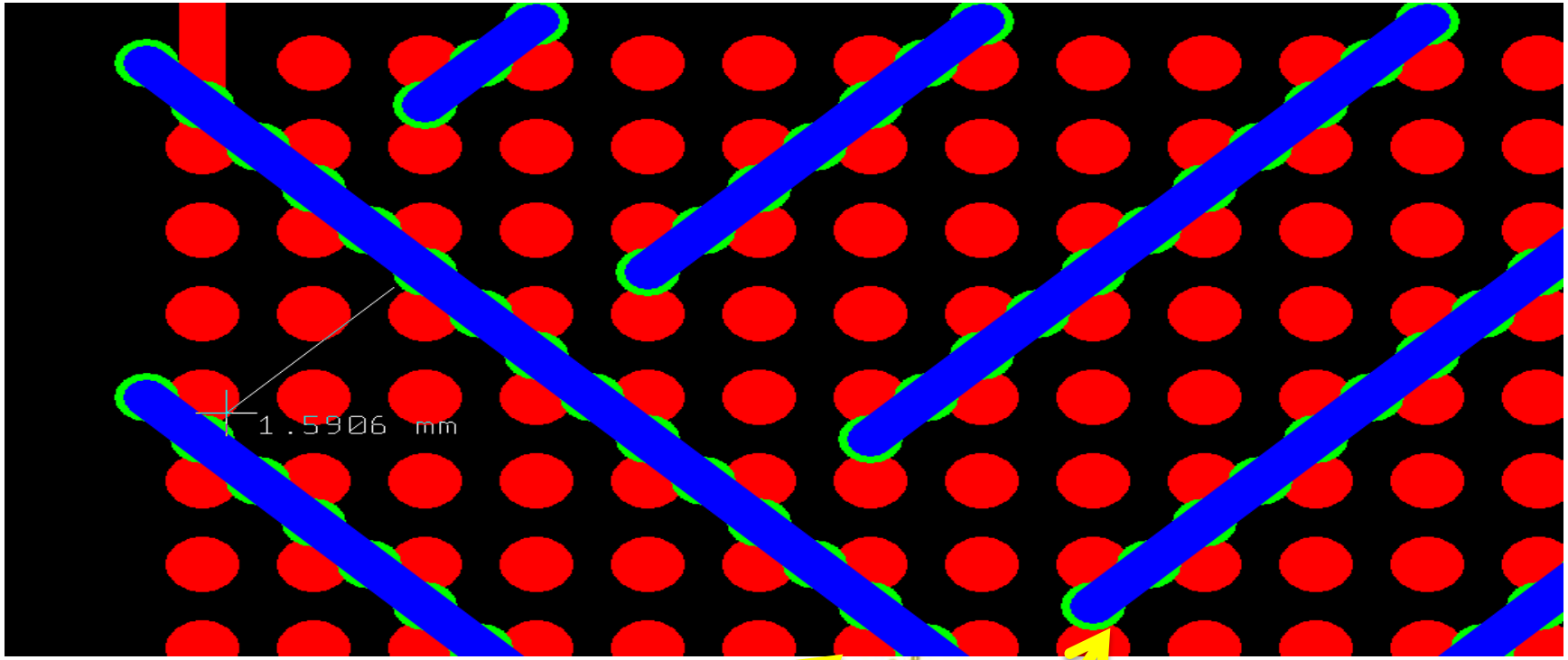
Diagonal slot placement



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Routing-channel utilization

Technology	Device pitch [mm]	Pad size BGA [mm]	Via pad size [mm]	Via drill size [mm]	Routing channel with [mm]	Trace width [mm]	Spacing [mm]	#traces per channel / Equivalent	improvement
Through hole	1	0,4	0,45	0,25	0,55	0,1	0,1	2	
VeCS	1	0,4	0,5	n/a	1,5	0,1	0,1	3	150%
Through hole	0,8	0,4	0,45	0,25	0,35	0,1	0,1	1	
VeCS	0,8	0,4	0,5	n/a	1,1	0,1	0,1	5	500%
Through hole	0,7	0,4	0,45	0,25	0,25	0,1	0,1	X	
VeCS	0,7	0,4	0,5	n/a	0,9	0,1	0,1	4	Massive
Through hole	0,7	0,4	0,45	0,25	0,25	0,075	0,075	1	
VeCS	0,7	0,4	0,5	n/a	0,9	0,075	0,075	6	600%
Through hole	0,5	0,35	0,35	0,15	0,15	0,05	0,05	1	
VeCS	0,5	0,4	0,4	n/a	0,6	0,1	0,1	2	200%
VeCS	0,5	0,4	0,4	n/a	0,6	0,075	0,075	3	300%
VeCS	0,5	0,4	0,4	n/a	0,6	0,05	0,05	5	500%

VeCS-2
or
High Aspect Ration Blind Structures (HARB)

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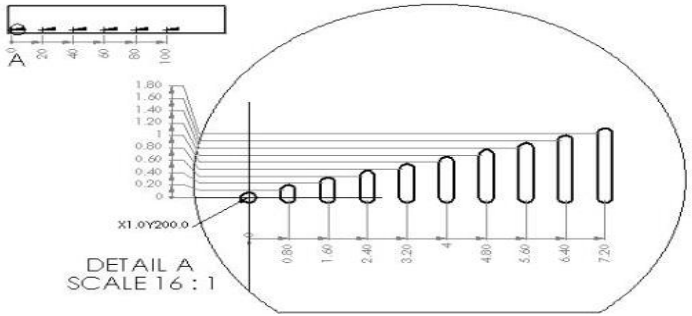
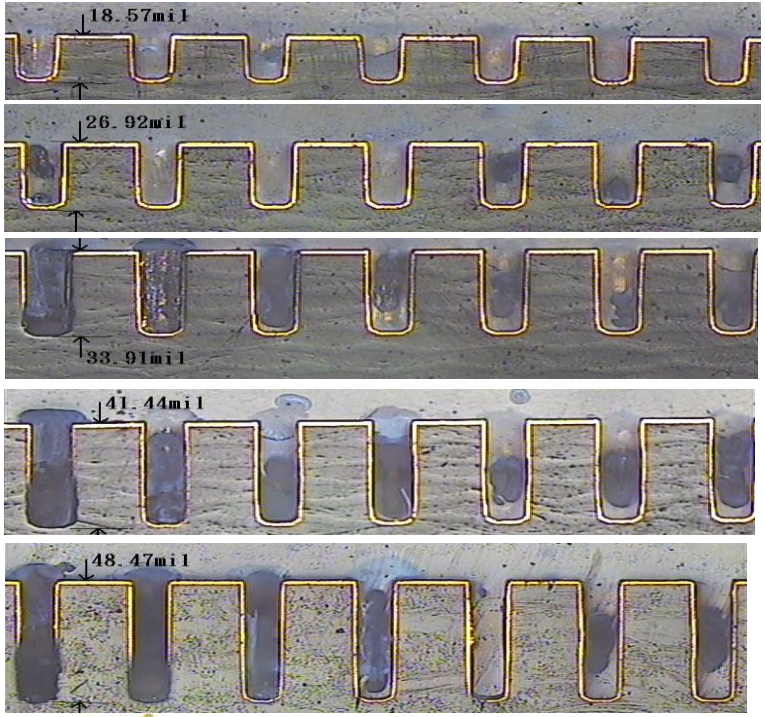
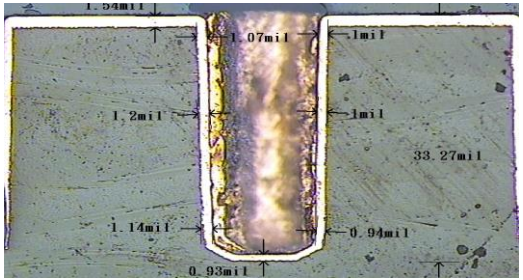
Plating results blind structures





❖ Shorter slot length reduce the plating capability.



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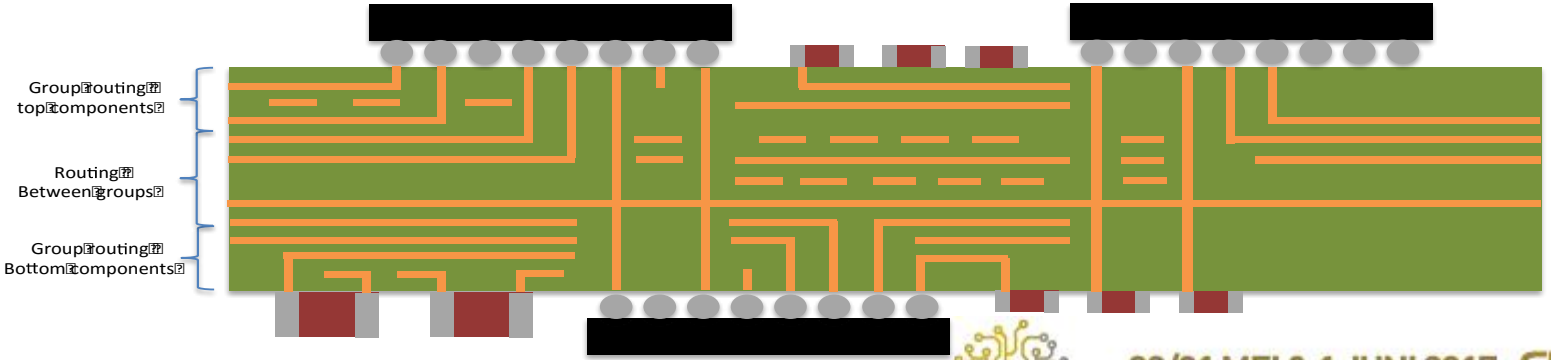
What can you do with VeCS-2

- Separate circuits on top and bottom – increase density and
- Utilize routing space much better, no via penetration through the board. (no sequential lamination required).
- Create connections for power(s) and ground for power hungry applications.
- Stubless connection to internal layers.
- Avoid sequential built-ups



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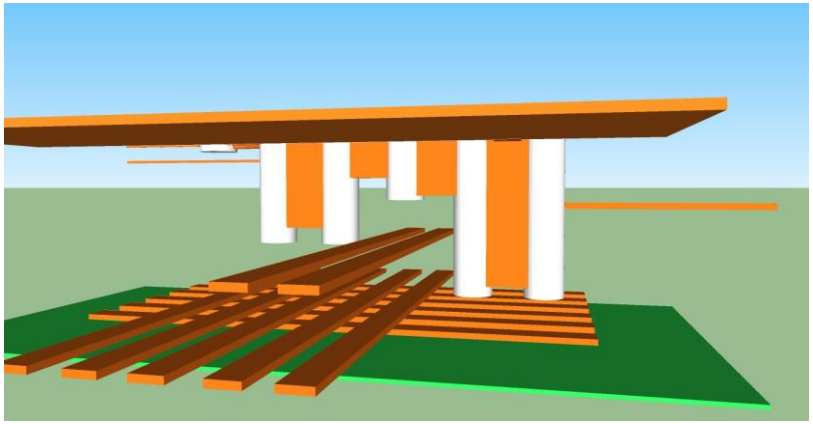
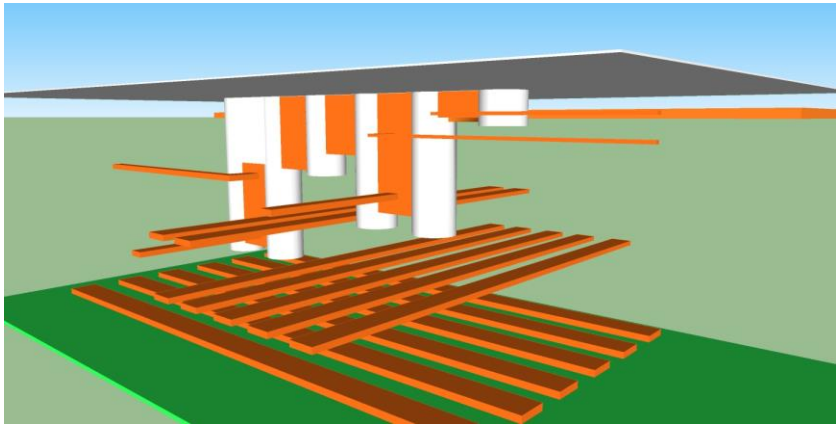
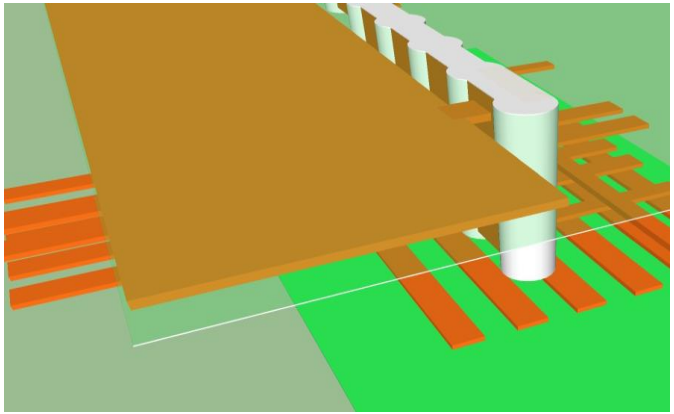
VeCS-2 application



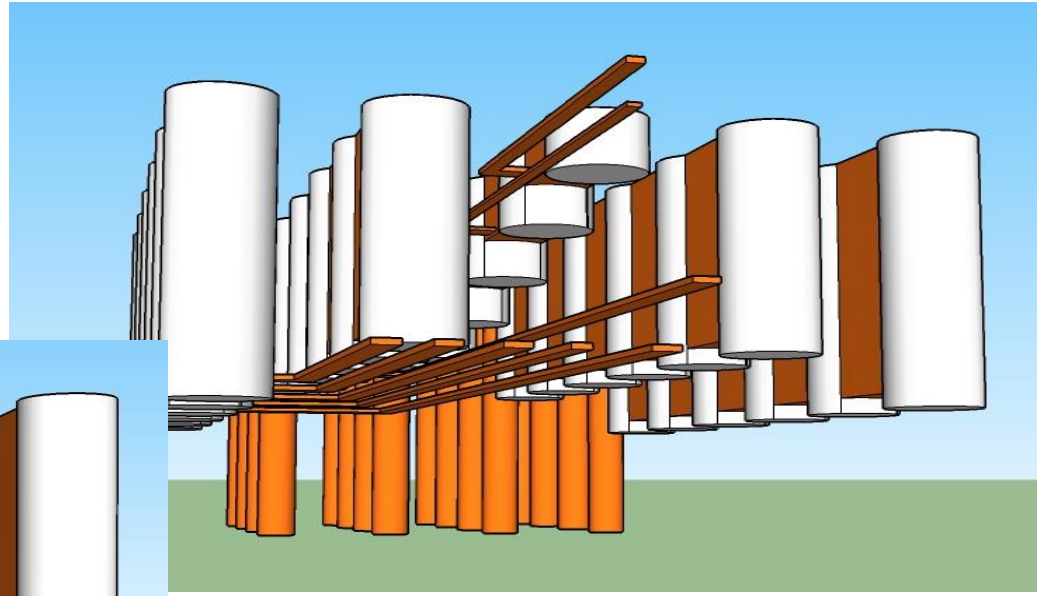


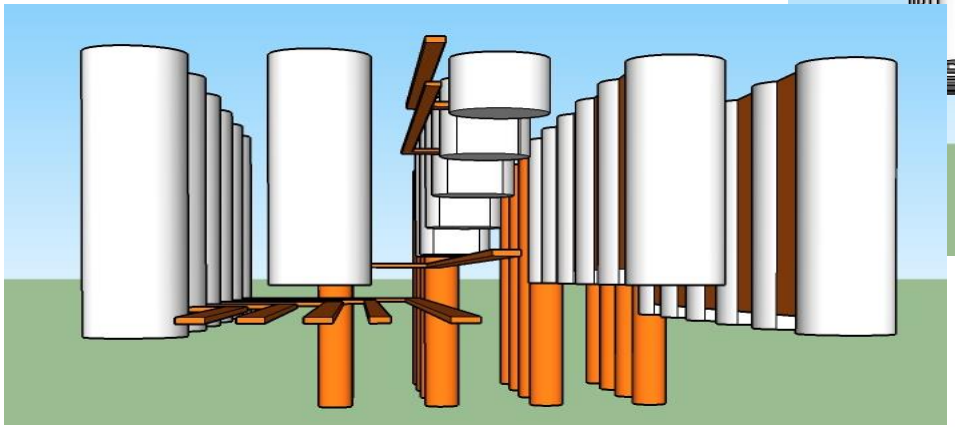


- Blockage free routing under the VeCS element.
- No backdrilling required – stublength of ± 8 mil.
- VeCS-2 element can be stretched, bent, etc.

BGA fanout

- Slot depths step down to each layer creating a wide routing channel.





Application Notes

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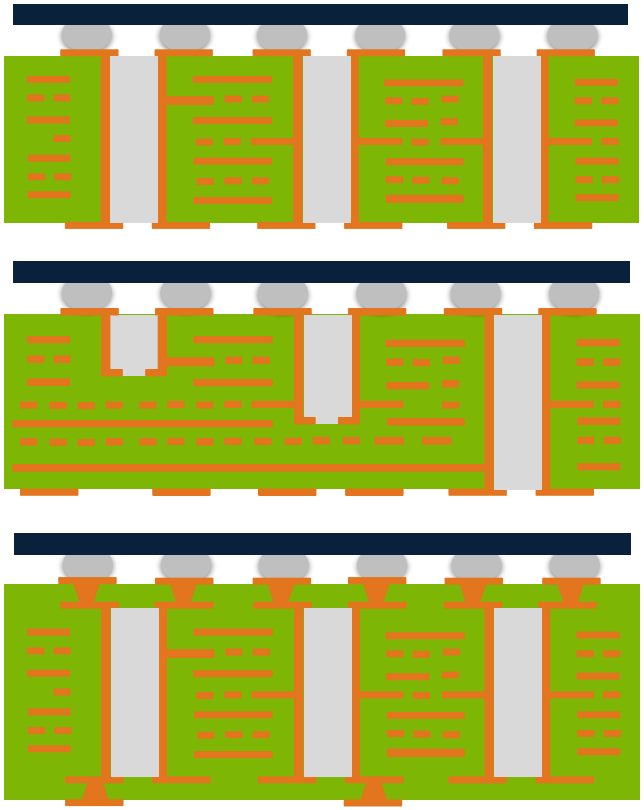
Connection to the Next Level

VeCS stackup configurations



"Traditional", VeCS-1, slot going all the way through the board.

VeCS-1 buried and capped using Microvias as the connection to the out-side.

VeCS-2, slots to certain depths combined with a through slot. This can be buried as well in combination with Microvias. VeCS-2 slots can be applied from both sides.

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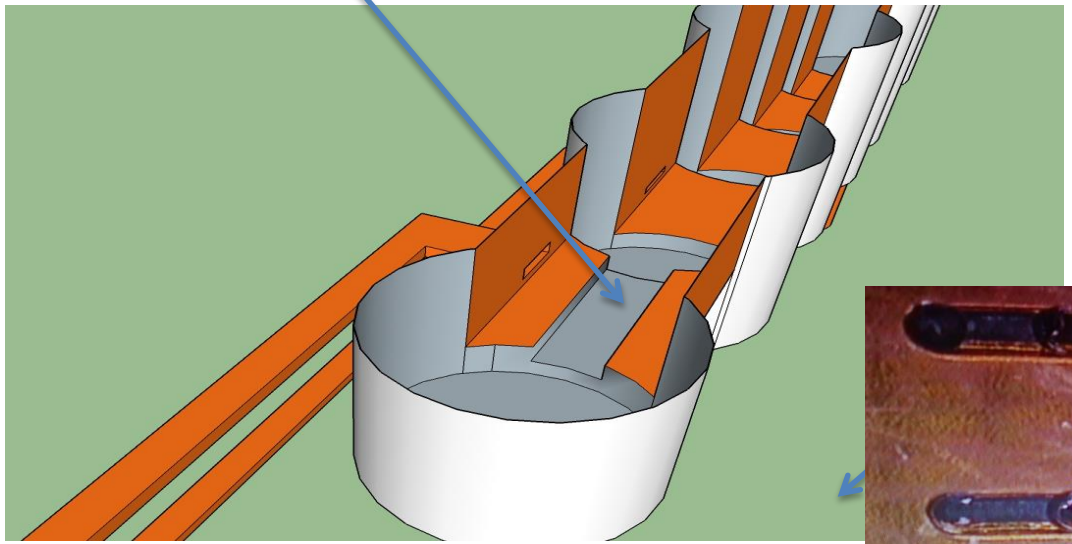
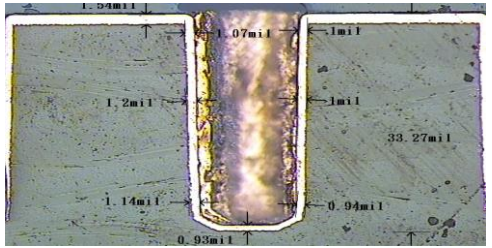
BGA fanout using VeCS-2

The middle part (conductive material is removed to create two different potentials two the left and right of the slot. Not every position in the slot need to be processed in this way. It dependents on the design





Top view of VeCS-2 slot showing multiple depths and a section going through the board.

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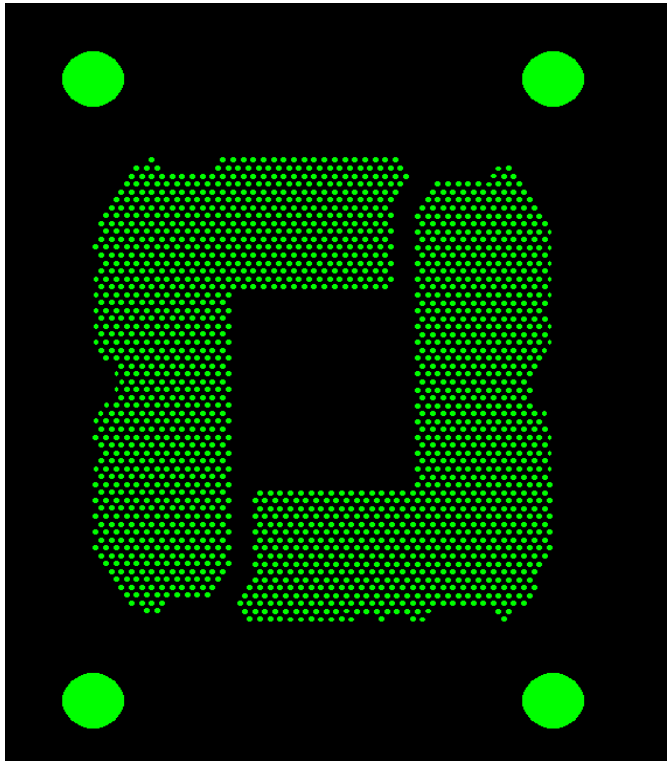
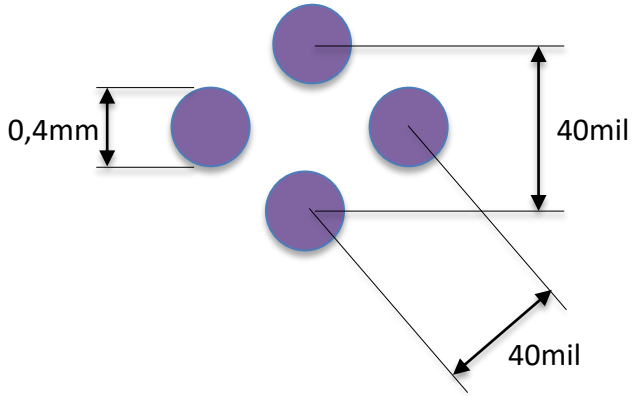
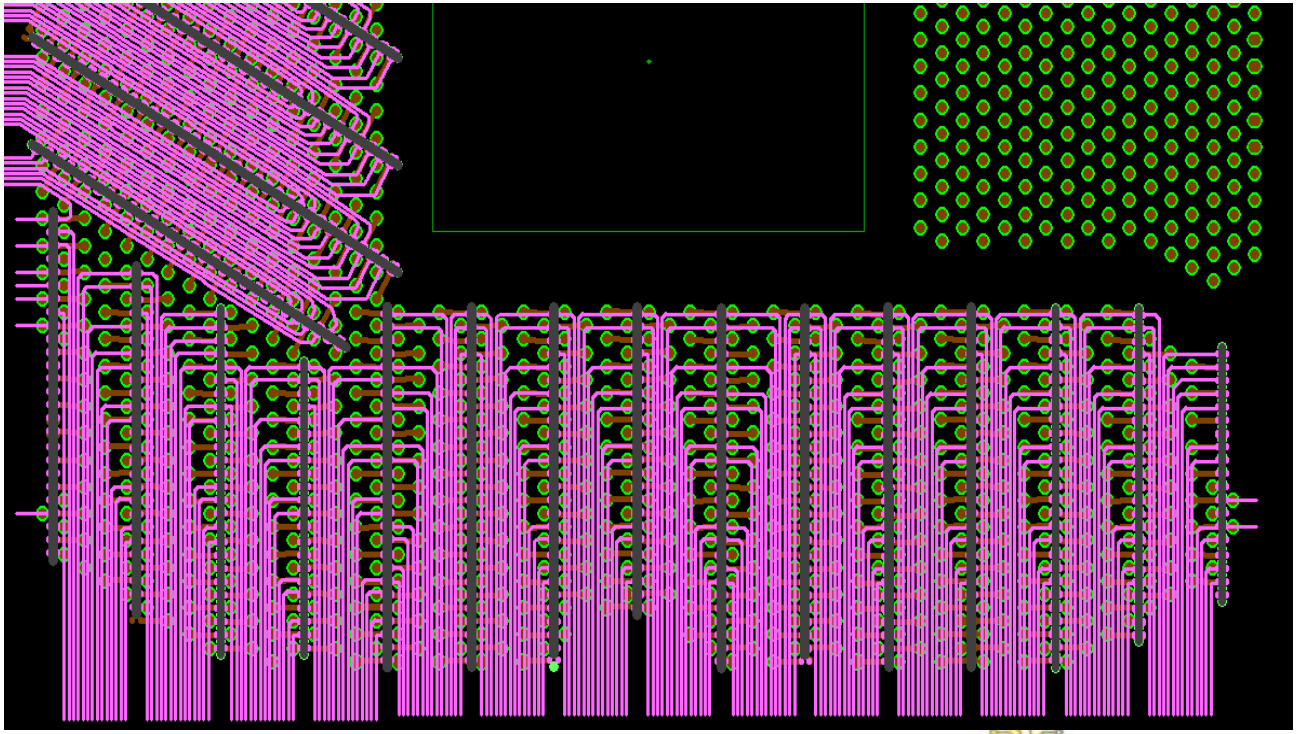
Intel Xeon E7 Footprint



Example of the Intel Xeon E7 footprint
The pads are arrange in an equal pattern of 40 mils as shown below.



VeCS fanout of Intel Xeon E7



This example shows a possible VeCS fan-out of the Intel Xeon E7 footprint.
The track and gap is 0,1mm, there are 14 lines per VeCS channel.
Many other VeCS patterns are possible, one example is given in this document.

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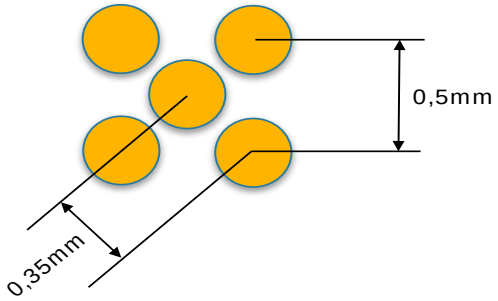
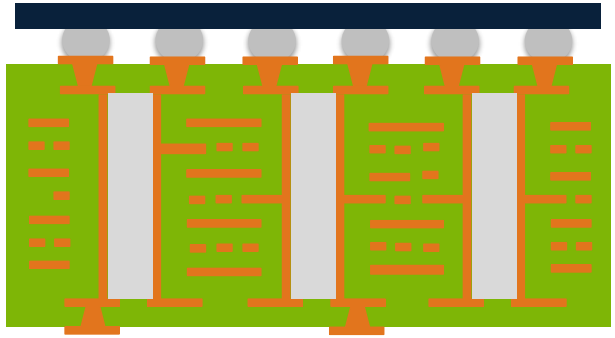
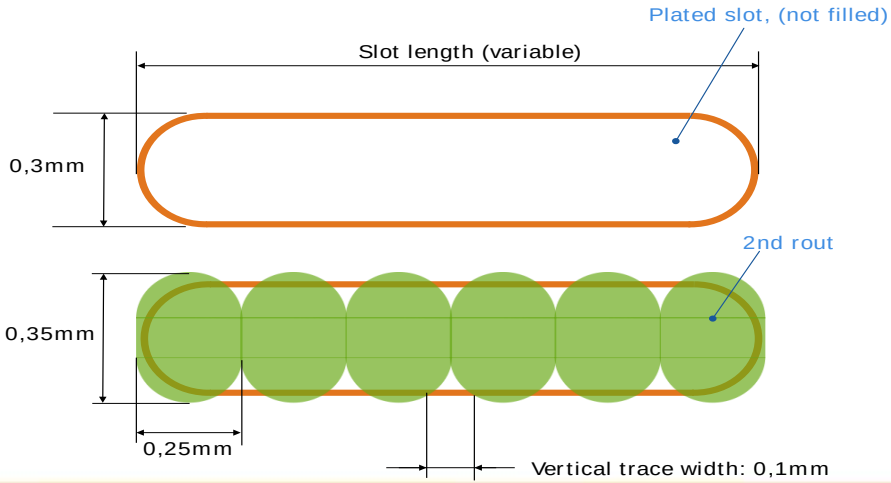
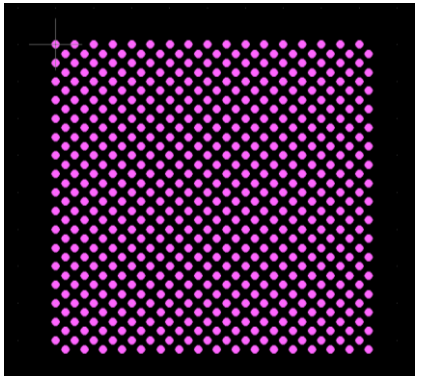
0,35mm staggered VeCS fanout

VeCS slots are buried and connected using Microvia on two sides.









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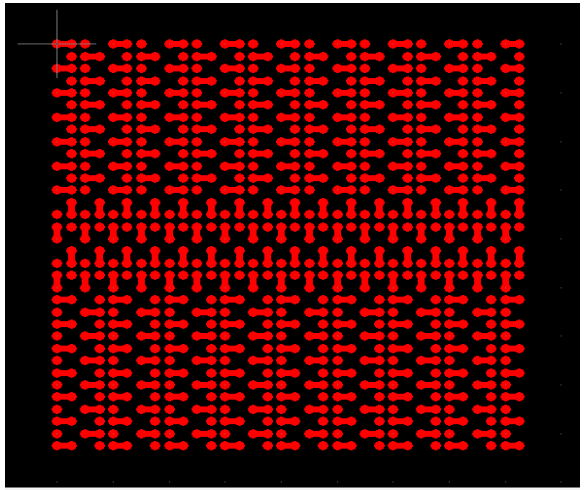
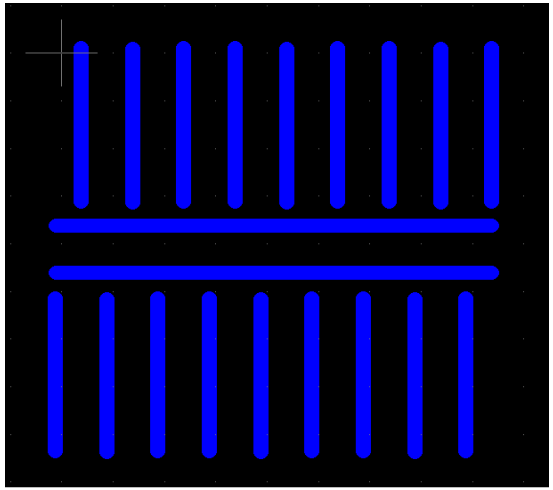
0,35mm staggered VeCS fanout

A high dense BGA (578 I/O) routed either with 2 traces of 0,12mm and 0,12mm gaps or a 3 traces of 0,08mm and 0,08mm gap

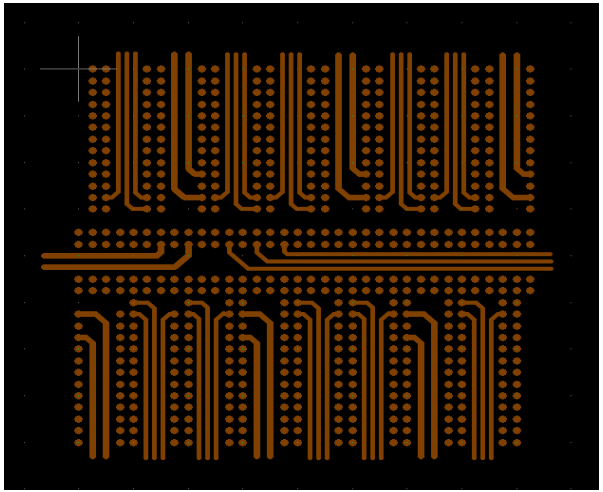
Layer 2/Ln-1, microvia landing pads



Slot layer



Signal layer



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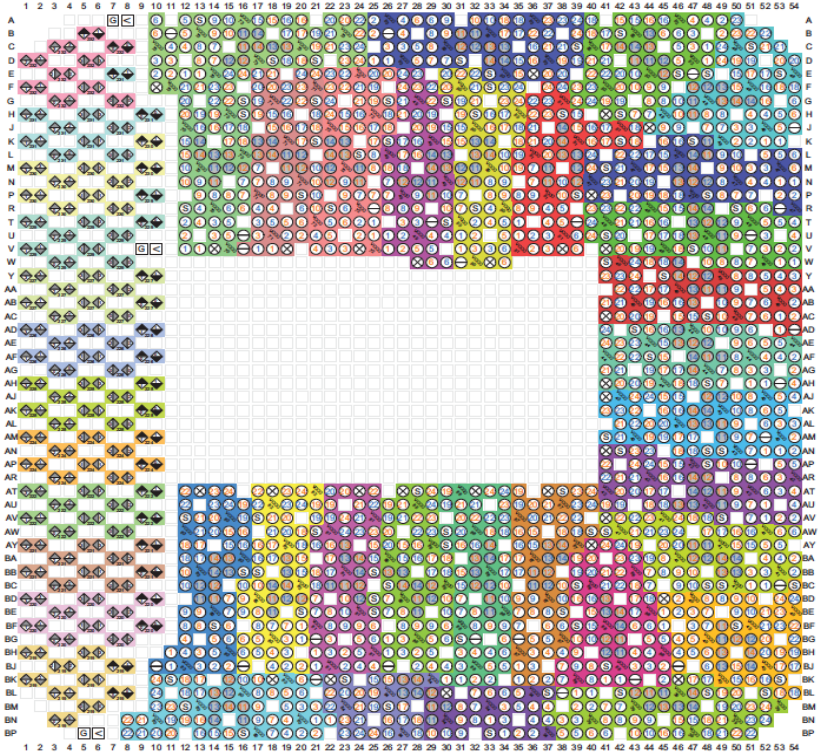
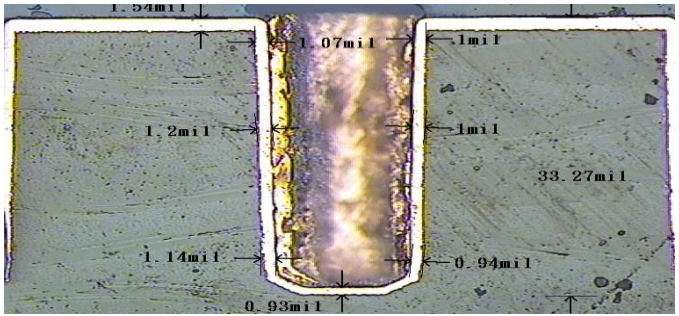
Fan-out of Xilinx FLGA 2892



- Fan-out using VeCS-2 of the 54x54, 1.0mm pitch BGA from Xilinx FLGA 2892
- High speed SERDES (differential lines) , banks are all differential as well.
- Uncoloured squares are all power / GND pins.



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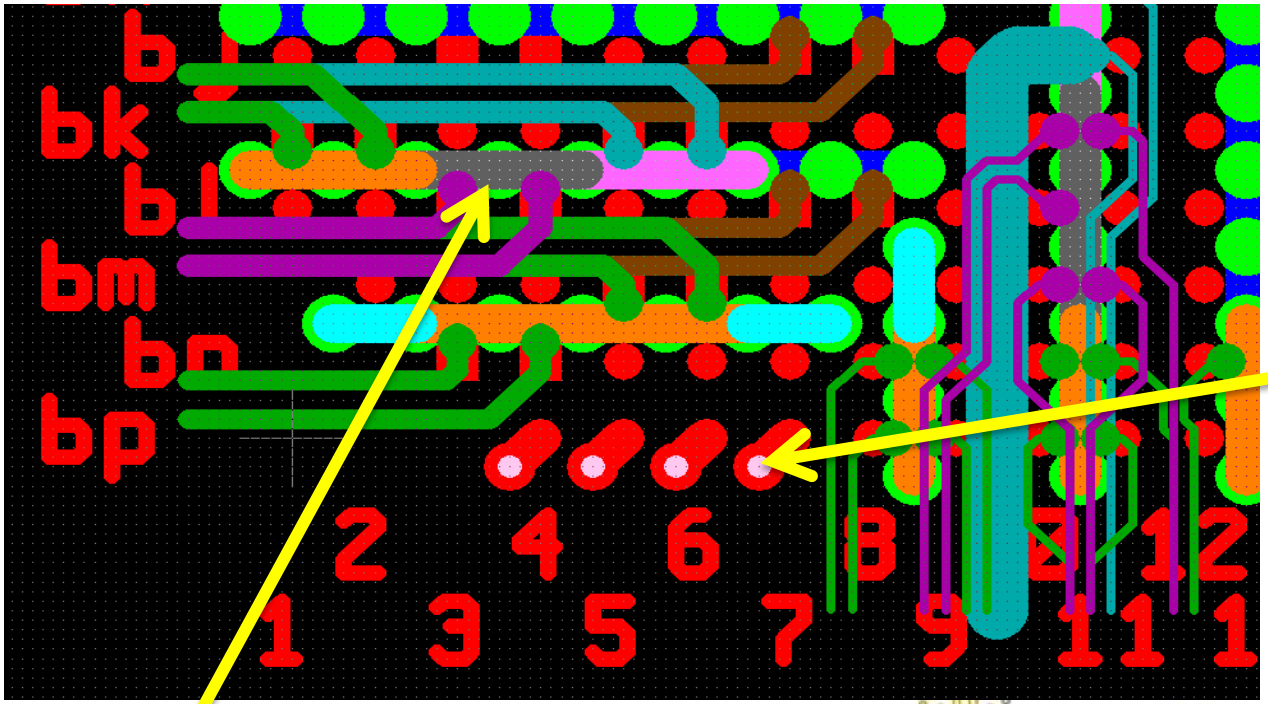
Fan-out of Xilinx FLGA 2892

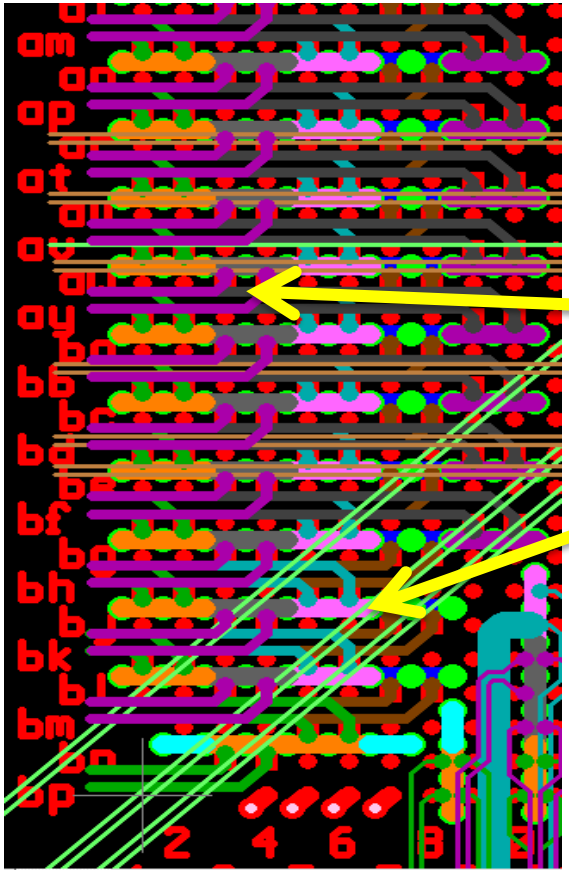
Fan-out of Xilinx FLGA2892, BGA 1,0mm, array 54x54



Through hole (standard) Vias

Different depths of VeCS-2

Fan-out of Xilinx FLGA 2892



High Speed SERDES channels can be routed with wider traces then a traditional channel.

Trace on lower layers (green) can be routed without any blockages.

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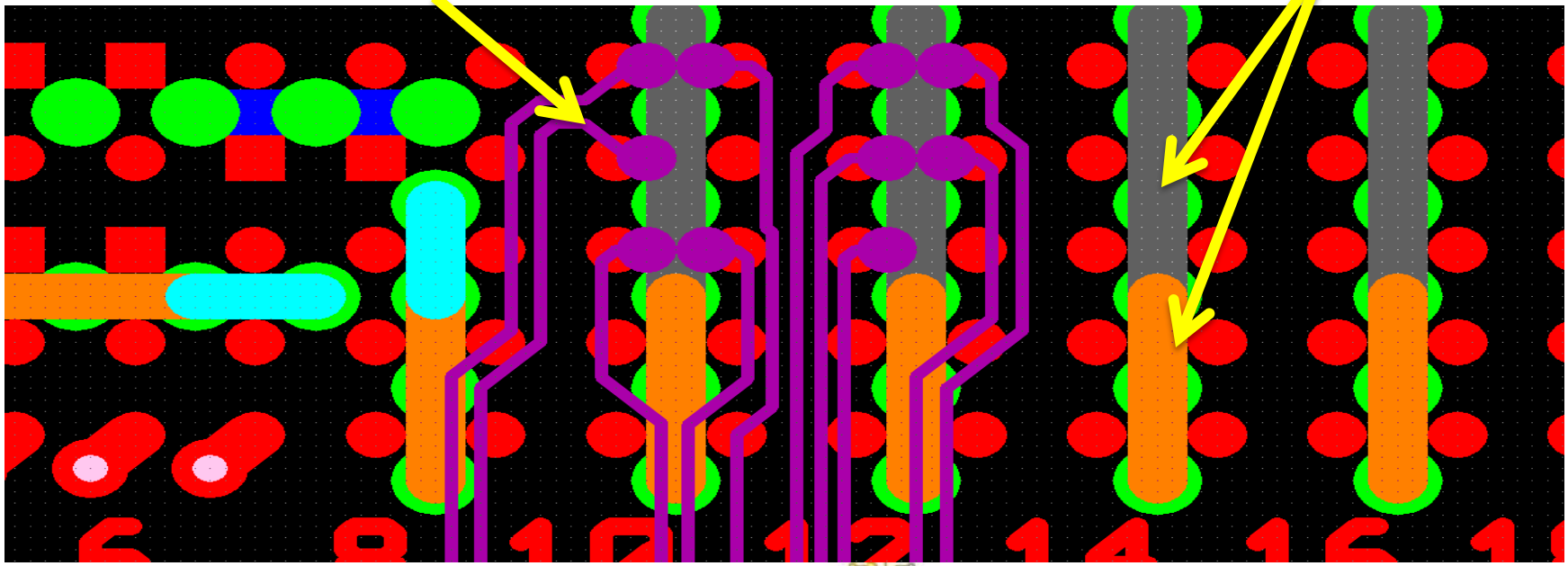
Fan-out of Xilinx FLGA 2892

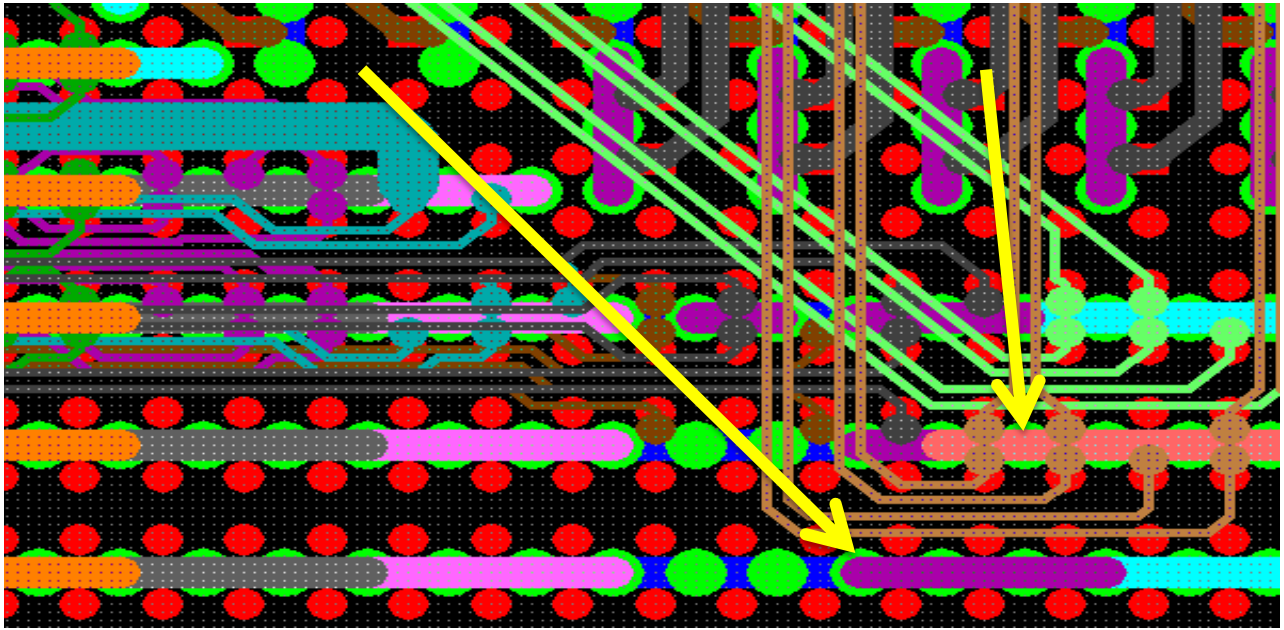
Differential routing using VeCS-2

Different slot depths in different colours



Fan-out example(s)

Fan-out of Xilinx FLGA2892, BGA 1,0mm array 54x54



Non-blockage routing when using blind technology. Traces cross over (below) slots.

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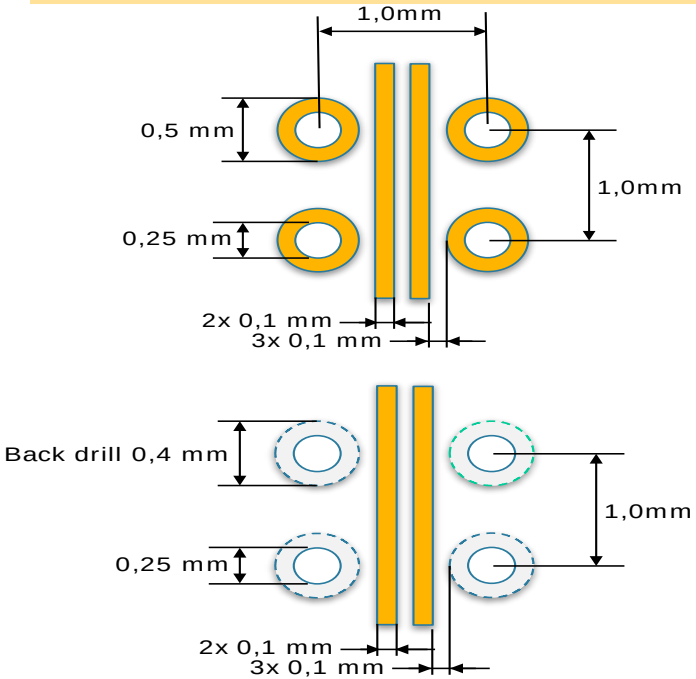
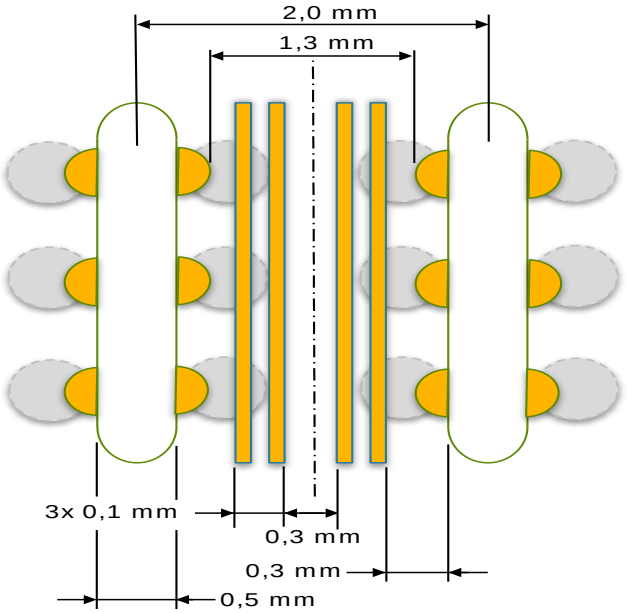
Fan-out 1,0 mm pitch BGA

Through hole + backdrill design rule



Diff. pair VeCS design rule



Cost Comparison

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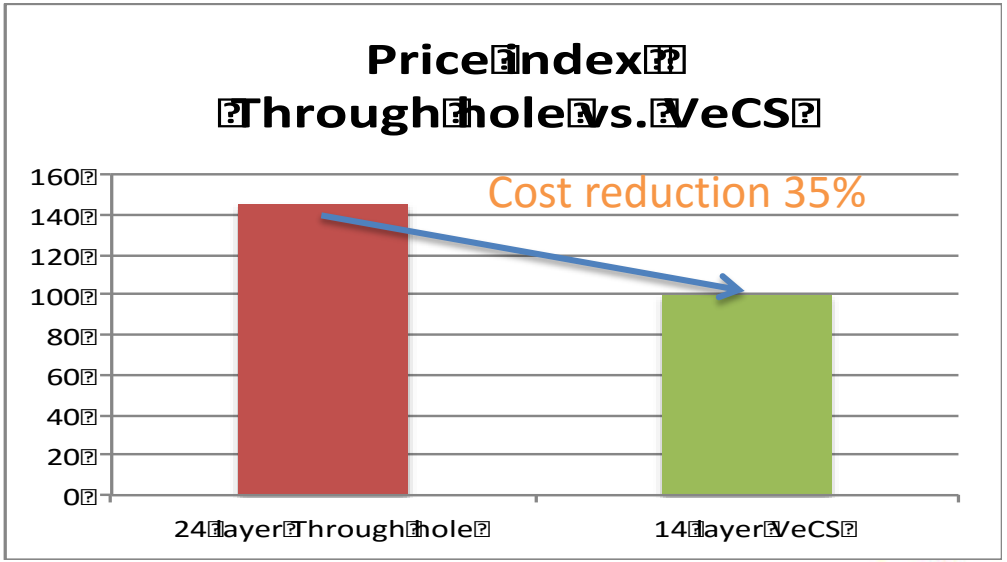
Cost comparison

- The cost reduction is realized by reducing the layer count of the board ie. making more efficient use of the routing space.



- In this example a 24 layer is reduced to 14 layers realizing a cost reduction of 35%
- The same bandwidth of reductions can be applied for other layer count and constructions.

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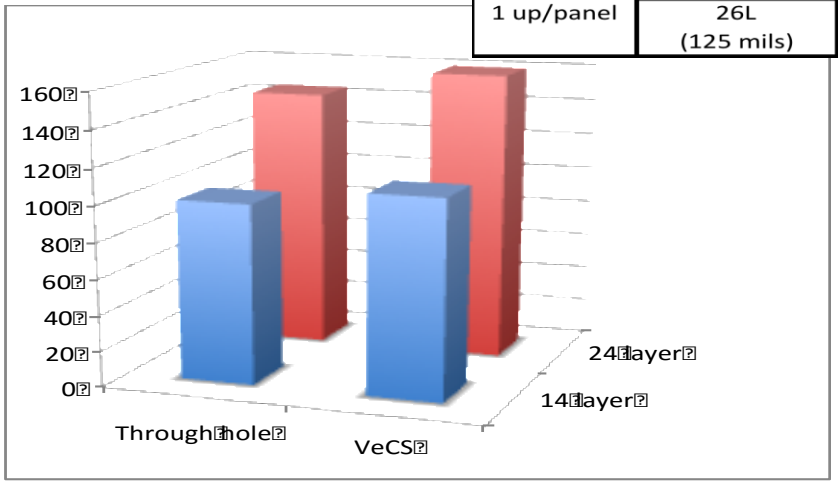
Cost comparison in detail

Cost [USD]

Mid Cost Material	Layer	No VeCS				VeCS			
		BOM	SUP	VOH	FOH	BOM	SUP	VOH	FOH
EM 888 16x18 1 up/panel	14L (100 mils)	42%	20%	21%	17%	38%	22%	24%	16%
		$100				$110			
	24L (120 mils)	49%	19%	21%	11%	45%	22%	23%	10%
		$145				$160			

High Cost Material		No VeCS				VeCS			
		BOM	SUP	VOH	FOH	BOM	SUP	VOH	FOH
Megtron 6 18x24 1 up/panel	16L (100 mils)	70%	9%	5%	16%	64%	12%	8%	16%
		$300				$330			
	26L (125 mils)	81%	7%	4%	8%	73%	10%	7%	10%
		$480				$528			



Legenda
BOM: Bill of Materials (direct materials)
SUP: Supplies (indriect materials)
VOH: Variable OverHead
FOH: Fixed OverHead

State of VeCS technology

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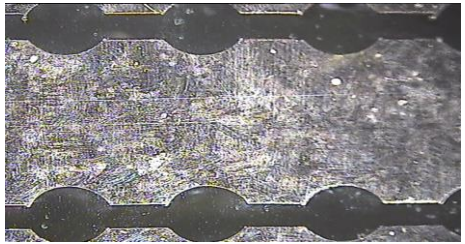
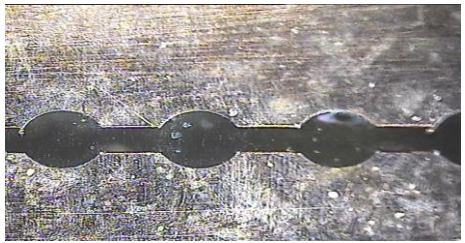
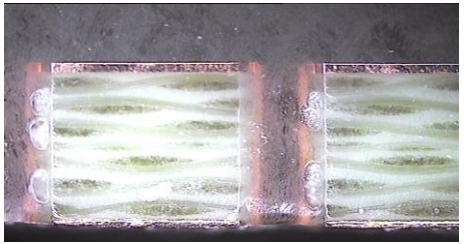
Initial results from Proof Of Concept

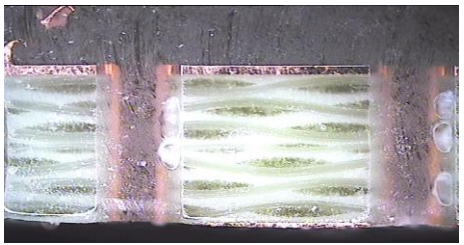
Top view after plate second drill, Cavity size 0,3mm, 2nd drill diameter 0,6 mm



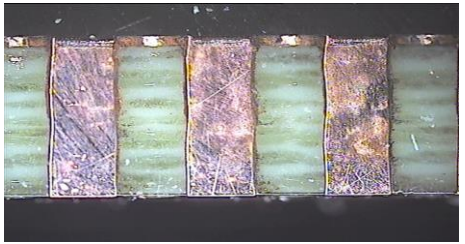


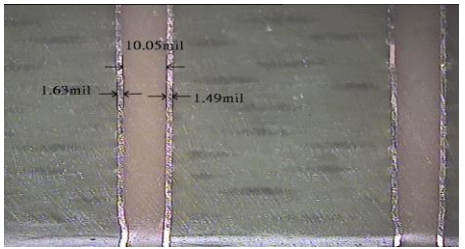
Cross section showing two sides of cavity





Cross section showing Vertical conductive structure





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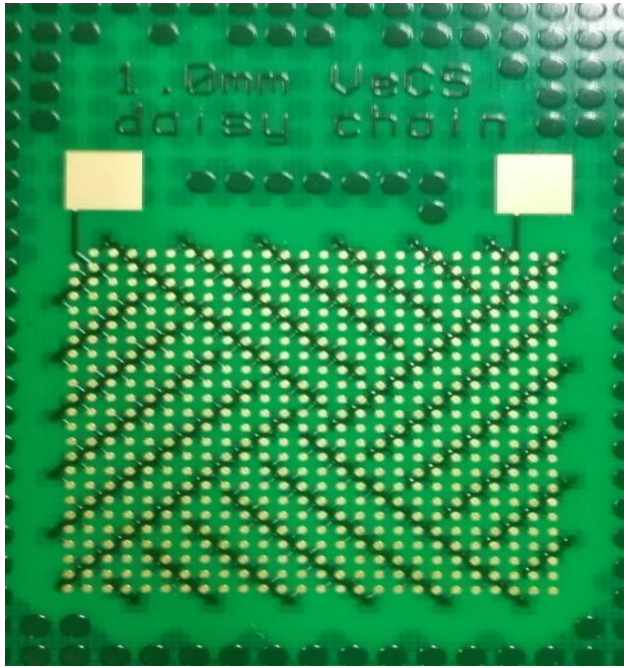
Manufacturing Examples

- 12 Layer Test Board, 2.2 mm thick, Megtron 6
- 0.5mm, 0.75mm, 0.8mm and 1.0mm BGA on a single panel
- Test vehicles are exposed to 6x reflow at 288 degree Celcius, not deviations found after cross section.



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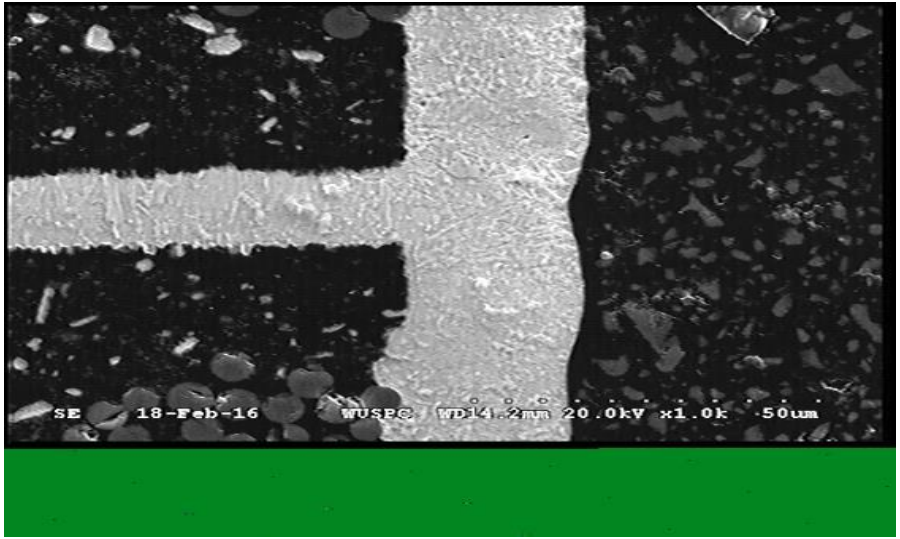
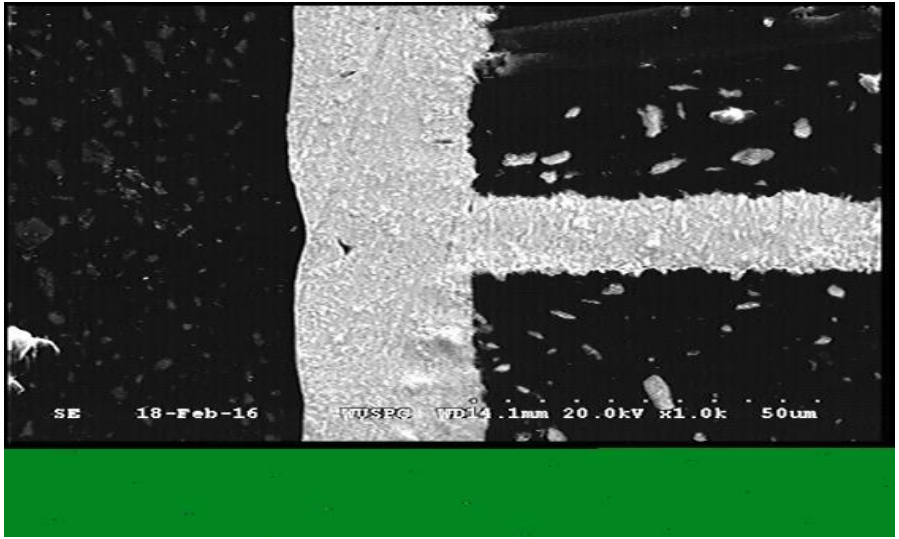
Examples after solder shock (6x)





VeCS

Signal Integrity performance

TDR measurements first prototype

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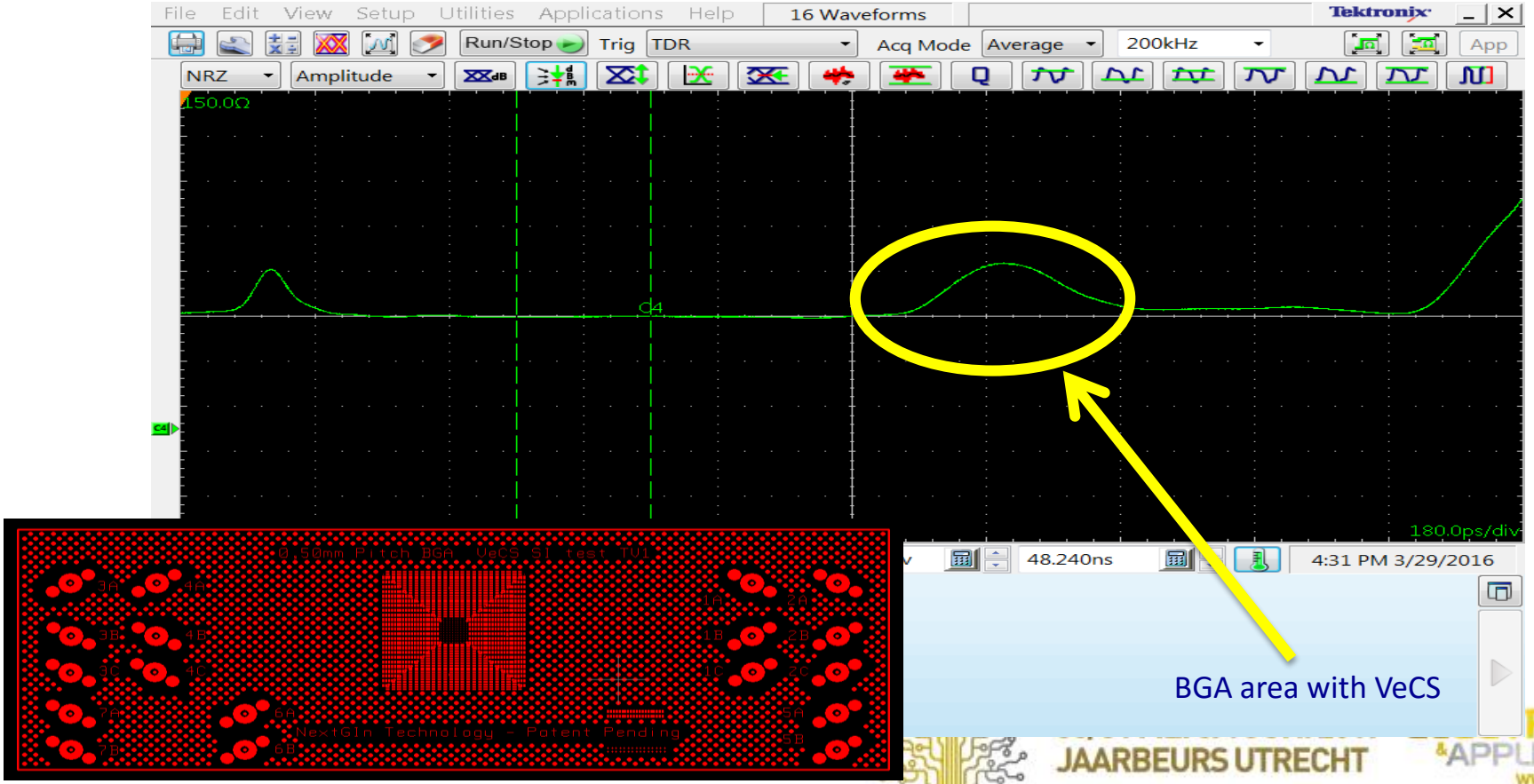
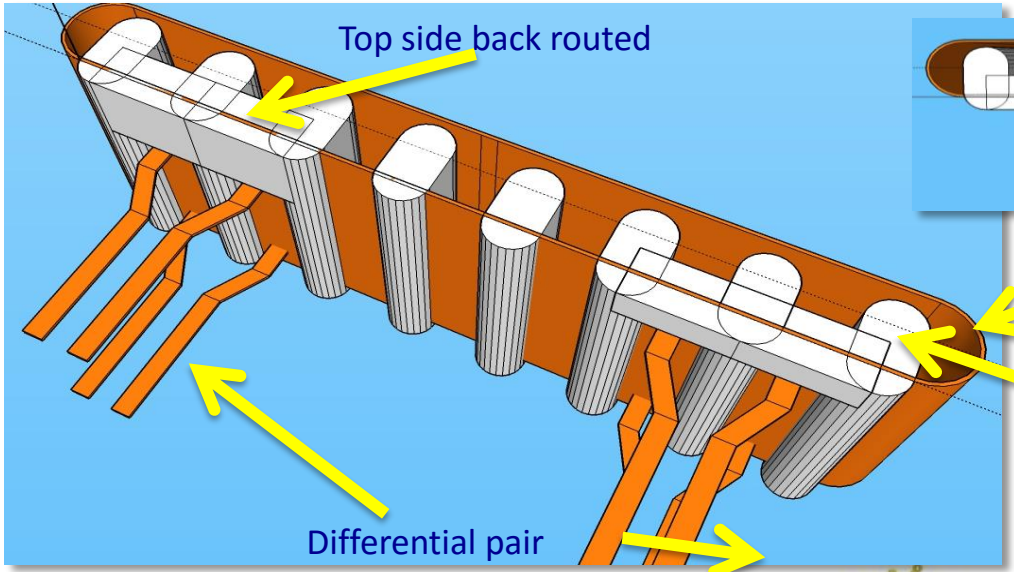
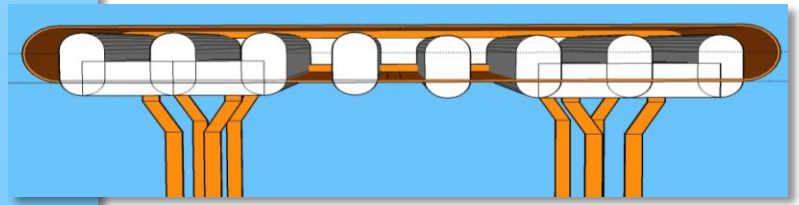


Transparant layer transition

Objective:
Create a non-reflective layer transition in order to re-introduce Via/VeCS-stitching to minimize point to point topology.



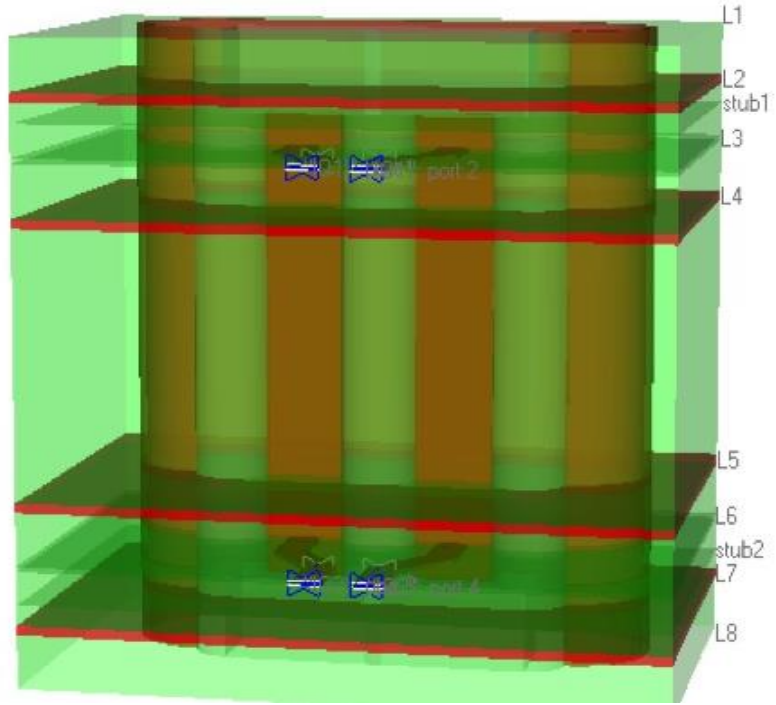


Plated slot

2nd route

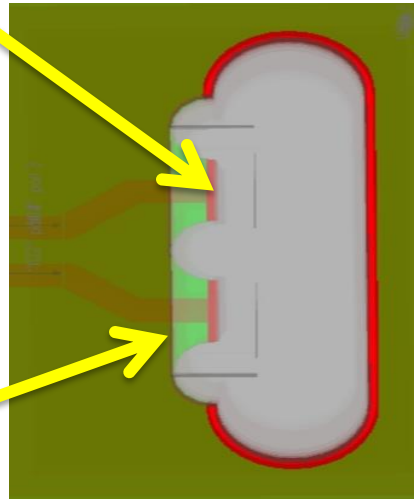
SMA connector forhigh frequency

Transparant layer transition



Vertical traces of the differential pair.

Anti-pad



Top view

The VeCS model is created in Simbeor for Si simulations

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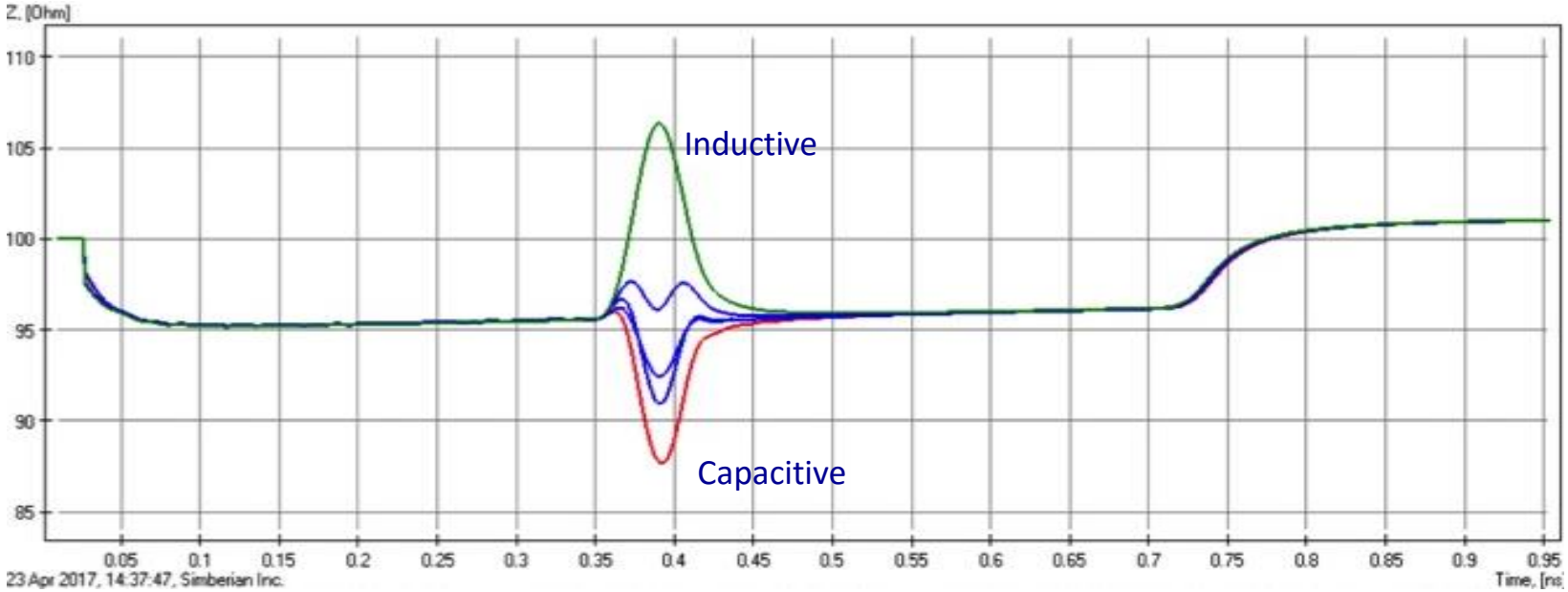
Transparant layer transition



TDR response shows simulations for different trace widths and anti-pad sizes going from Capacitive to Inductive.
The VeCS-2 element we can tune close to a “transparent”, non reflective element.

Simulations made using Simbeor

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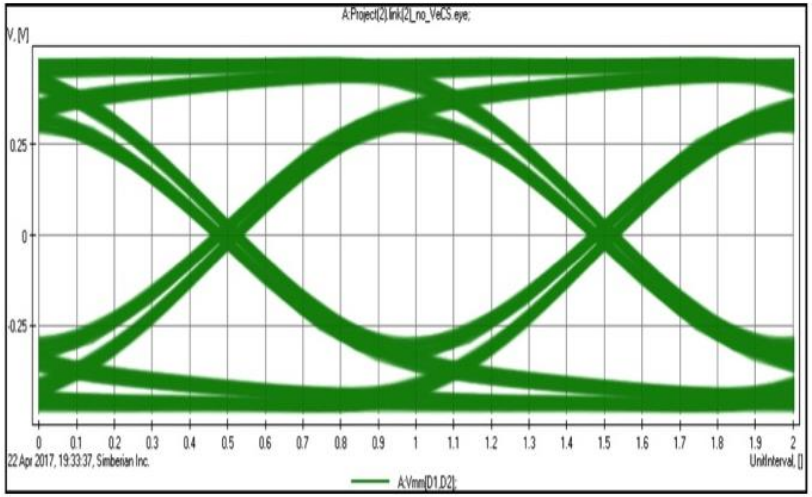
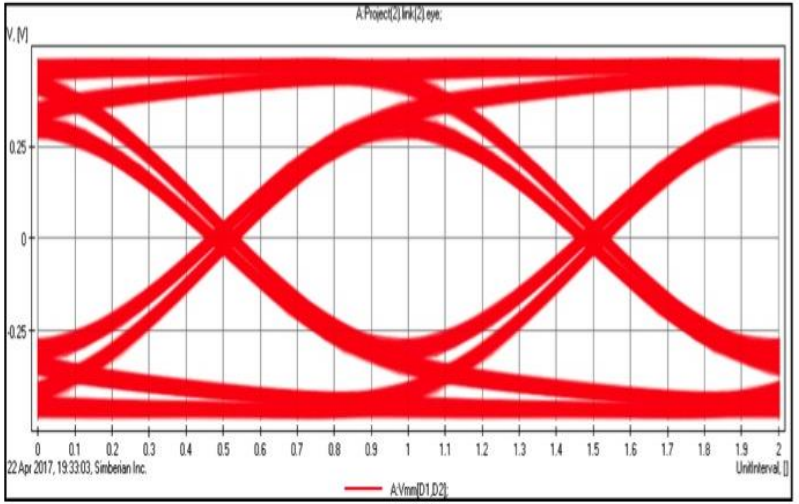
Transparant layer transition

Eye-diagram simulation at 30Gb/S

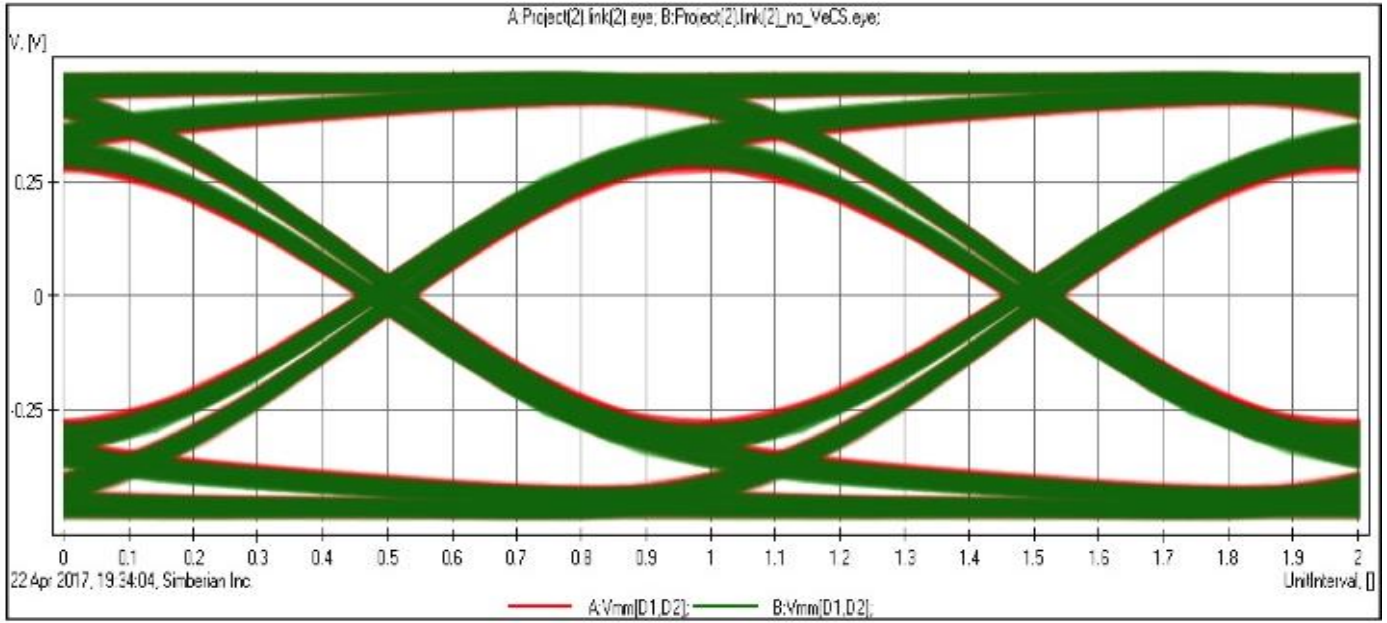


Eye diagram of launch signal



Eye diagram of exit signal

Transparant layer transition



Input and output eye-diagrams superimposed.
The (red) eye is just slight smaller then the input diagram.

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Connection to the Next Level

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