

Submicron Bonding

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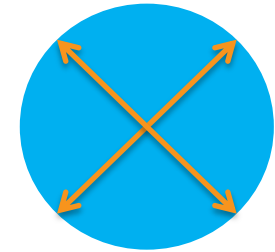
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Passive vs. Active Alignment

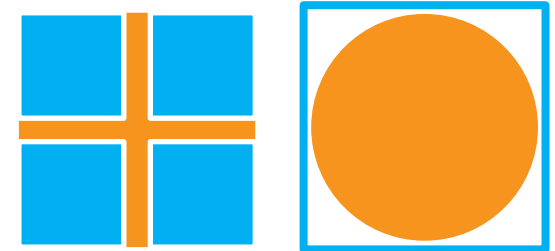
Passive Alignment	Active Alignment
<ul style="list-style-type: none">• No activation of components and measuring → simpler equipment• Flexible → machine config. remains the same when changing components (e.g. chip to lens)• Faster <p data-bbox="421 945 550 991">Chips</p>	<ul style="list-style-type: none">• No reference structures needed → simpler material design• No need to determine accuracies → Short tolerance chains• No dependency on material tolerances• No dependency on optical resolution <p data-bbox="1136 945 1483 991">Fibres or lenses</p>

Requirements on material for passive submicron bonding

- References / alignment marks must be unique, intact, sharp and clearly visible
 - Mechanical references (edge, corner, holes) are usually not convenient → chamfers, irregularities
 - References must not be too far apart from each other
- A circle is the most efficient mark for automatic alignment (only variable is diameter)
- A cross in a matrix or circle in box is convenient for manual alignment (align cross, so that minimum of light is visible between cross and matrix)



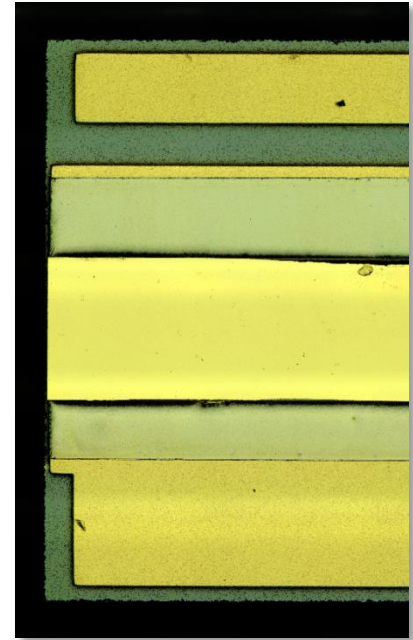
Fiducial for automatic alignment



Fiducials for manual alignment

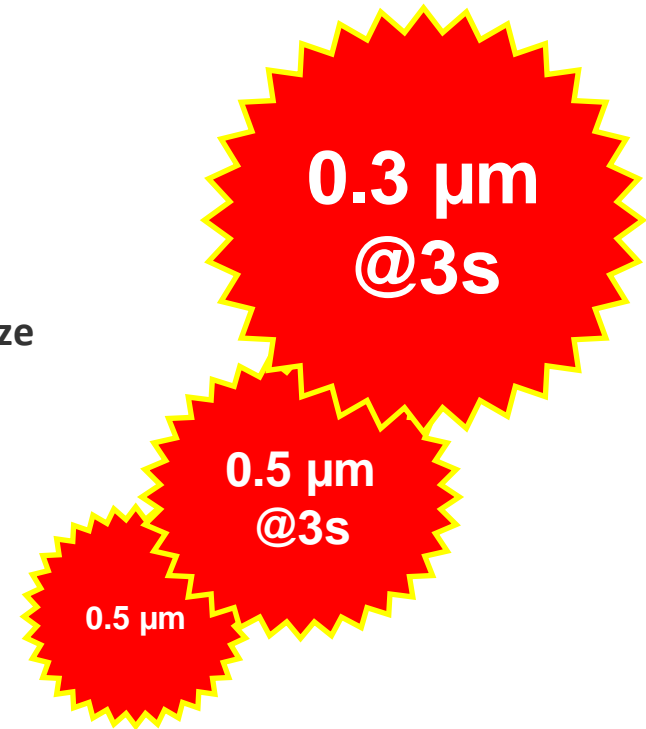
Requirements on application and machine for passive submicron bonding

- Reference should be in plane with the important / active structures
 - On chip due to tolerances of layer overlapping
 - On substrate to avoid motion in Z
- The tolerance chain must be as short as possible
 - Inside machine the e.g. minimize the number of moved axis
- Decouple force application and alignment / placement mechanism
- Mechanical tolerances must be minimized and compensated
 - E.g. inside tooling with gimbals
 - Incl. material tolerances



Machine capability and post bond accuracy

- Machine specification reflects only the capability of the machine
- Process parameters introduce additional inaccuracies!
- **The challenge is to minimize this influence and so maximize post bond accuracy**
- Processes that are not suitable for submicron post bond accuracy
 - Ultra sonic bonding → US movement of several microns
 - FC soldering → self alignment of chip
→ works if FC is kept in place during soldering
 - All processes with high forces

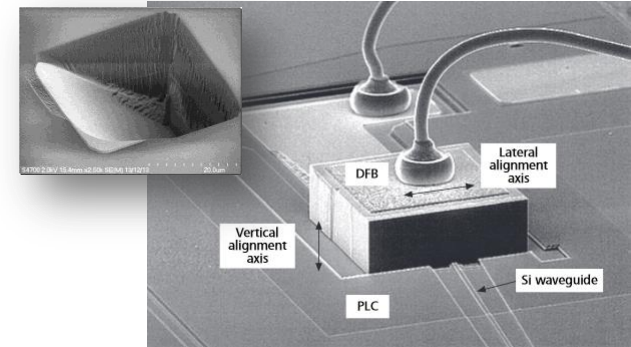
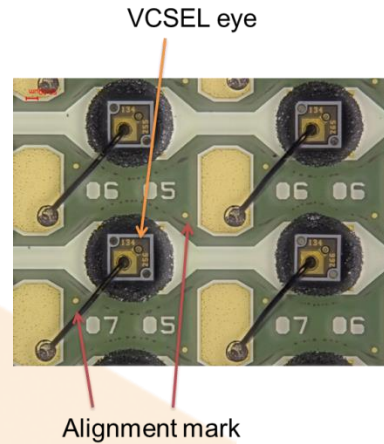
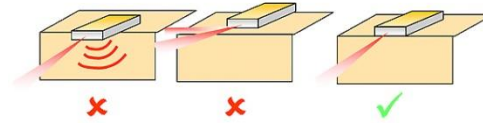


What are potential root causes for inaccuracies

- Gluing processes
 - Glue flows after chip has been placed e.g. due to surface tension or when cured
 - Glue shrinks
- Soldering processes
 - Temperature drift of machine parts like heating plate or placement tool / arm during soldering profile
 - Temperature expansion of substrate and chip → connection is made at a higher temperature than alignment
- Welding processes
 - Large number of bumps require high force, which causes machine parts to deform
- Material requirements from slide 2 not kept

Where is submicron bonding used?

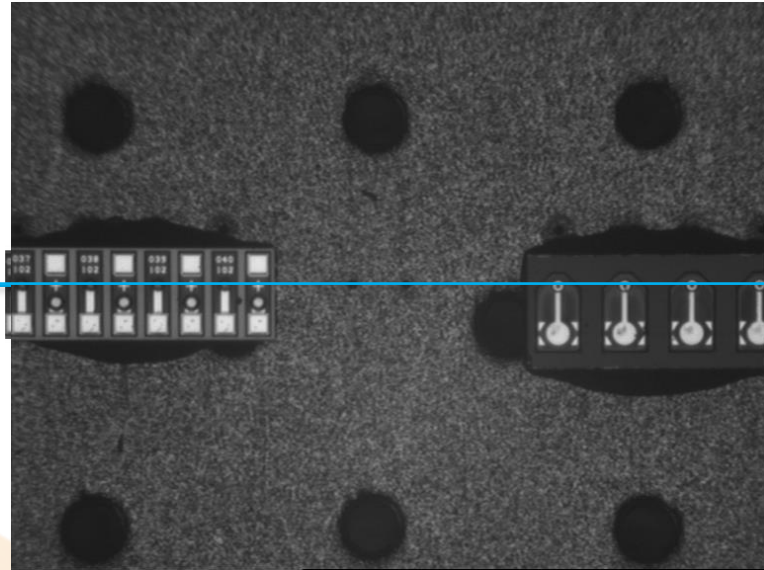
- Laserbar bonding
- VCSEL and PD (arrays)
- Dies on PLC
- Wafer level fan out



Transceiver – VCSEL and PD arrays

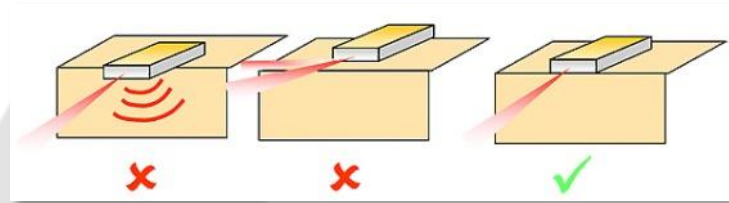
Sufficient relative placement accuracy to be able to put one single lens / fibre array on top

- First component is aligned to pattern on substrate
- Second component is aligned to first one
- Defined distance and orientation

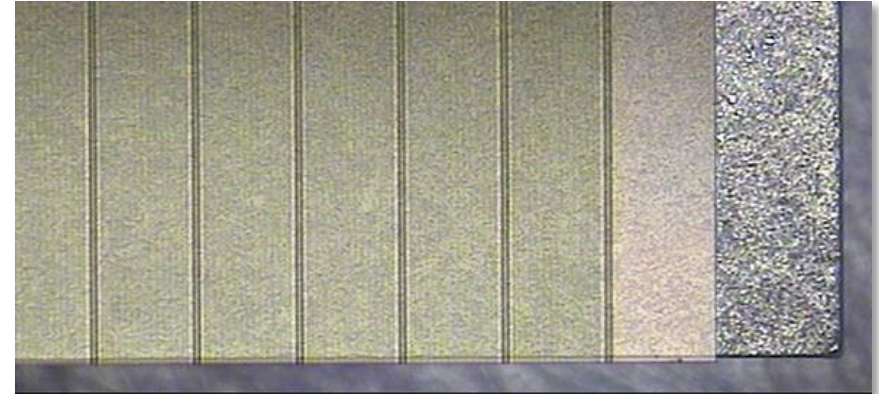
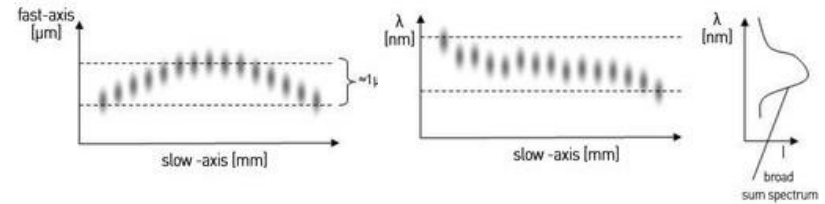
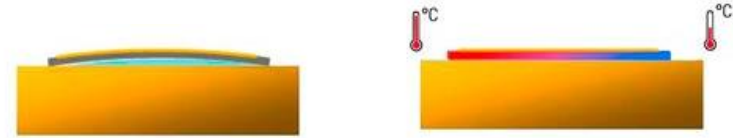


Laserbar bonding

- Light exits on bottom side of laser bar



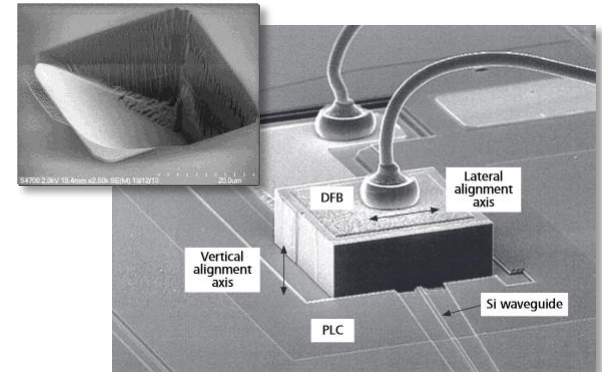
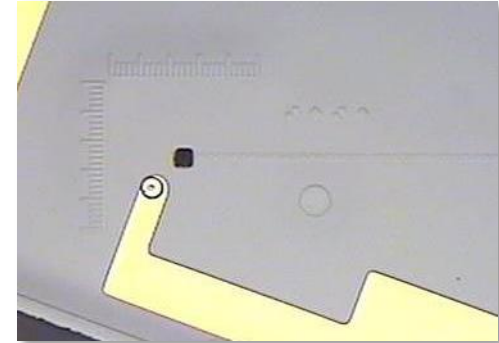
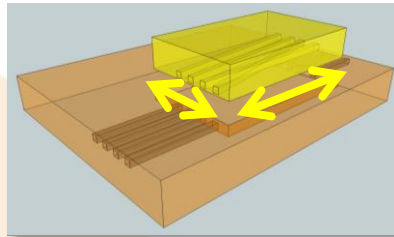
- Alignment of facet to edge of heat sink
- Placement and soldering of die
 - Minimize temperature drift
 - Avoid oxidation / reduce oxides
 - Homogenous solder thickness
 - Avoid smile effect



PLC bonding

Planar lightguide circuit

- Alignment marks from same masks as lightwave guide structures
- Bonding in plane or out of plane
- Passive optical alignment in XY
- End stops in Z



How accurately has the chip been placed?

- Checking a placement accuracy of 1 μm , requires a measurement system of
 - 0.1 μm resolution
 - this is only possible with a superior measurement optics + subpixeling in the pattern recognition
 - If there is **no systematic error** in the measurement the standard deviation of the measurement values must be $<0.33\mu\text{m}$ ($3s, cg=1$)
 - This is only possible when all references are in the same field of view
 - 2,7 % of chips which are placed perfectly are measured out of spec
- Nonius scales are more reliable but give no statistics

