LAN-Party at your Lab

Jan Zegers
Geert Verbruggen
FPGA for real-time data processing
Electronics & Applications
May 30 – June 1, 2017

easics

independent
SoC design
company

- ASIC
- FPGA
- embedded
software

spin-off company of

- imec
- KU Leuven - ESAT

25 YEARS
Founded in 1991

easics

Located at the Arenberg Science Park in Leuven, Belgium

About Easics

Easics is a **System-on-Chip design** company, targeting designs in digital & mixed-signal **ASICs** and **FPGAs**, and embedded software.

Easics designs **reliable** and **scalable high-performance & low-power** embedded systems

for **leading product companies** active in

wired & wireless connectivity, imaging / image sensors, multimedia, broadcast, industrial, medical / healthcare, (aero)space, and measurement equipment

Customers:

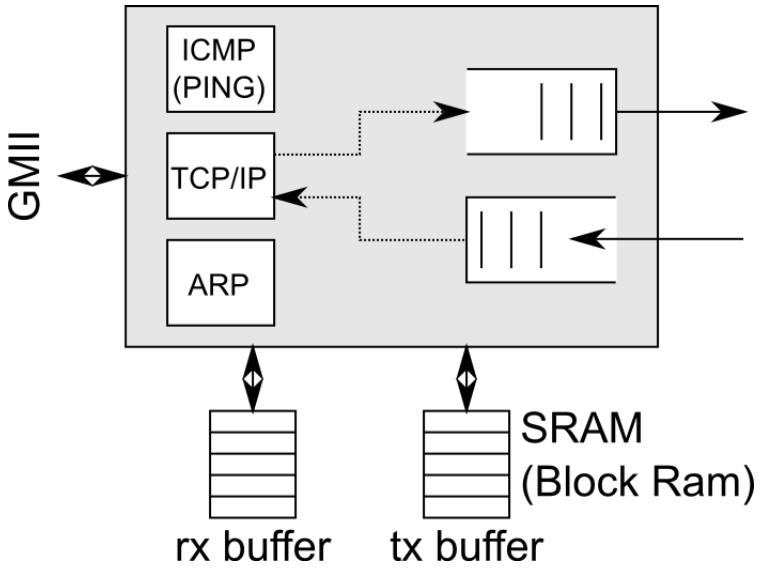
- ► OEMs: electronics, optics, mechanics
- ► Semiconductor companies
- ► Analog / Mixed-signal IC design houses

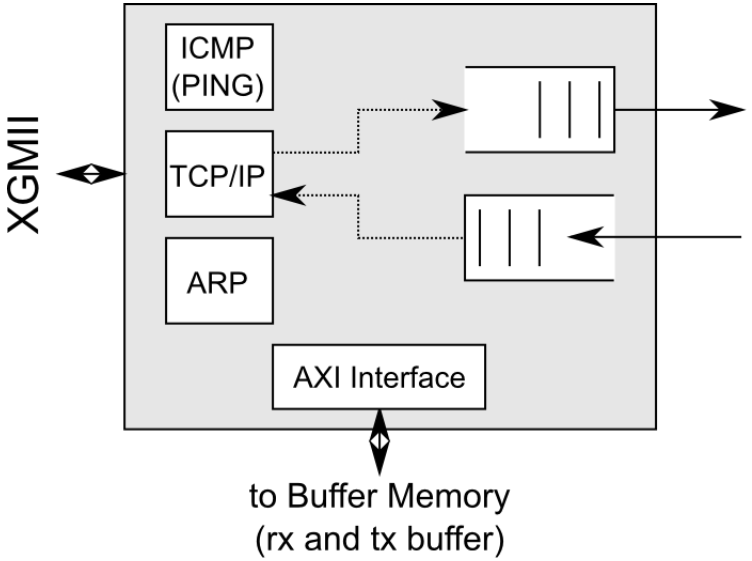
Easics Customers

Background

- Need for a debug/verification interface for control AND data
  - High bandwidth is needed, interfaces like UART are not sufficient
- Reliable
  - No data loss
- Possibility to interface with a variety of platforms (Linux, Windows, ...)
- Interfaces available on PC and standard FPGA development boards
- Easy to use from test software
  - C/C++ as well as scripting languages
  - Use of standard drivers
- Small footprint
  - To be added on top of a design

Easics TCP/IP core

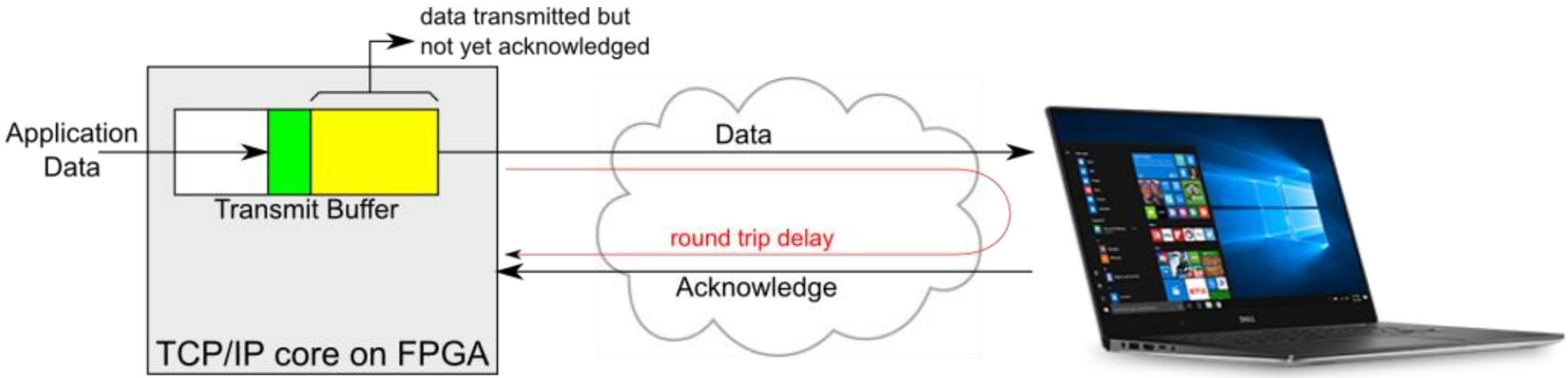




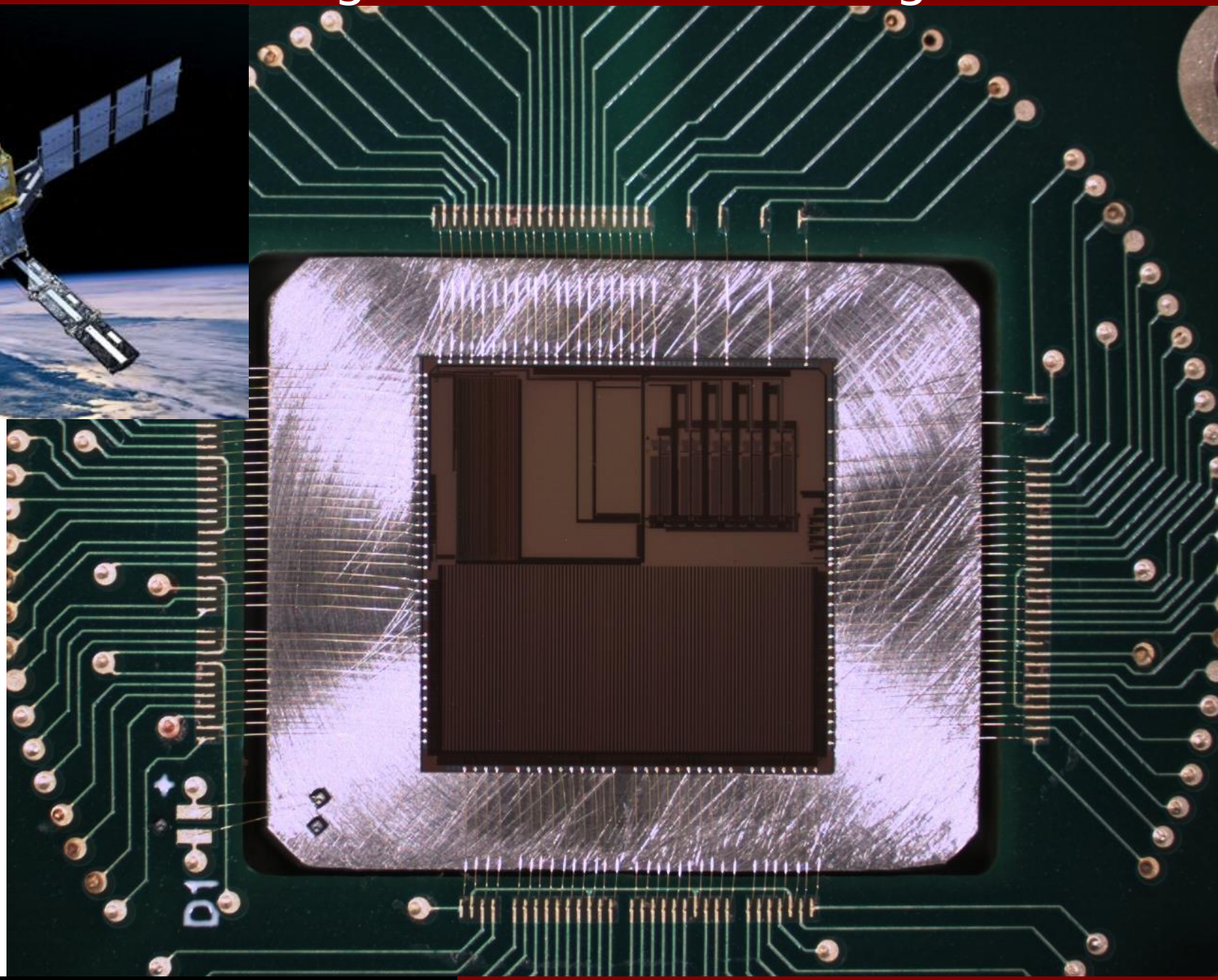
- 1G and 10G versions available
- Acts as a TCP Server
  - PC can connect to it, opening a TCP socket
- Single or multiple connections
- Responds to PING requests
- Responds to ARP requests (mapping of IP to MAC address)
- Small Footprint: no processor involved
- Full implementation of the TCP/IP stack
- Easy to integrate

Low Latency is requirement for small Footprint

- Sender needs to keep transmitted data until acknowledged
- Transmit buffer size determined by Bandwidth x Latency product
  - Latency = transmit path latency + round trip delay + receive path (+interpretation!) latency

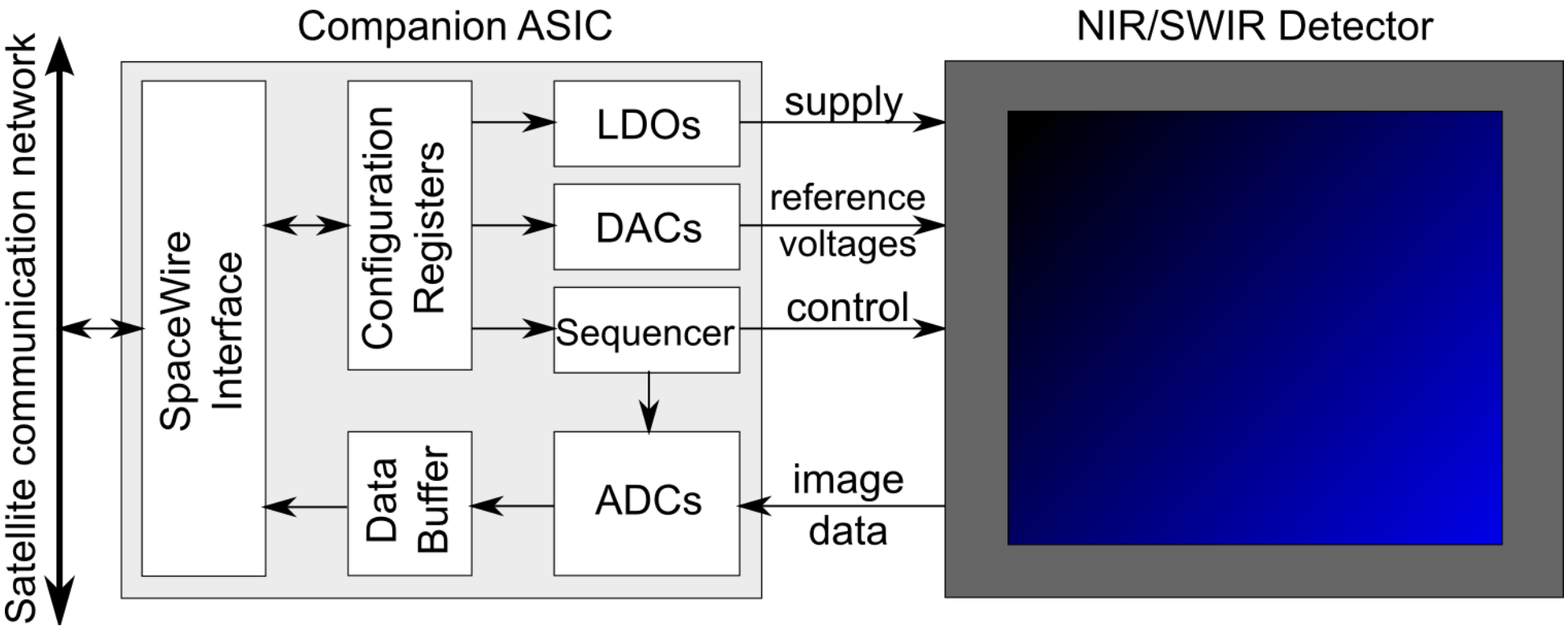


Example 1: Test setup for Companion ASIC for high-end scientific image sensors



Companion ASIC Function

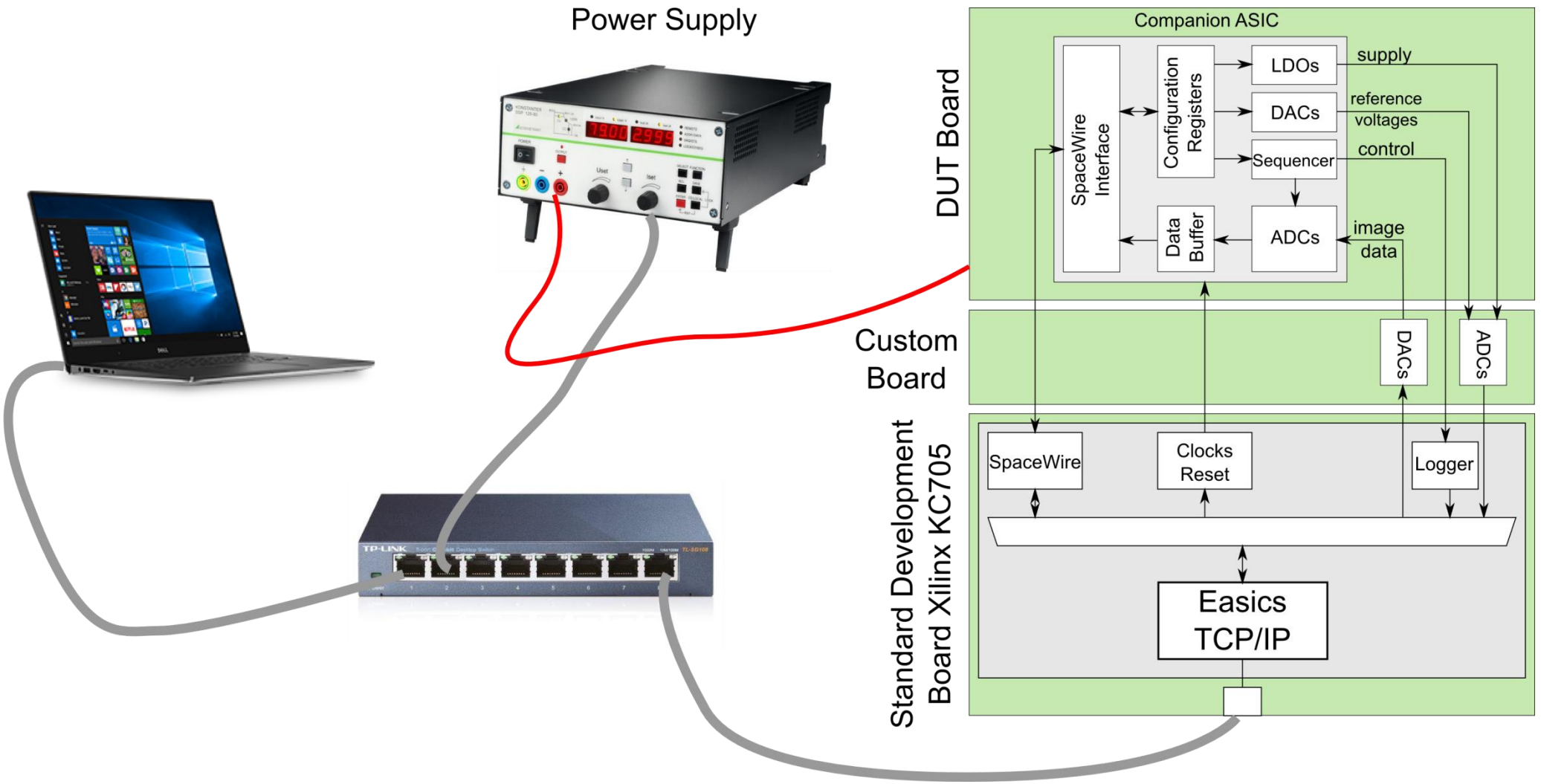
- Bridge between Satellite communication network and analog detector



Challenges

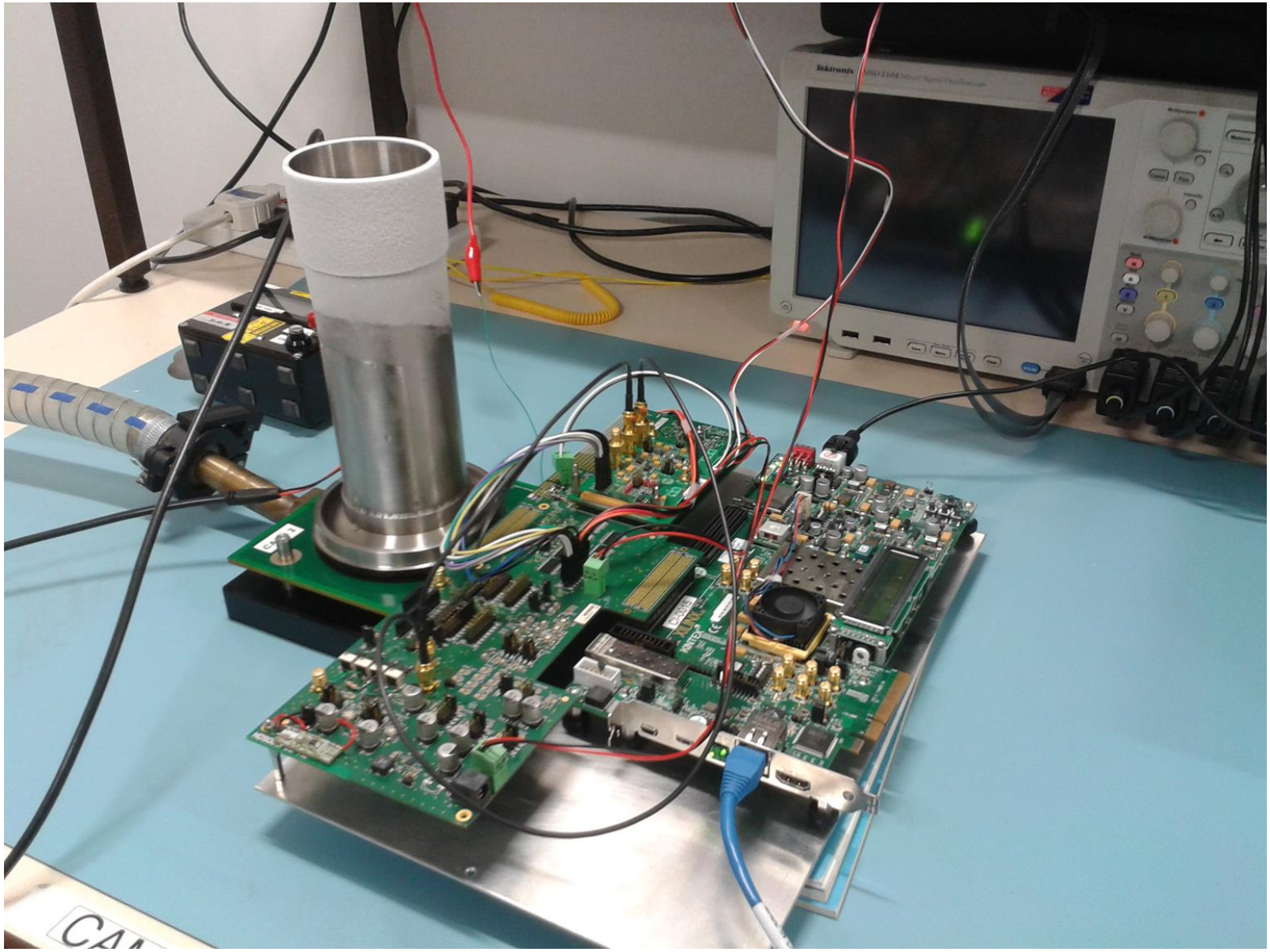
- Companion ASIC surrounding components were not available
  - Detector chips were still under development
  - SpaceWire network was not yet known
- Budget is very limited
- Access to test lab for cryogenic tests and radiation test is limited/expensive
  - External facilities are used

Companion ASIC Test Setup



Companion ASIC Test Setup

Cryogenic measurement setup: ASIC in liquid nitrogen + FPGA board



Test Setup Advantages

- Cheap and compact test setup
  - Most complex PCB is an off-the-shelf Xilinx board
  - Entire test setup fits in one suitcase
- Tests are fully scripted (Python)
  - Completely tested in advance, before going to the external facilities
  - Only interaction is replacing the test samples
- Automated generation of characterization reports

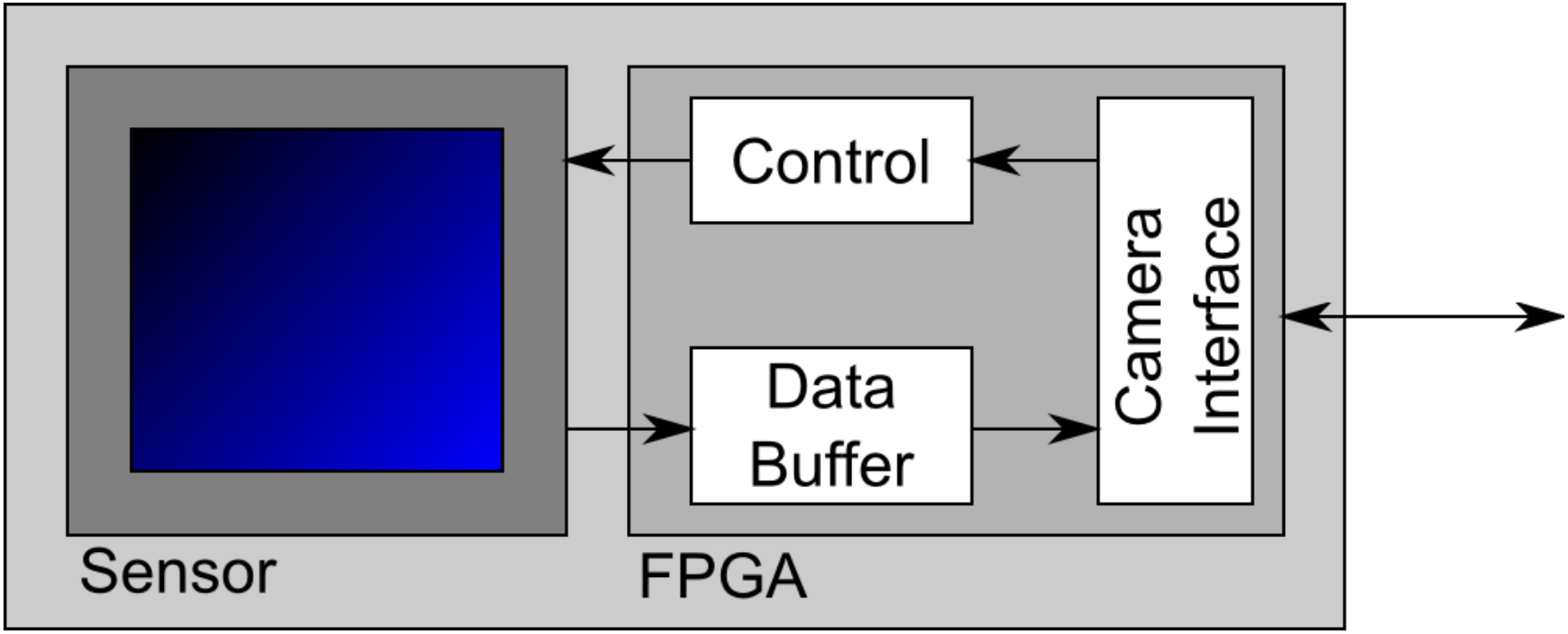
Example 2: Real-time image enhancement FPGA for thermal camera

Xenics Infrared Solutions

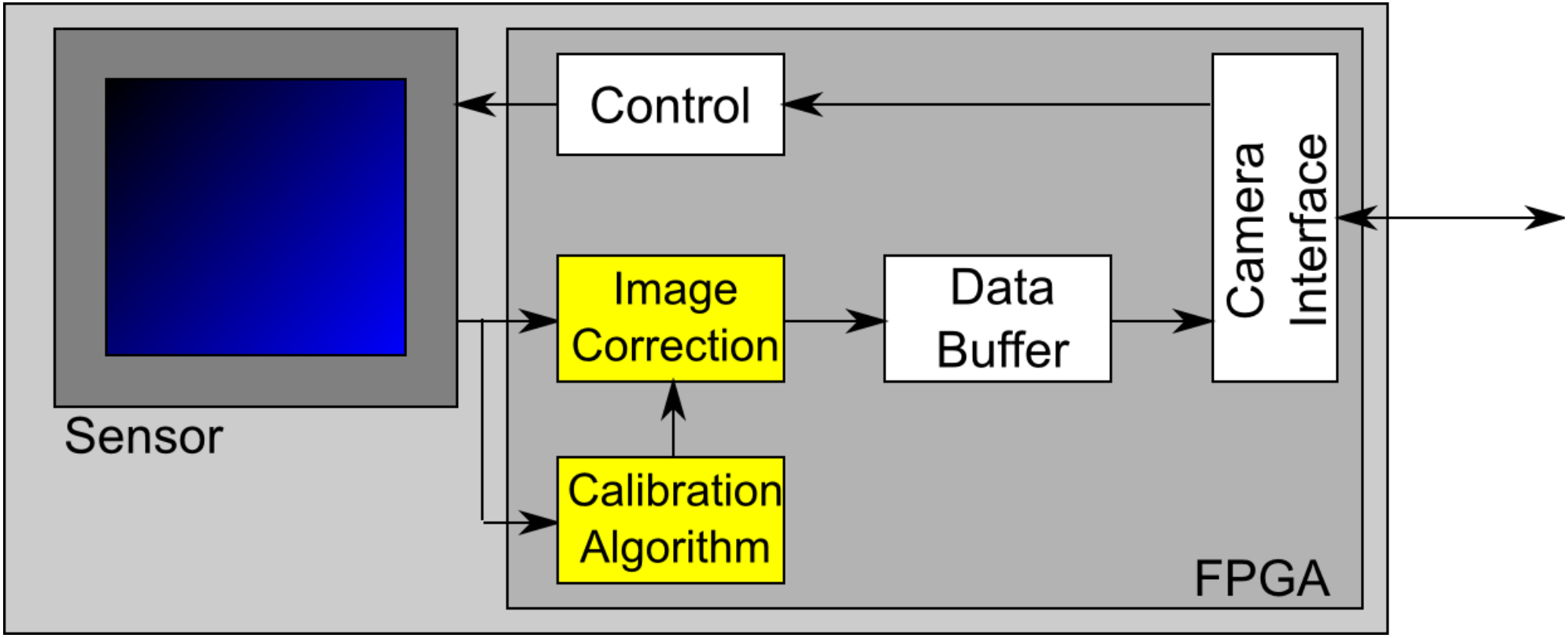
easics

- Micro Bolometer Camera generates fixed noise, due to warming up of the detector and surrounding components
- Previous solution:
  - On a regular basis close a mechanical shutter and capture a reference image. This reference image contains the noise only, and is subtracted from the images
- Disadvantages:
  - Mechanical shutter
  - Continuous capturing is not possible
- New Solution: Image adjustment parameters are determined out of real scene images (algorithm developed by Xenics) and continuously updated

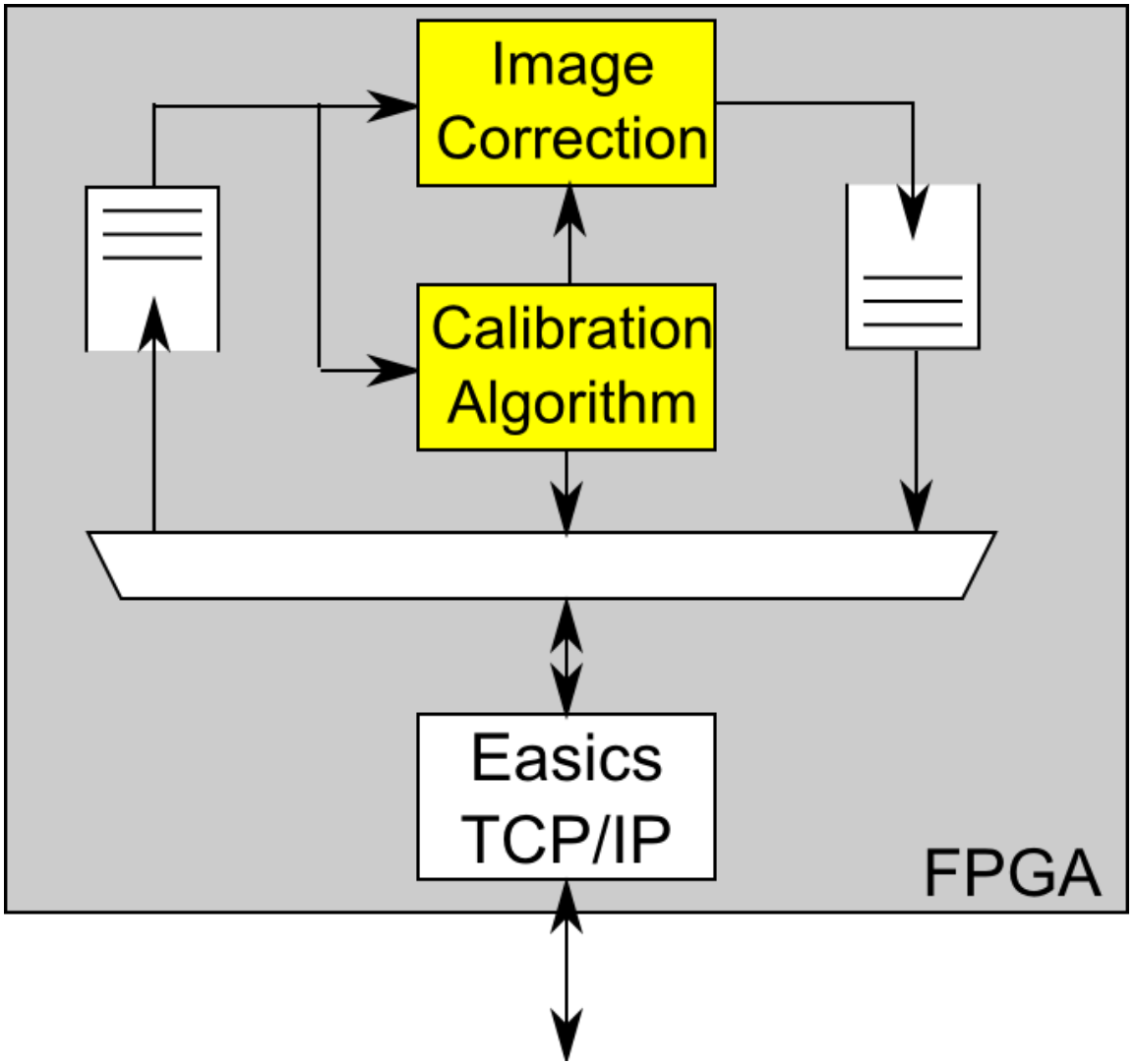
Thermal Camera: Block Diagram



Thermal Camera: New Block Diagram



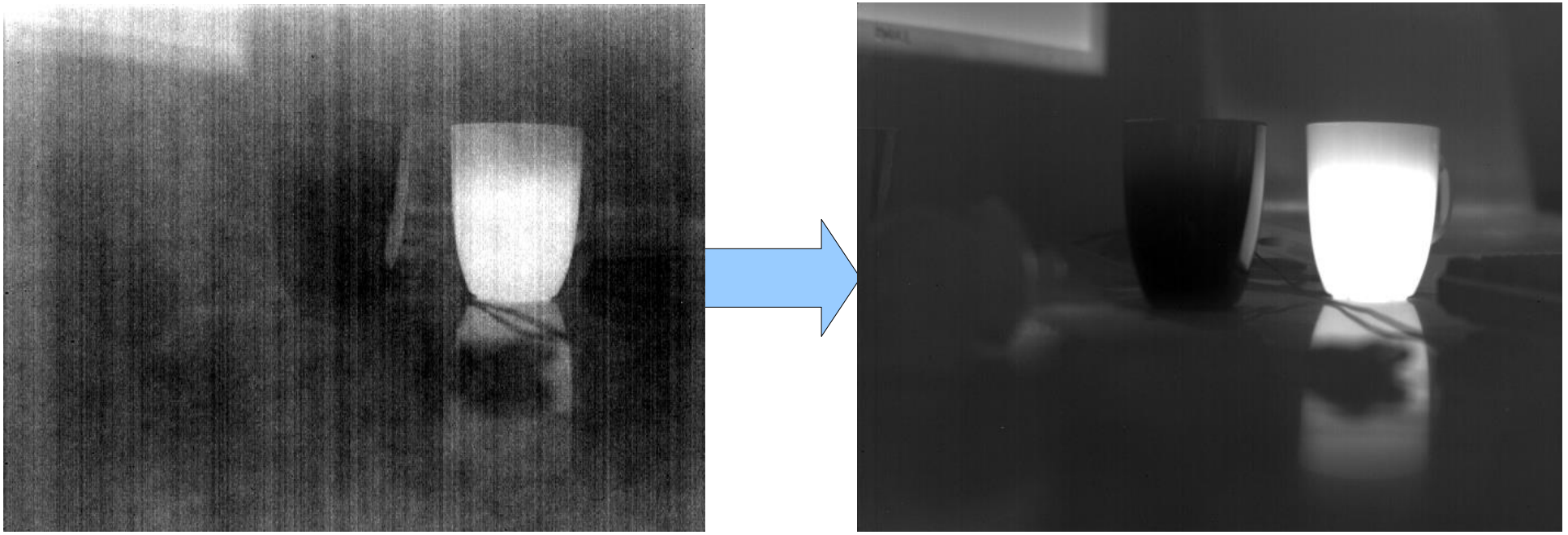
Verification Platform



Advantages

- Calibration has a long time constant
  - Too long for simulation
  - can be executed real time, using real images, captured off-line with an legacy camera
    - => realistic and deterministic setup
  - Possible to monitor calibration algorithm through debug port
- No hassle with interfaces: direct, standard connection to any PC
- Tested on an off-the-shelf FPGA Development Board
  - Before the new camera PCB has been built

Results



Easics Contact information

Easics NV
Arenberg Science Park
Gaston Geenslaan 11
3001 Leuven
Belgium

www.easics.com
@easics_nv

tel +32 16 395 611

Ramses Valvekens, CEO
ramses@easics.be

Jan Zegers, director
jan.zegers@easics.be