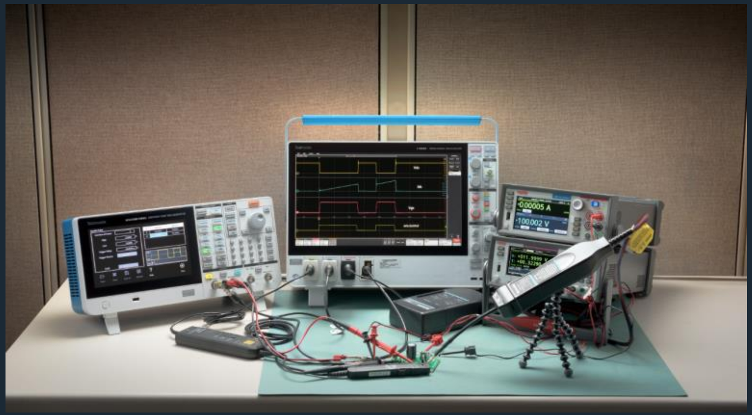


# Tektronix and CN Rood Presents

The Standard Method for Measuring Switching Parameters

E&A ELECTRONICS & APPLICATIONS '23

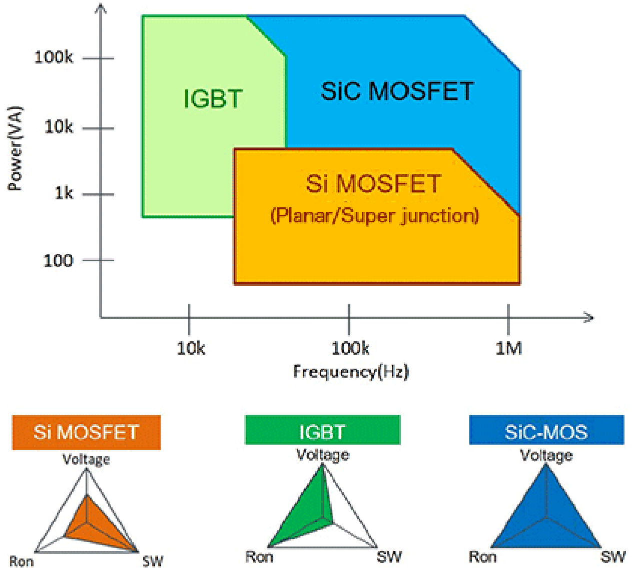
# Agenda

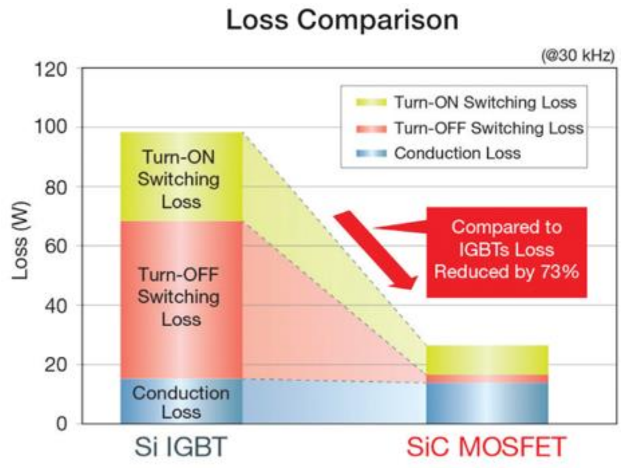
- Why  Wide Bandgap (WBG) ?
- What is Double pulse test

❑ *Principle and Key measurements*

- Measurement Challenges
  - ❑*Gate driving Stimulus, Probing ( Low /High Side) , Deskew*
- Questions

# Why Wide Bandgap?





**Higher Power Levels**
**Faster Switching speeds**

**Lower Switching Losses**

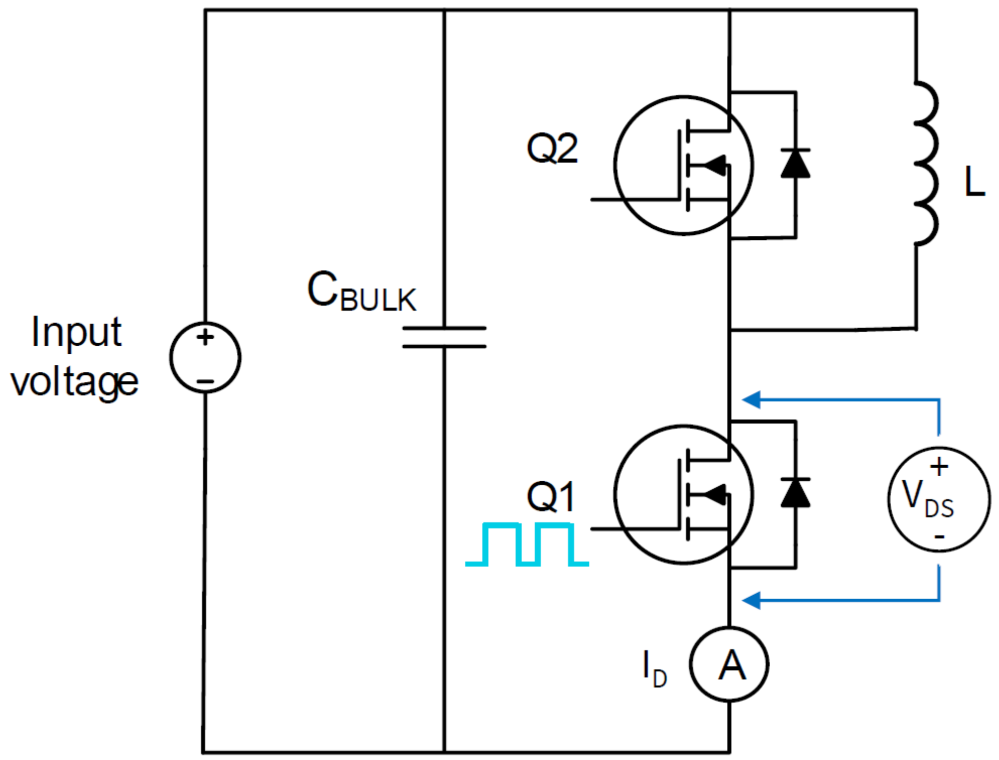
**Smaller Form Factor**

*Image source: ROHM Semiconductor*

# What is a Double Pulse Test?

# What is Double pulse test (DPT) ?

## DEFINITION




Double-Pulse Test Circuit

Evaluate and optimize the switching performance of power MOSFETs or IGBT

Why?

- Gate drive optimization
- Calculating switching losses in the final design

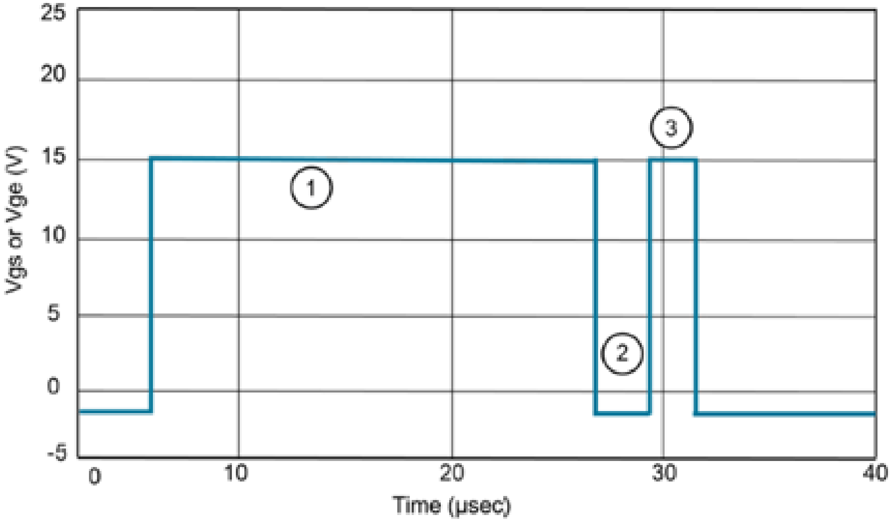
Dynamic performance evaluation over the full range of operating conditions

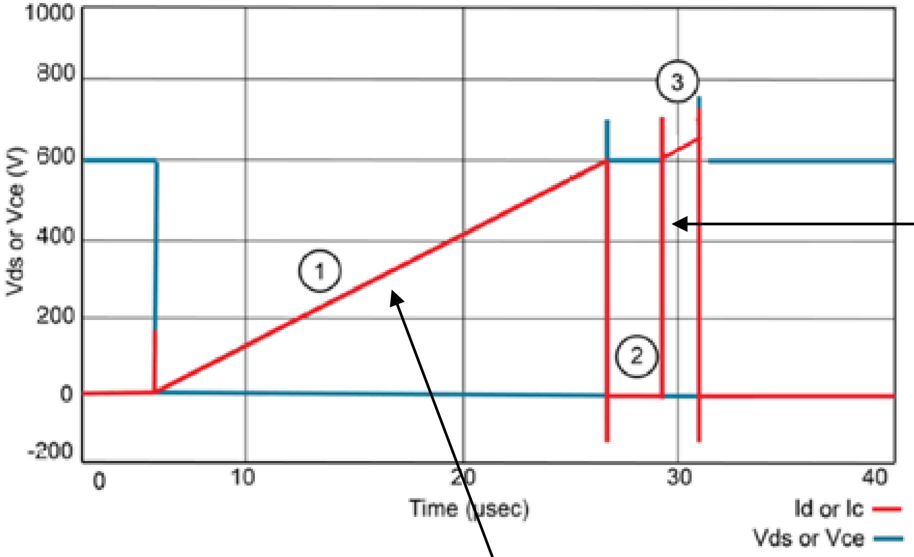
- Timing (Tdon, Tdoff, Trise, Tfall…)
- Amplitude (overshoot, ringing…)
- Speed (dI/dt, dV/dt …)
- Switching energy (Eon, Eoff, Err…)

# What is Double pulse test (DPT) ?

## DEFINITION

Q1 gate is driven with a controlled double pulse pattern, while Q2 is off



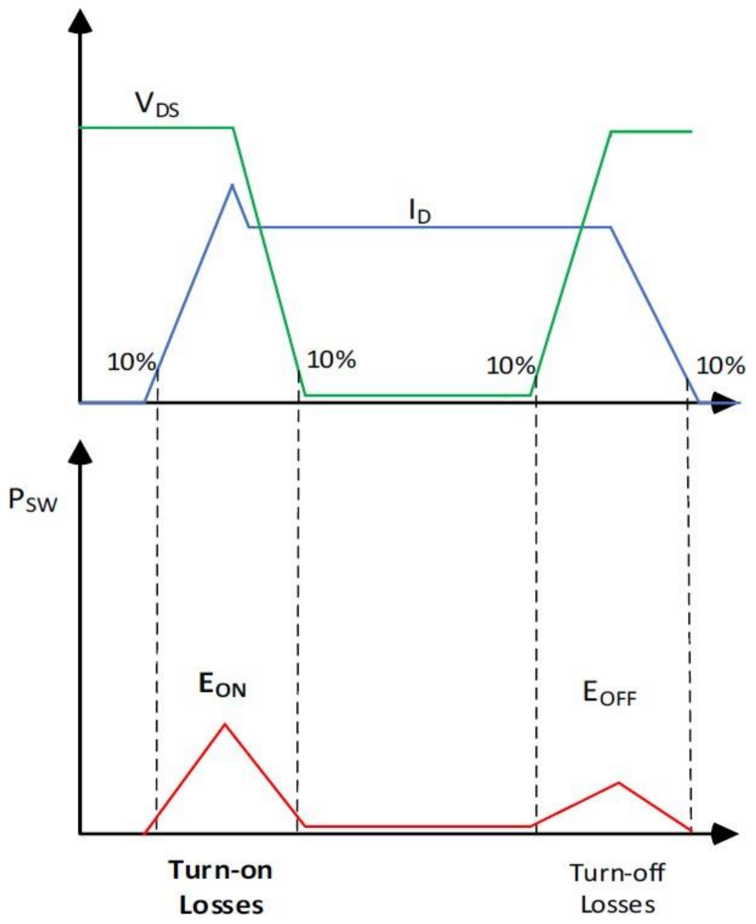




Second pulse is where the parameters are measured

During the 1st pulse the current builds through the inductor $Imax = \frac{V * \Delta t}{L}$

# What is Double pulse test (DPT) ?

## KEY MEASUREMENTS: EON, EOFF

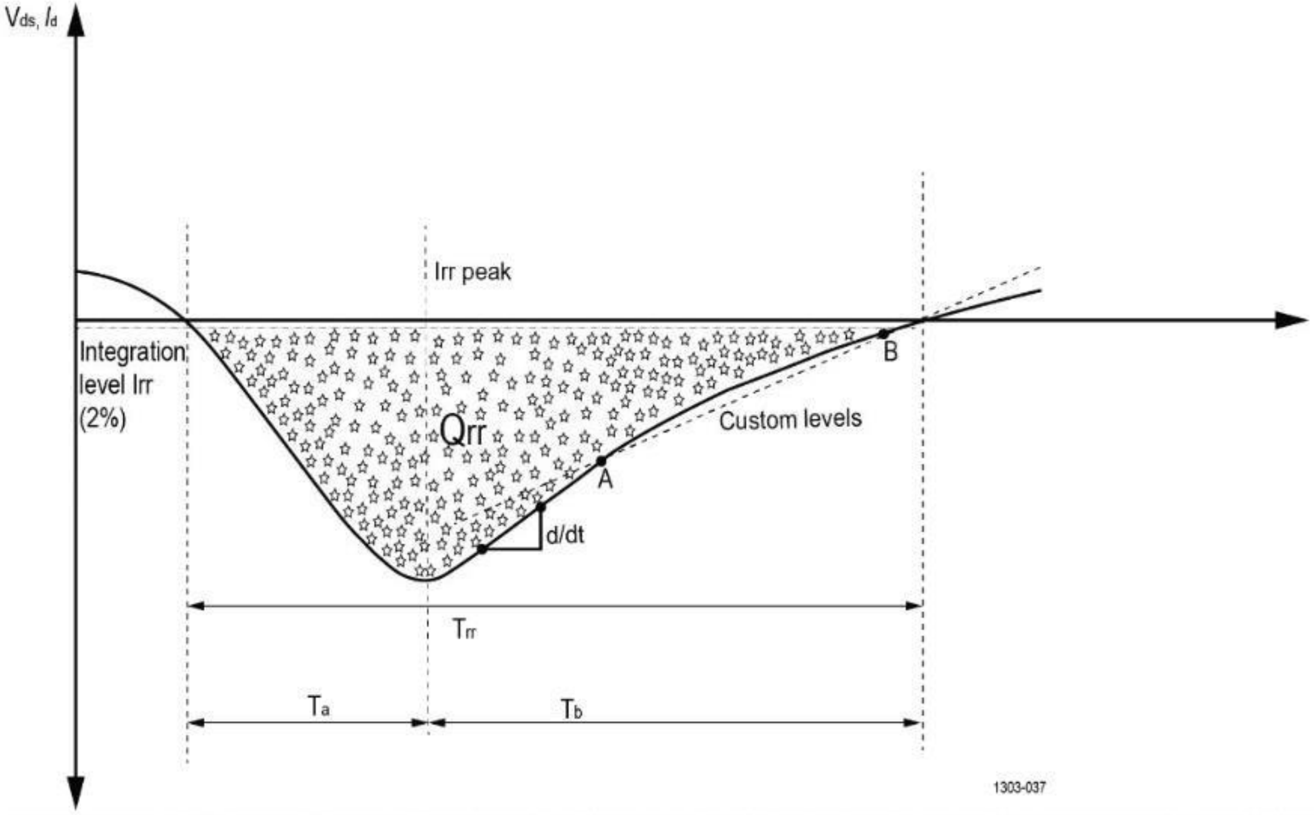



$$E_{on} = \int_{10\%\, Ids}^{10\%\, Vds} V_{DS} \times I_{DS}$$

$$E_{off} = \int_{10\%\, Vds}^{10\%\, Ids} V_{DS} \times I_{DS}$$

# What is Double pulse test (DPT) ?

## KEY MEASUREMENTS: REVERSE RECOVERY

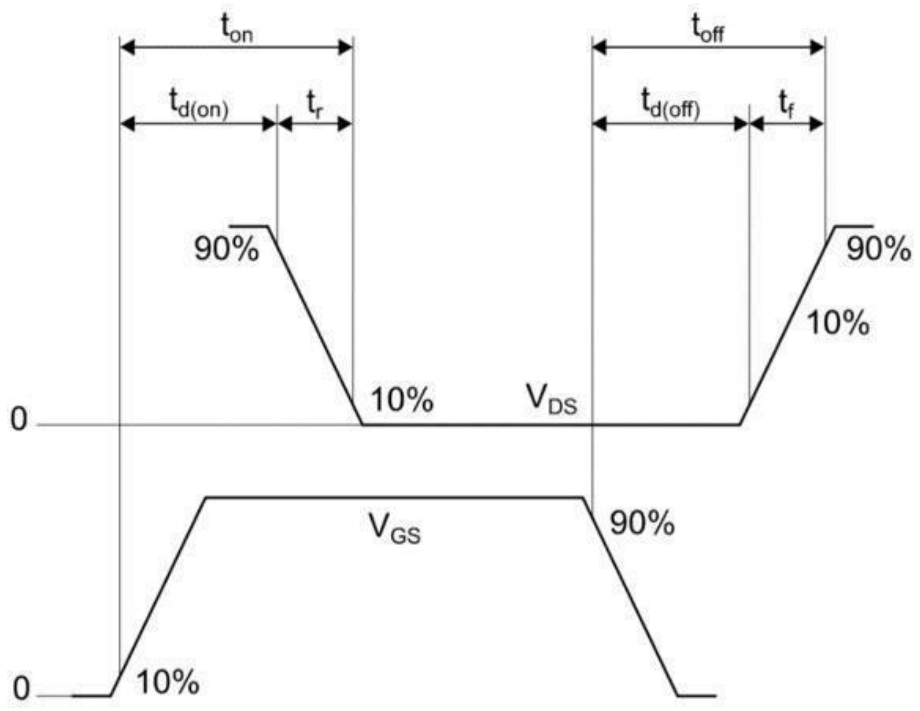



$$Qrr = \int_{t_0}^{t_0+t_i} Irr \times dt$$

$$Err = \int_{t_0}^{t_0+t_i} V_R \times Irr \times dt$$

# What is Double pulse test (DPT) ?

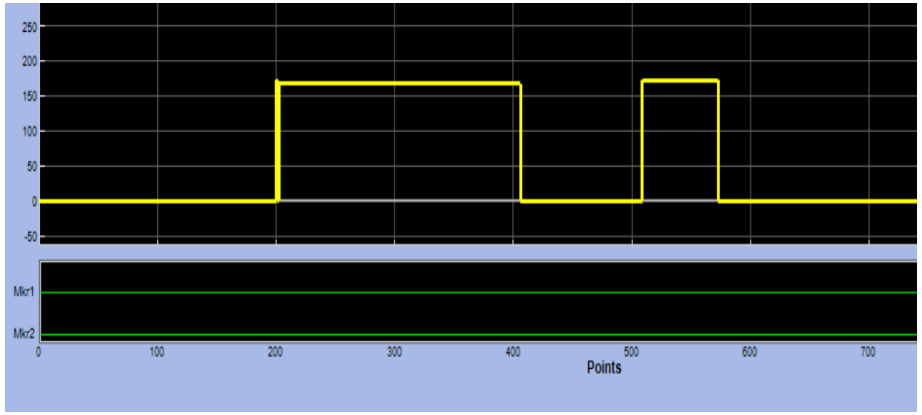
## KEY MEASUREMENTS: TIMING

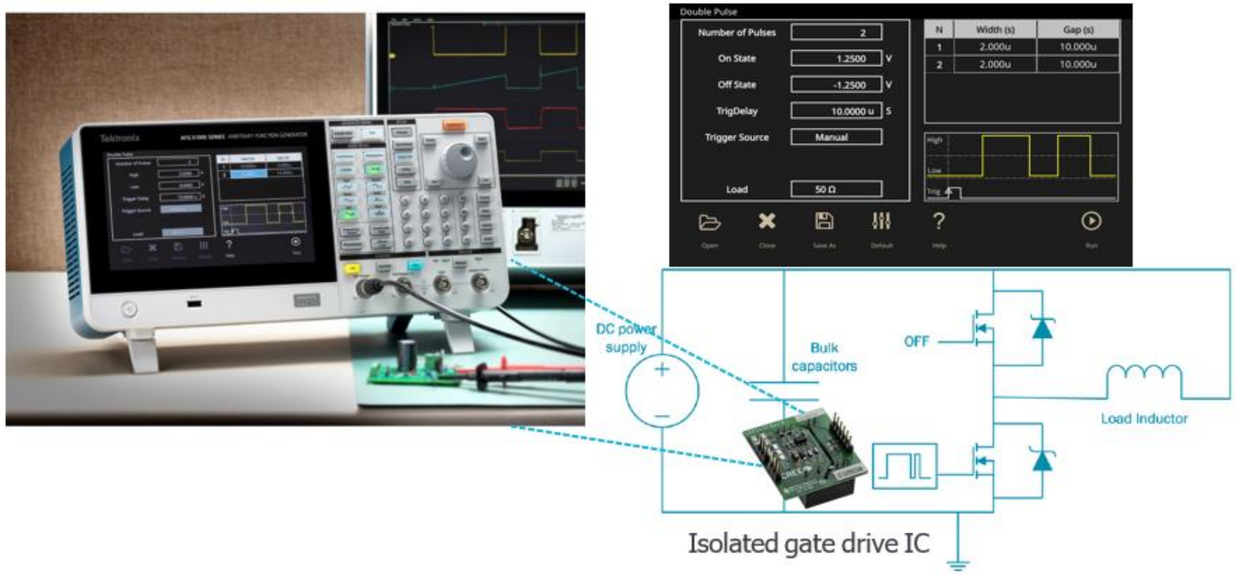


# Measurement Challenges

# How to drive the gate?

- Traditional function generator cannot control each pulse width individually
- Using PC to create arbitrary waveforms and load them onto the AFG is cumbersome and time consuming
- Using uC requires the user to write code. Off the shelf solutions lack flexibility



# The importance of probing

# The importance of probing

## BANDWIDTH

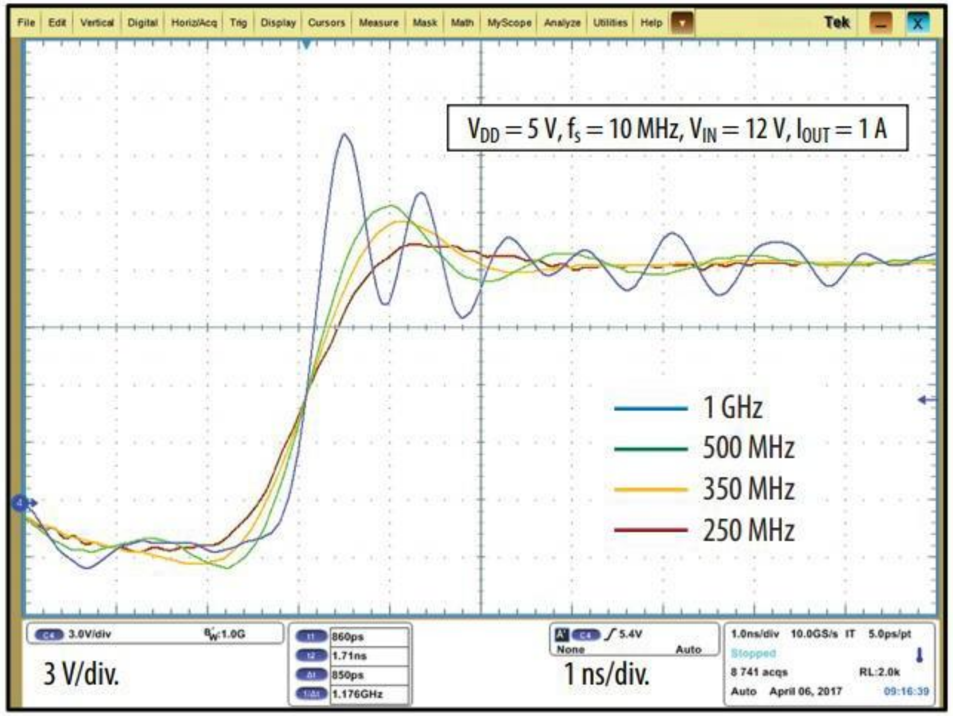



*Figure 3: Effect of probe/system bandwidth on captured waveform (EPC8009 based board).*

$$t_{r(probe)} = \frac{0.3 \ldots 0.4}{BW}$$

$$t_{r(measured)} = \sqrt{{t_{r(signal)}}^2 + {t_{r(probe)}}^2}$$

For reasonable accuracy, $t_{r(probe)} \approx 5 * t_{r(signal)}$

PE29100
High-speed FET Driver

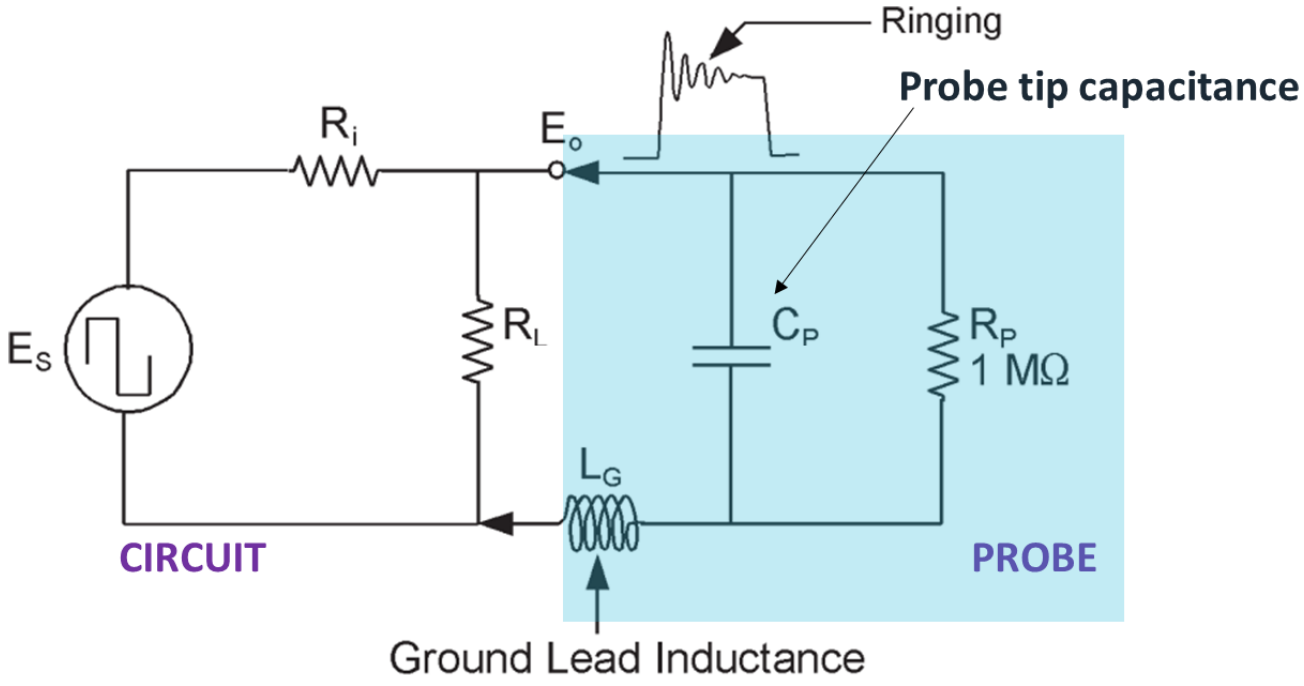
Peregrine Semiconductor

Table 3 • *DC Characteristics (Cont.)*

| Parameter | Condition | Typ | Unit |
|---|---|---|---|
| Dead-time control voltages | 30k to 80 kΩ resistor to GND | 1.2 | V |
| Dead-time from HSG going low to LSG going high | RDHL = 30 kΩ | 0.8 | ns |
| | RDHL = 80 kΩ | 3.4 | ns |
| Dead-time from LSG going low to HSG going high | RDLH = 30 kΩ | 0.8 | ns |
| | RDLH = 80 kΩ | 3.2 | ns |
| **Switching Characteristics** | | | |
| LSG turn-off propagation delay | At min dead time | 8.4 | ns |
| HSG rise time | 10%–90% | 1.0 | ns |
| | 10%–90% with 1000 pF load | 2.5 | |
| LSG rise time | 10%–90% | 1.0 | ns |
| | 10%–90% with 1000 pF load | 1.8 | |
| HSG fall time | 10%–90% | 0.9 | ns |
| | 10%–90% with 1000 pF load | 2.5 | |
| LSG fall time | 10%–90% | 0.9 | ns |
| | 10%–90% with 1000 pF load | 1.8 | |
| Max switching frequency @ 50% duty cycle | RDHL = RDLH = 80 kΩ | 33 | MHz |

# The importance of probing

## PARASITIC CAPACITANCE




- **Decrease amplitude**
- **Change phase**
- **Slow down rise time**
  tr=2.2*Rsource*Cp

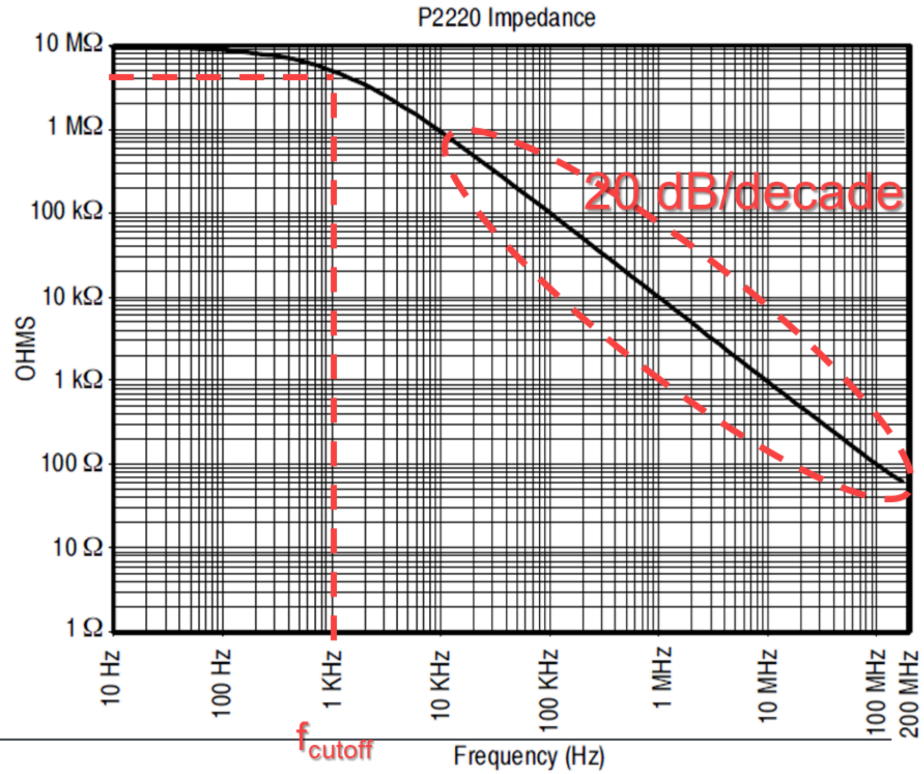
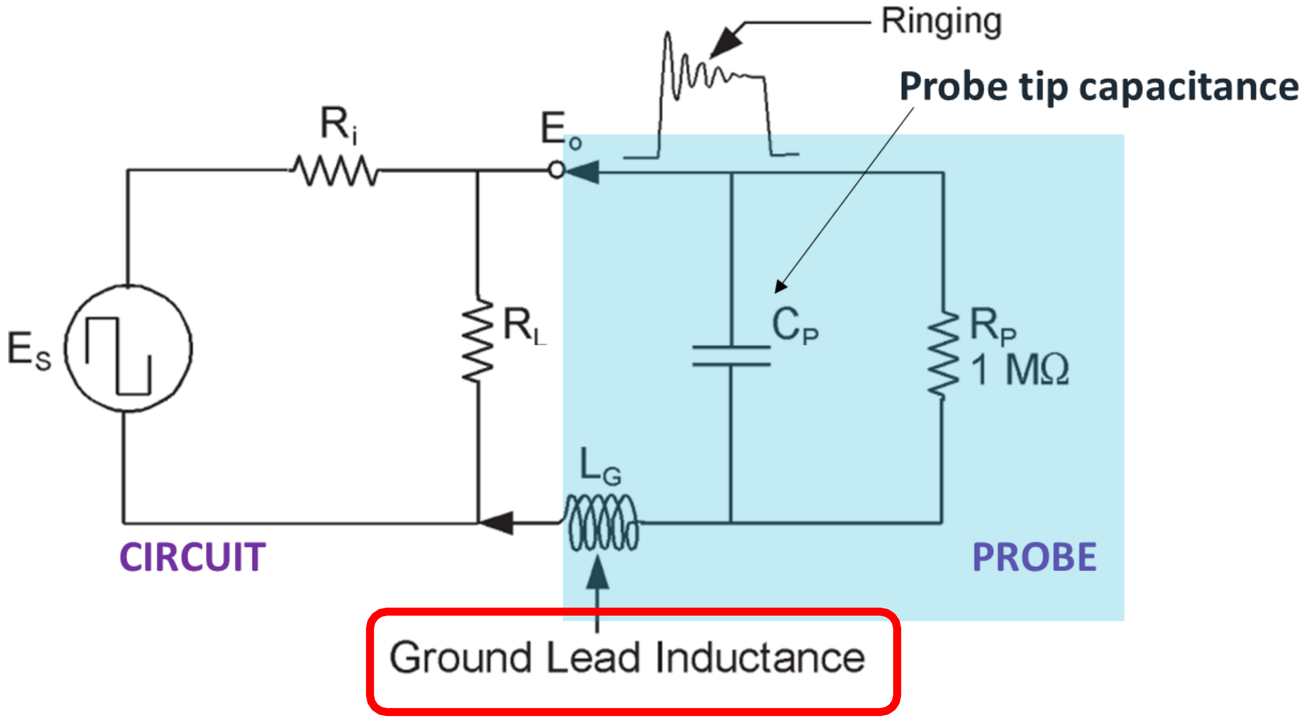


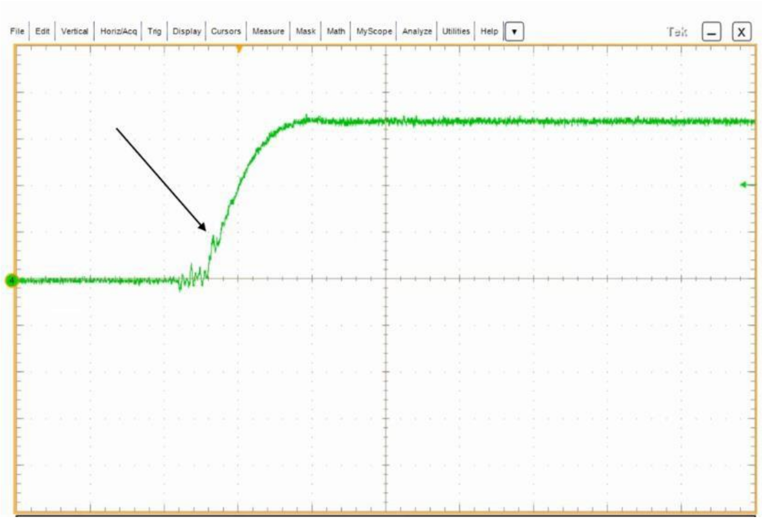

Figure 3: P2220 Input impedance

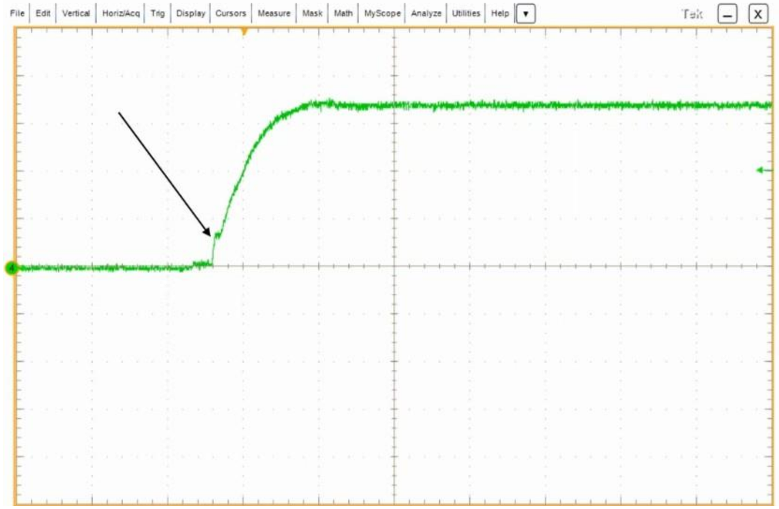
# The importance of probing

## GROUND LEAD INDUCTANCE

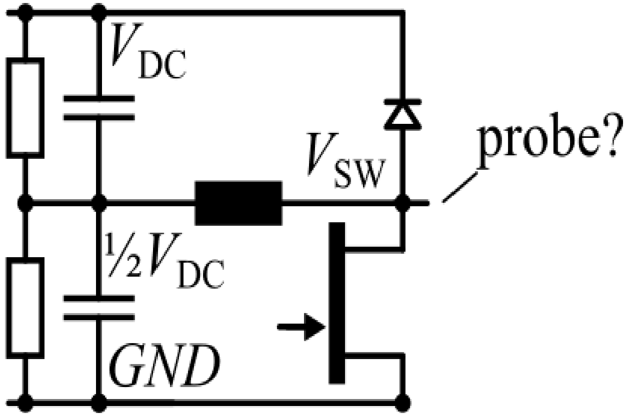



**Inductance +tip capacitance resonate =ringing**

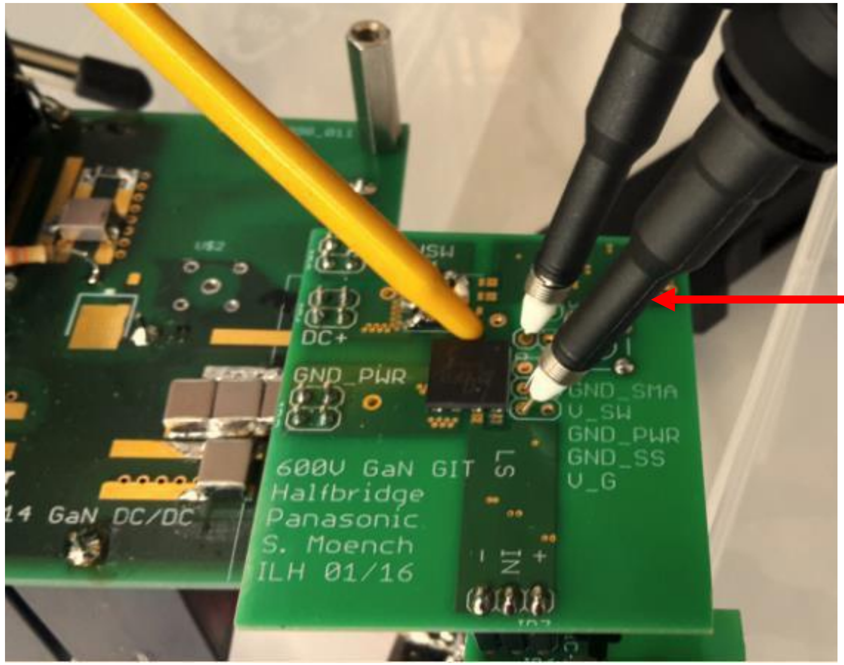




# The importance of probing ( low side )




Low Side Vds requires high bandwidth and high voltage capabilities

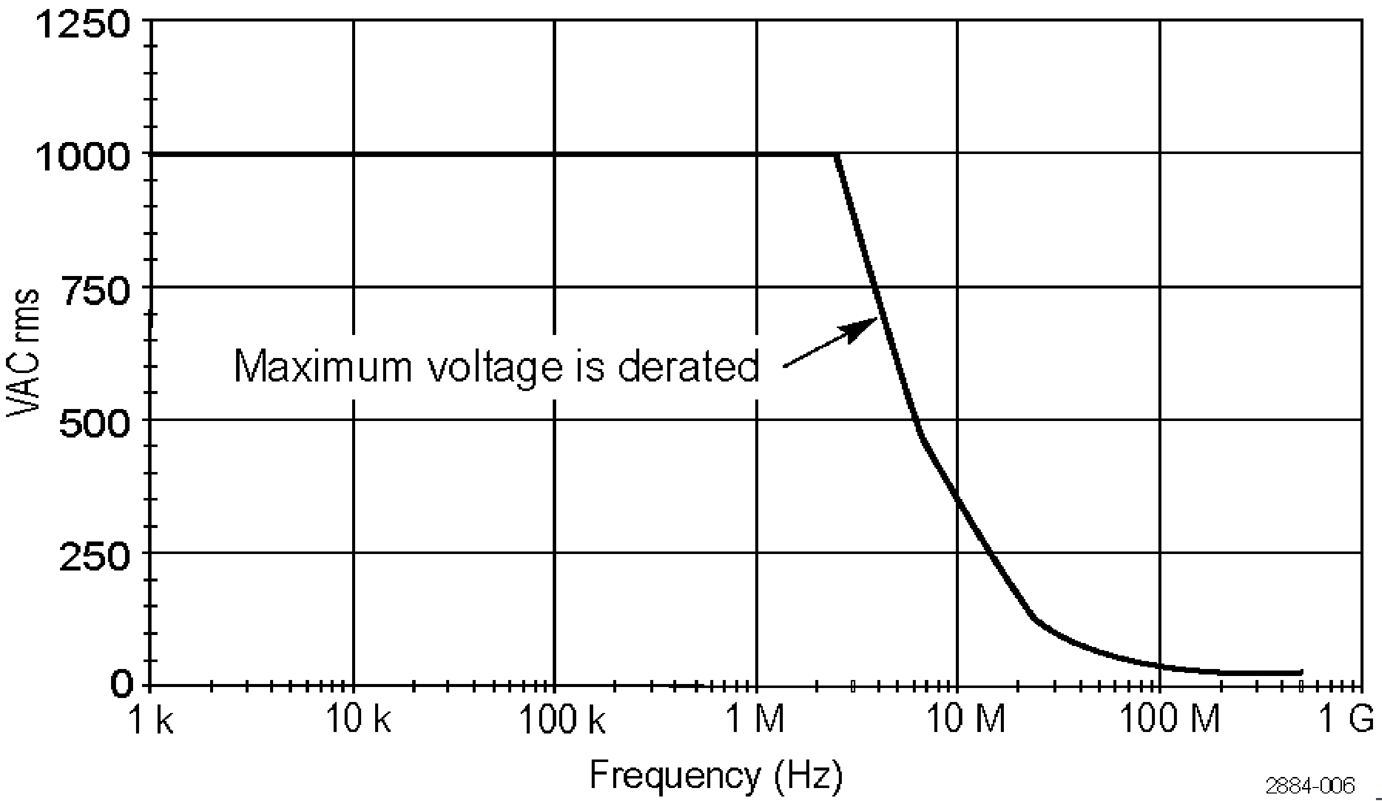



University of Stuttgart, Germany

# The importance of probing

LOW SIDE MEASUREMENTS CONSIDERATIONS

**Beware of voltage derating vs frequency!**



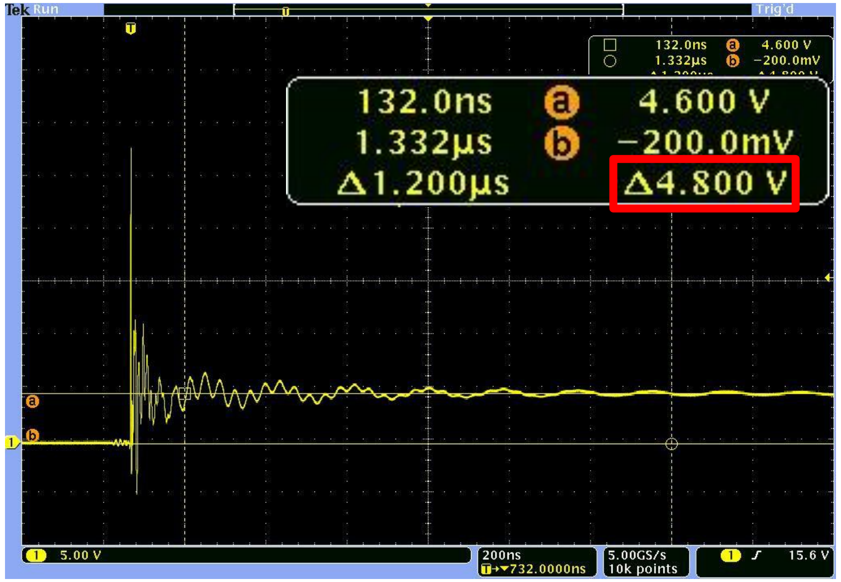
# The importance of probing ( High Side )

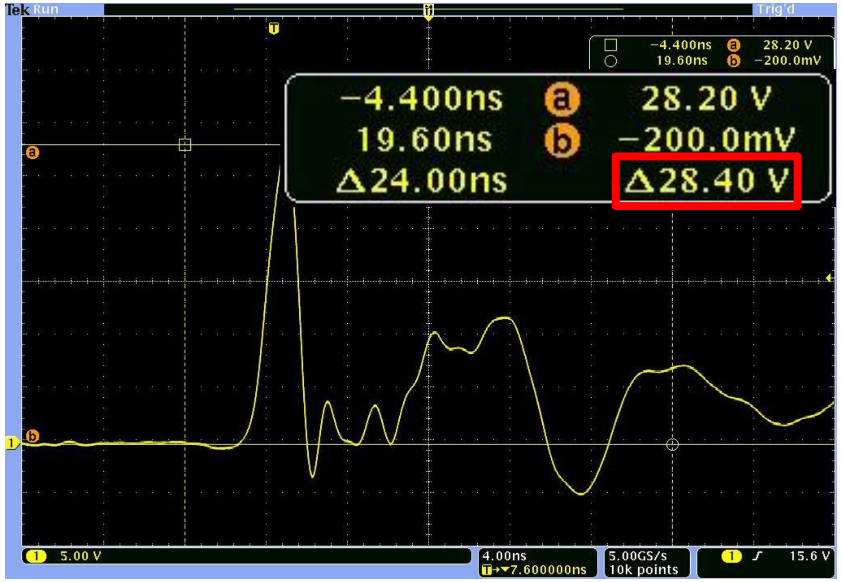
## Differential probes are the preferred choice

- Safety
- Reduce ground loop
- Common mode noise subtracted out of signal (CMRR)
- Smaller input cap

# The importance of probing

## Differential probes are expensive: Why not float the oscilloscope and use passive probes?




High side gate measurement comparison

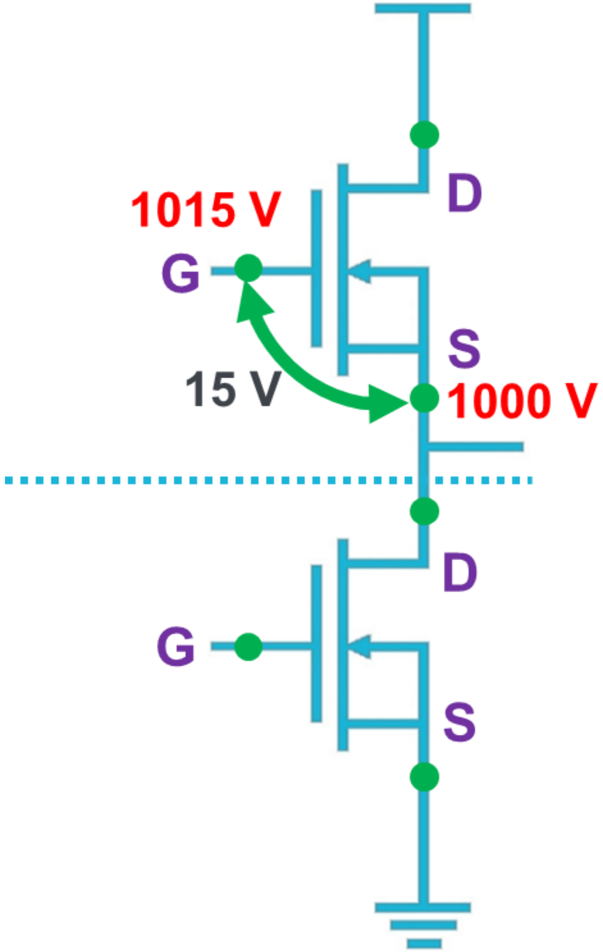
**Bad signal fidelity (capacitive coupling) and unsafe**

# The importance of probing

## HIGH SIDE MEASUREMENTS CONSIDERATION

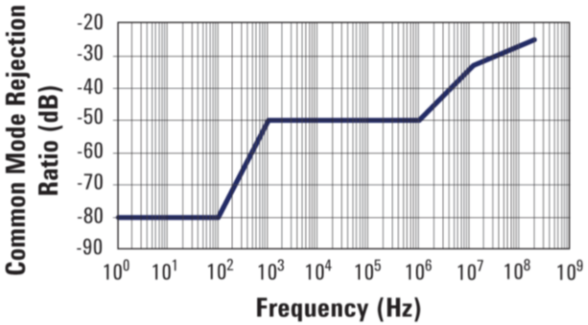
**But high voltage differential probes have downsides**

- High attenuation degrades signal to noise (High Side Vg)
- Radiated noise couples to the measurements through the leads
- Voltage derating vs frequency also applies
- **CMRR is insufficient**



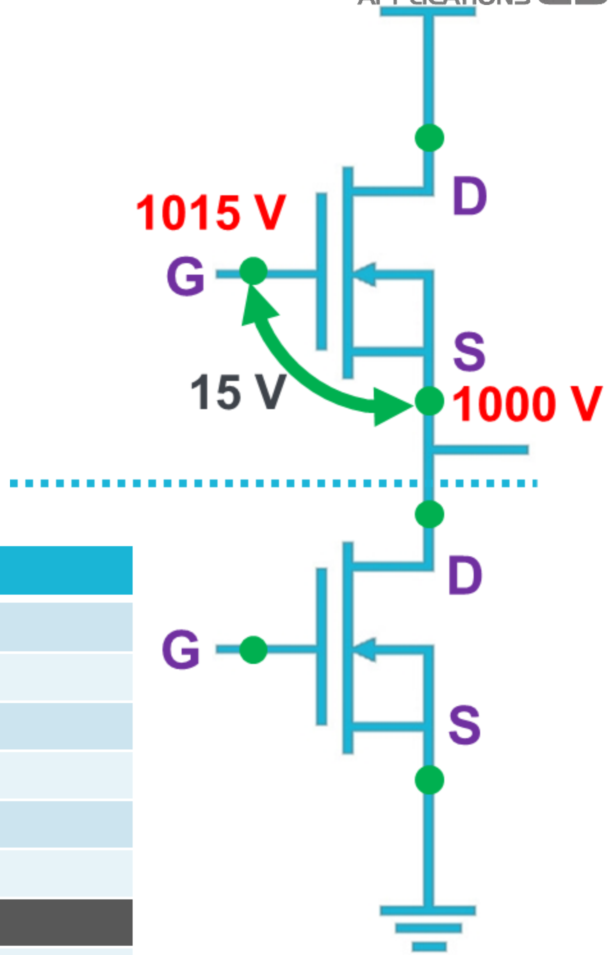
# The importance of probing

## CMRR




← Exemple of CMRR derating curve

**CM error at 100MHz: 1000V/22 =45V**

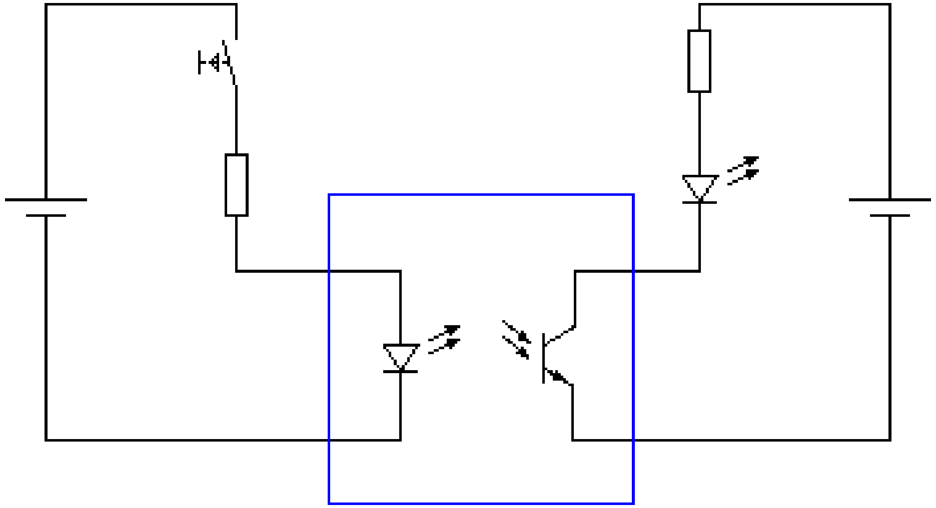



| | High Voltage Differential |
|---|---|
| | X probe |
| Bandwidth | 200 MHz |
| CMRR DC | >80 dB (10,000:1) |
| CMRR 1 MHz | 50 dB (316:1) |
| CMRR 100 MHz | 27 dB (22:1) |
| CMRR Full Bandwidth | 15 dB (5.6:1) |
| | |
| Common Mode Error (1kV) @ DC | 0.1 V |
| Common Mode Error (1kV) @1 MHz | 3.2 V |
| Common Mode Error (1kV) @100 MHz | 45.2 V |
| Common Mode Error (1kV) @ Full BW | 178.6 V |

# The importance of probing

## INTRODUCTION TO ISOLATED PROBES

An isolated probe uses galvanic (optical) isolation to divorce the reference voltage of the probe from the reference voltage of the oscilloscope

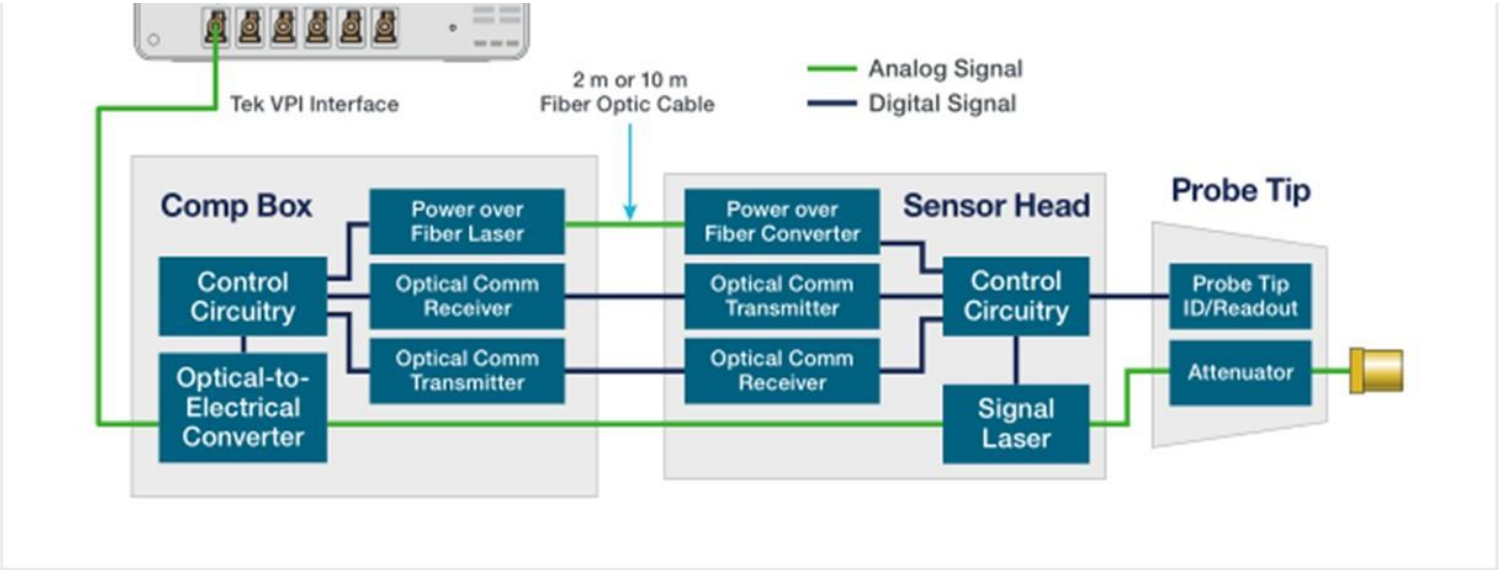


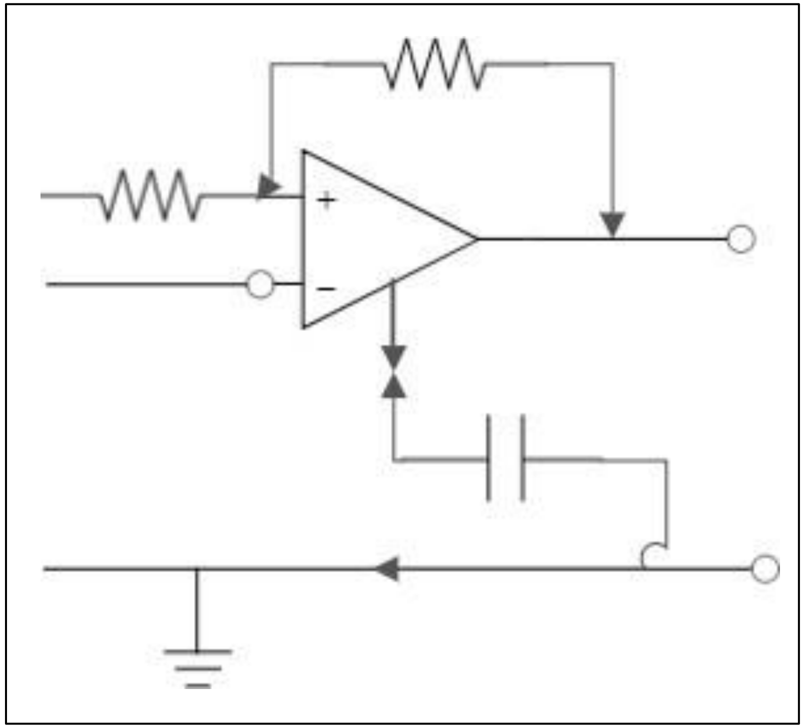
Advantages:

| | Isolated Probe |
|---|---|
| EMI Susceptibility | Shielded Coaxial cable with common mode chokes; less coupling, less ringing |
| Cable Length | 2m fiber optic cable, 10m cable option |
| Safety | Complete galvanic isolation allows scope to sit outside PVC chamber |
| Ground Loops | Eliminates ground loops |
| Loading | No input +to ground loading |

# The importance of probing

## INTRODUCTION TO ISOLATED PROBES: NOTE ON ARCHITECTURE



# The importance of probing

## INTRODUCTION TO ISOLATED/Optical PROBES

Planned test points (MMCX Connectors) ➔ Best Performance

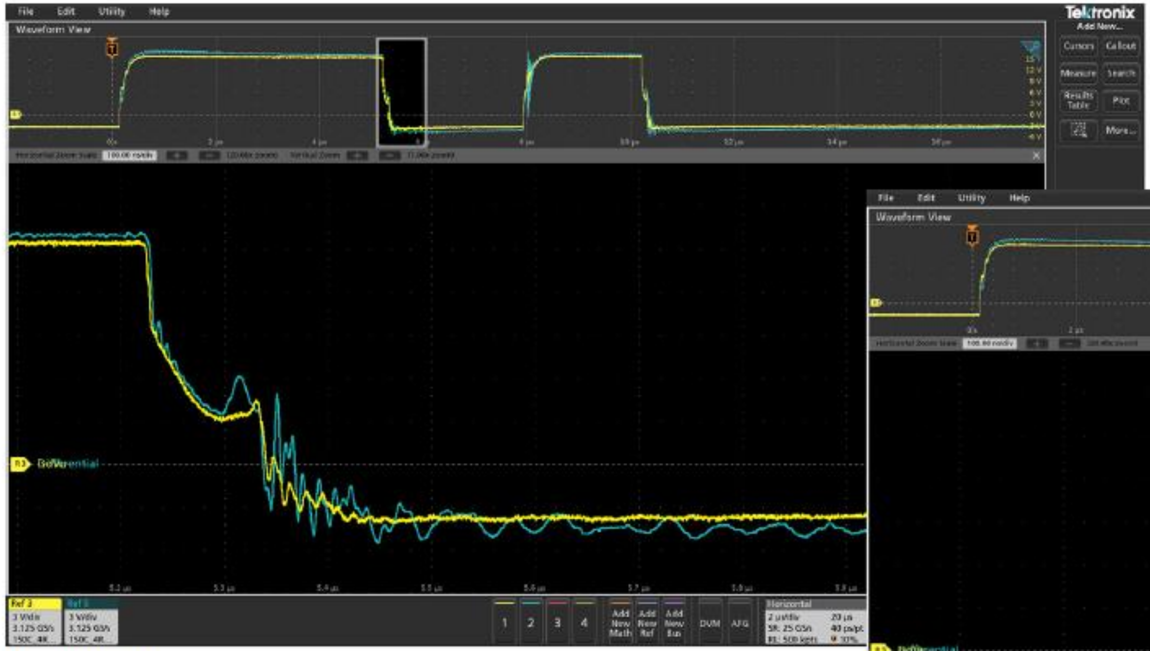
MMCX connectors are small, **shielded** ,inexpensive . They can be soldered onto unplanned test points.

Figure 3. CIL Evaluation kit for FM3 Module

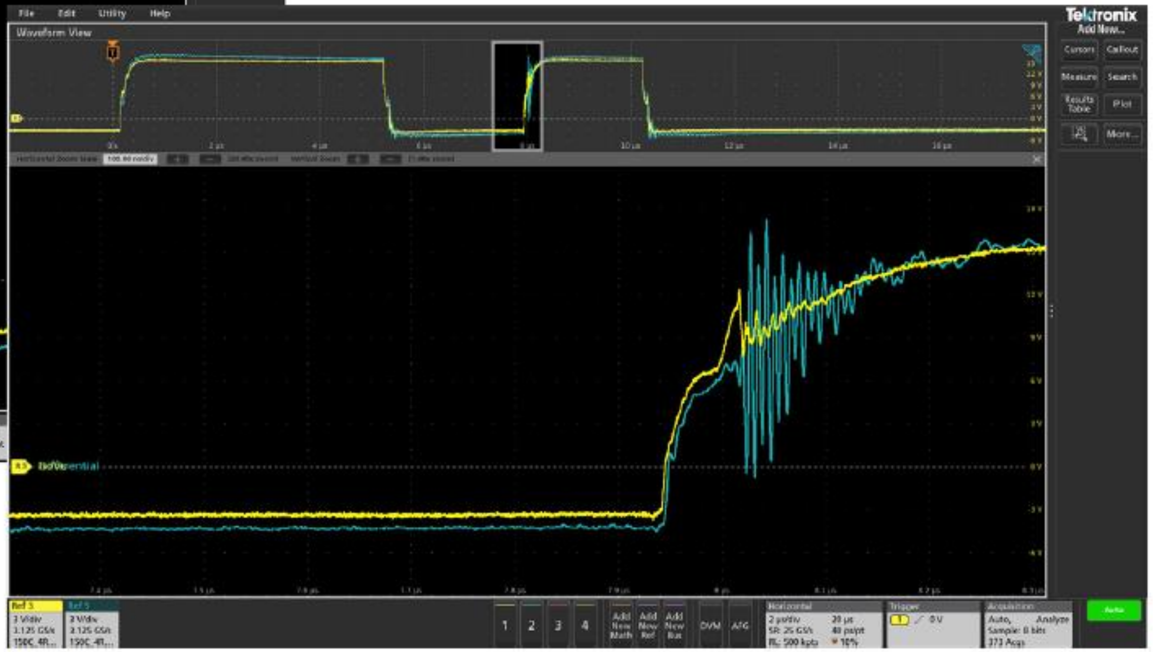
# The importance of probing

## INTRODUCTION TO ISOLATED PROBES

High Side Vgs example-Differential Probe (blue trace) vs. Optically Isolated Probe (yellow trace).



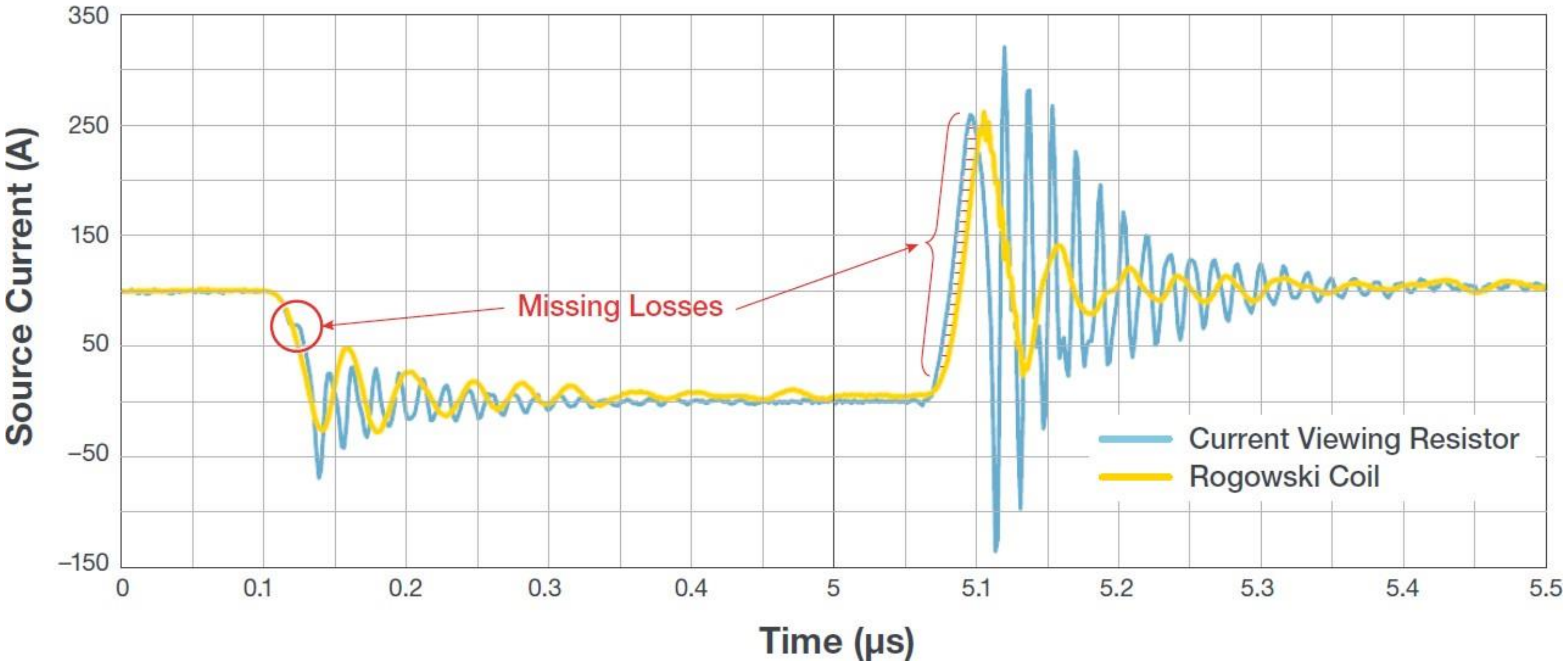
$V_{GS}$ Turn-off



$V_{GS}$ Turn-on

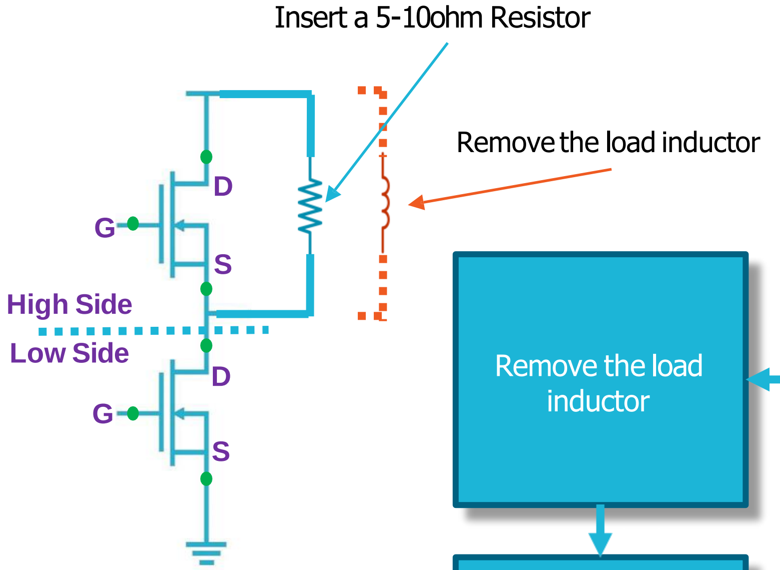
# The importance of probing

## CURRENT MEASUREMENTS




CVR vs Rogowski Current Probe, CAB011M12FM3 (TJ = 150°C, RG = 1 Ω), VDS = 600 V, IS = 100 A).

# Conventional Deskew Challenges



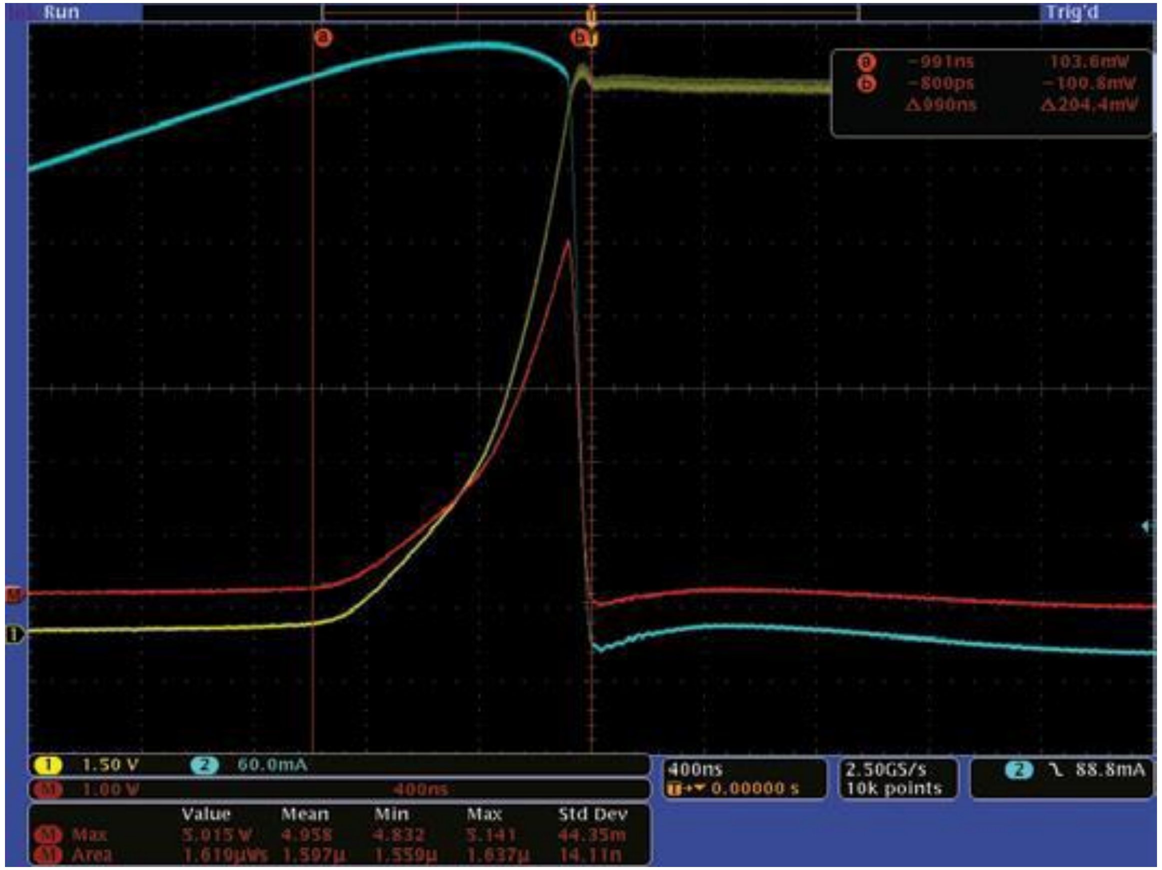

**Power =V x I**

- Critical to have signals time aligned to get accurate results
- Different probes have different delays

## +60 Minutes per deskew cycle

1. Remove the load inductor
2. Connect a low inductance resistor (~10 Ohm) across the device
3. Apply DC bus voltage
4. Measure Vgs, Vds and Ids across lower device
5. Save the waveforms
6. Align the V and I waveforms based on their vertical scales
7. Zoom to the turn on/off regions
8. Manually measure the delay between the waveforms and apply deskew on one of the channel until the two traces are perfectly aligned
9. Remove the resistor and reconnect the load inductor
10. Start testing; Repeat procedure if setup changes

# Deskew

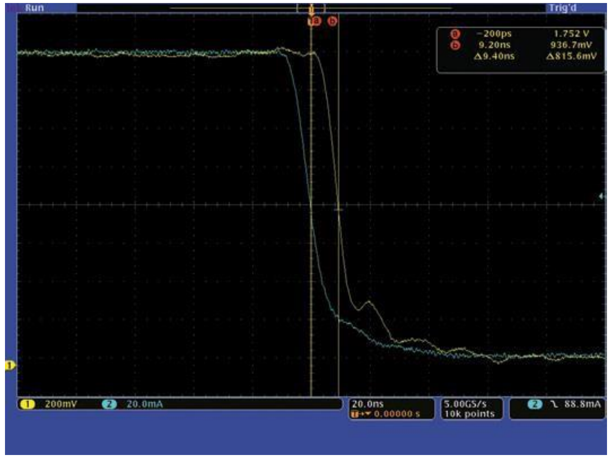



Switching loss **Mean power =4.958 W**

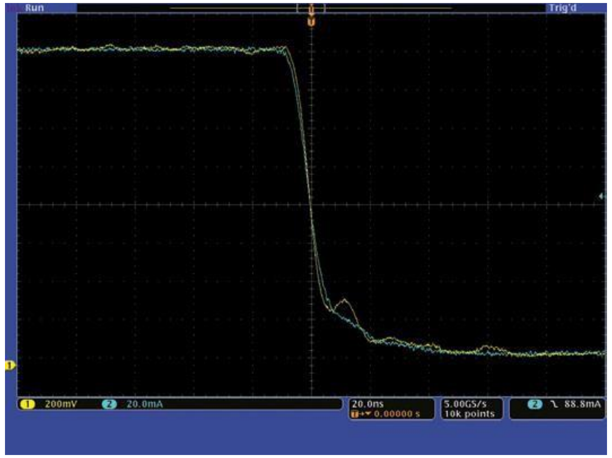
# DESKEW

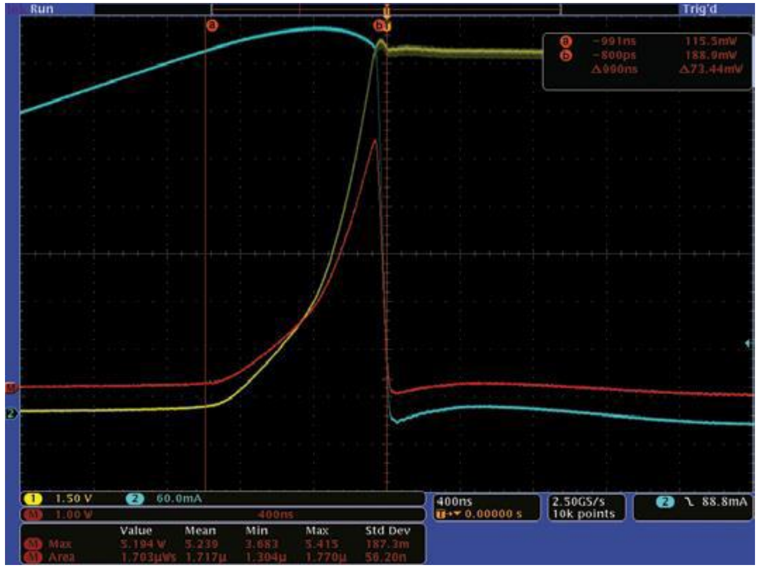
**Mean power =5.239 W**

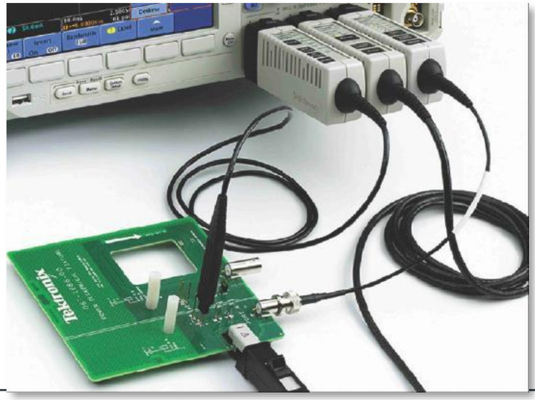
**5.6% error w/o deskew**



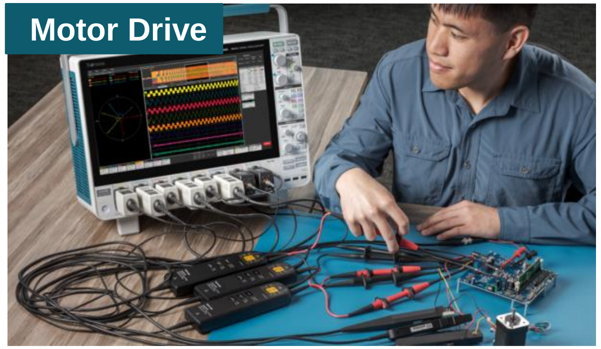

DESKEW

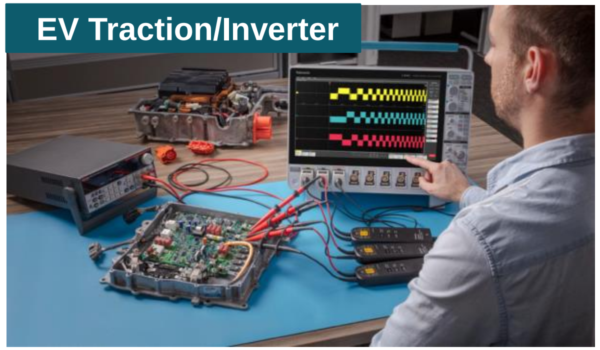


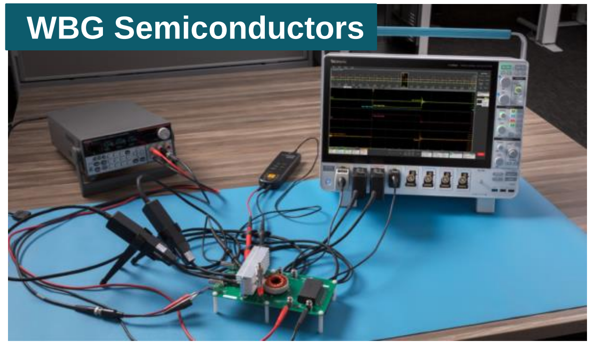



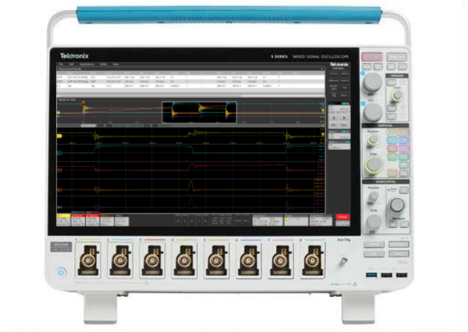
# Complete Wide Bandgap Validation




## SCOPE




5 SERIES B MSO

## PROBES

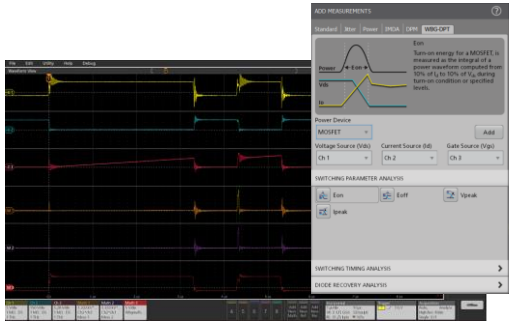
TCPx, TPPx, IsoVu

## DC POWER GATE DRIVE

SMU, AFG

## SOFTWARE

New!



Opt. WBG-DPT

## SERVICES

*Total protection service options to protect your investment over the lifetime of the solution*

## SOFTWARE BUNDLES

# Thank you ..