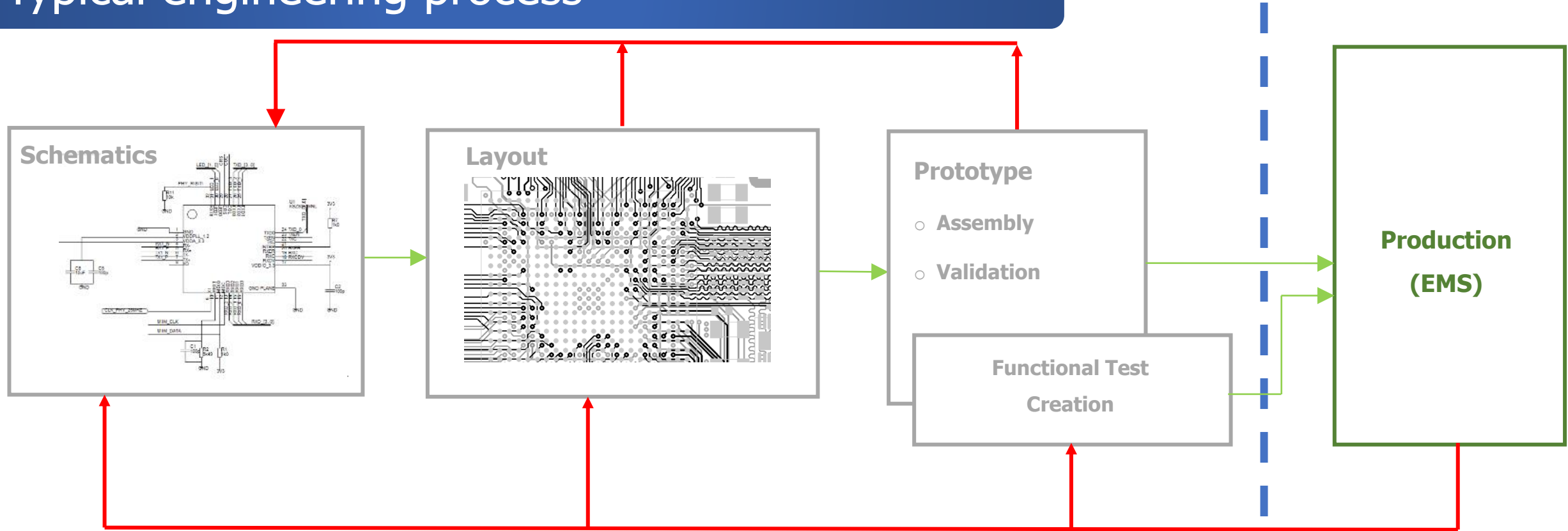


De voordelen van de JTAG interface voor een project met complexere elektronica boarden

- Typical engineering process
- Test methods overview
- JTAG interface Chip level
- Circuits that can be tested well via the JTAG interface
- ISP possibilities via the JTAG interface
- JTAG Test - and ISP applications development process
- Benefits overview

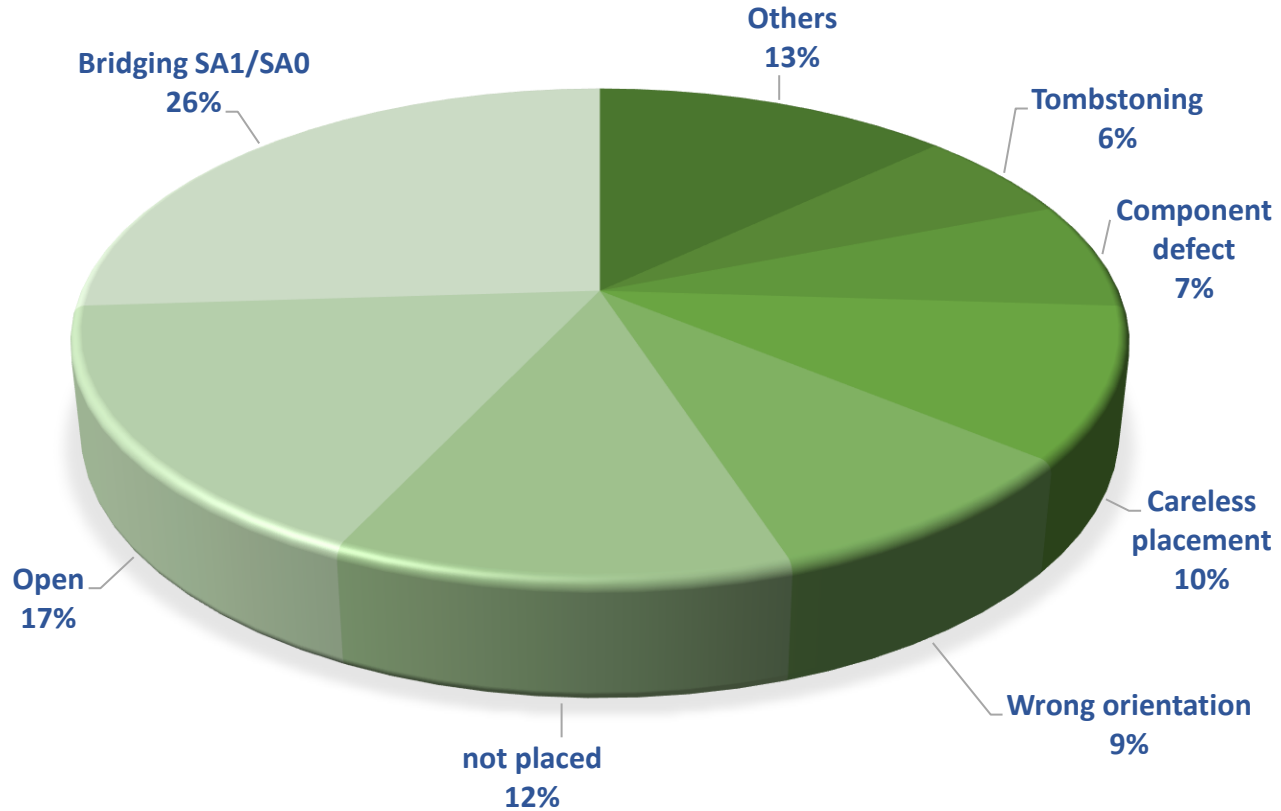
JTAG Technologies
Rik Doorneweert

Typical engineering process



- PCBA's prototypes are delivered untested
- Firmware required to validate HW design
- Test development only starts after layout
- Design change requests for test improvements have (too) much impact

Typical fault spectrum



Find the failures before
your customers do !!!

Various test methods used in production

X-RAY

Rontgen



ICT

In Circuit Test



FP

Flying Probe



FCT

Functional Test



AOI

Automatic Optical
Inspection



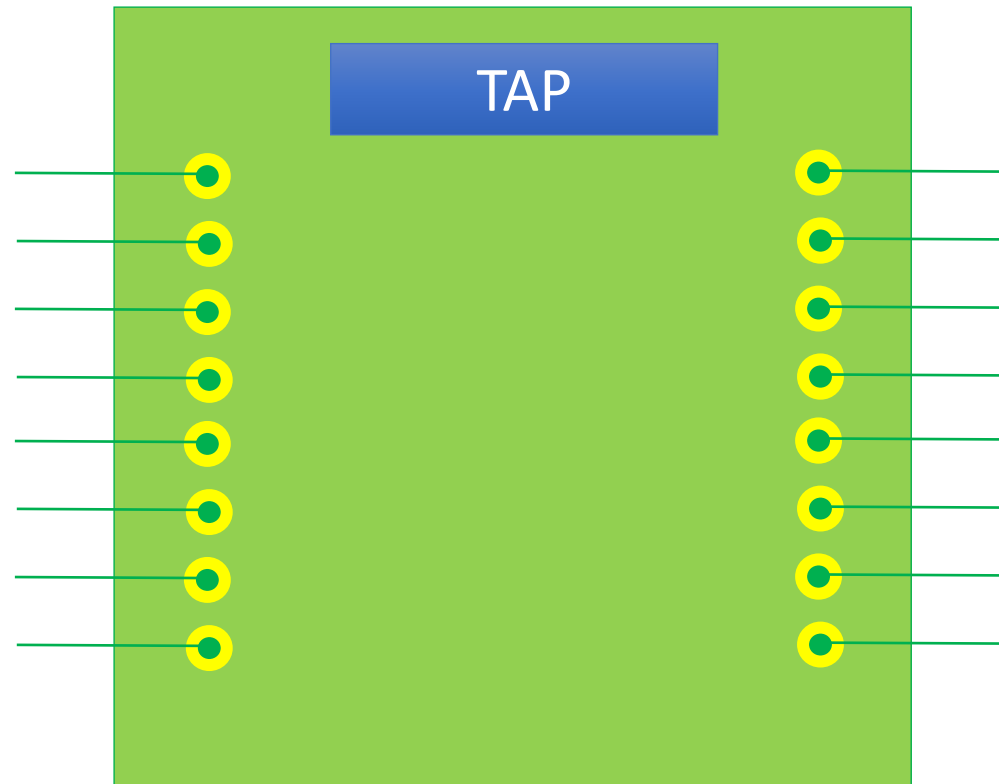
JTAG

Solutions



Basics – Chip Level

◆ Test Access Port (TAP)

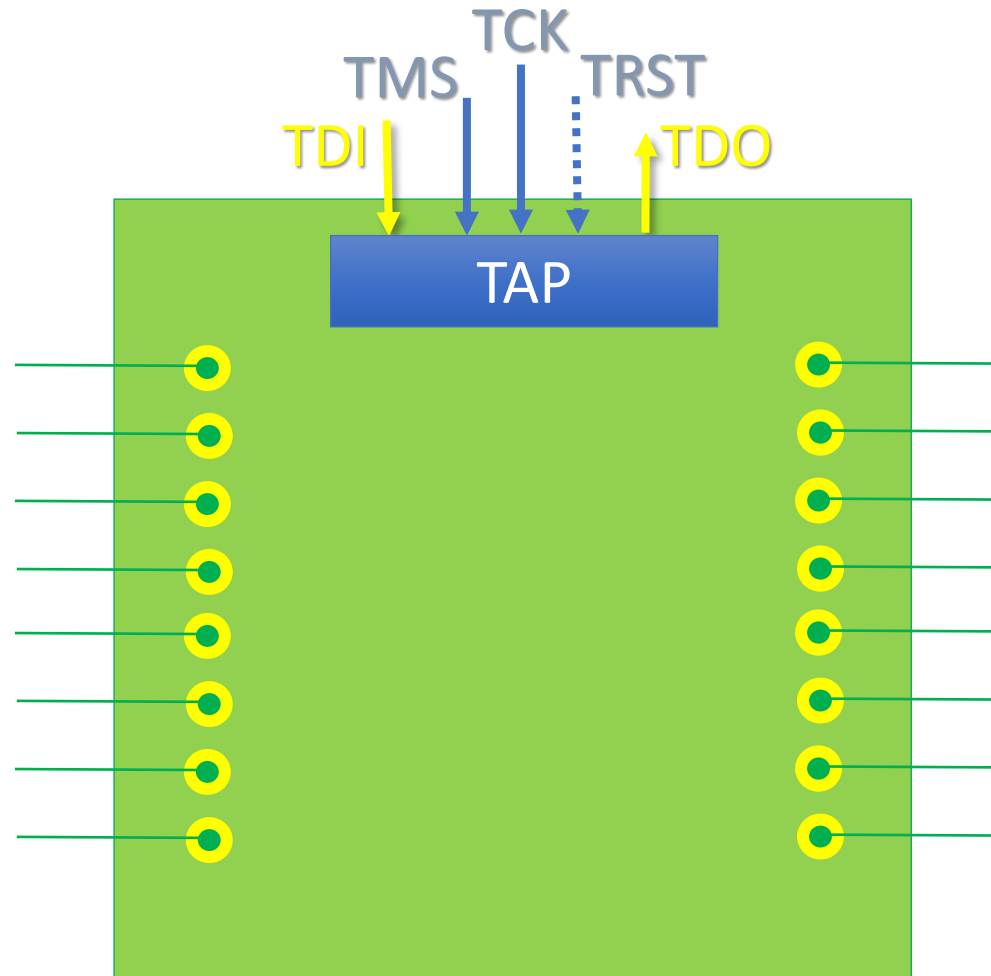


Basics – Chip Level

◆ Test Access Port (TAP)

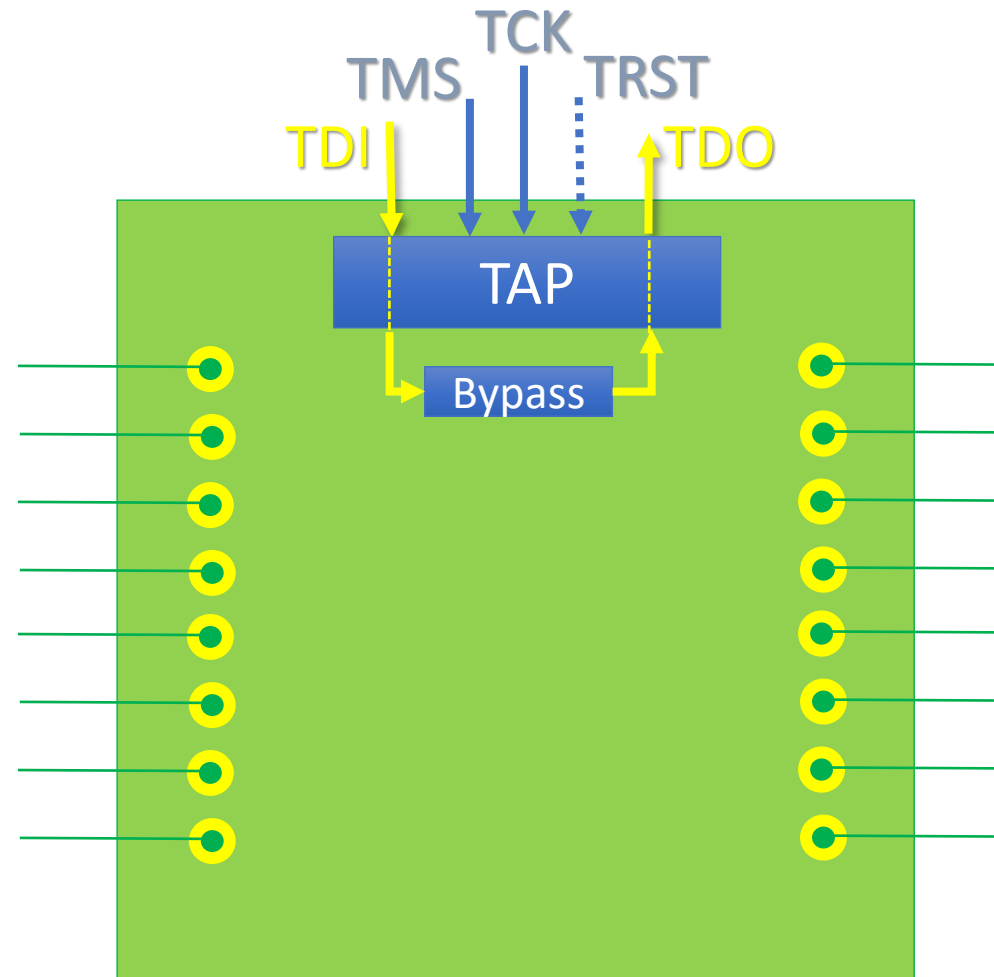
◆ TAP Signals:

- ◆ Test Data Input
- ◆ Test Data Output
- ◆ Test Mode Signal
- ◆ Test Clock
- ◆ Test Reset



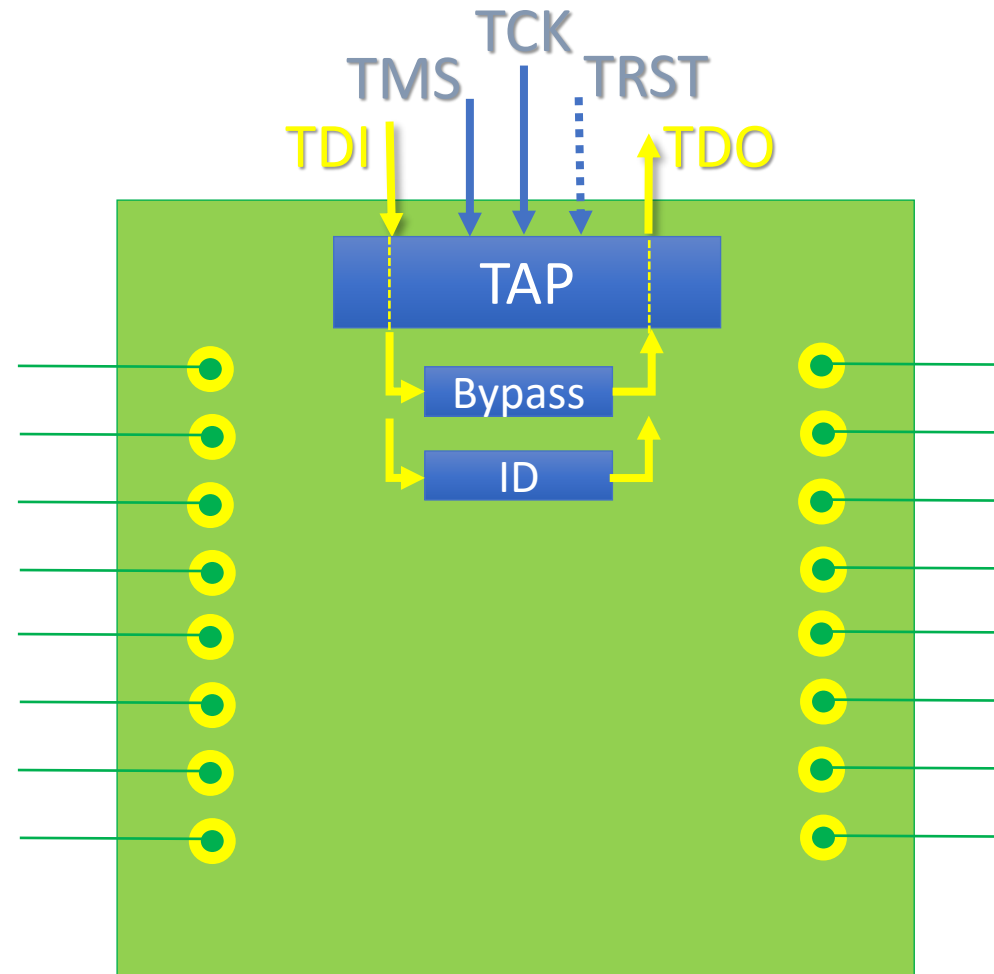
Basics – Chip Level

- ◆ Test Access Port (TAP)
- ◆ TAP Signals:
 - ◆ Test Data Input
 - ◆ Test Data Output
 - ◆ Test Mode Signal
 - ◆ Test Clock
 - ◆ Test Reset
- ◆ Bypass register



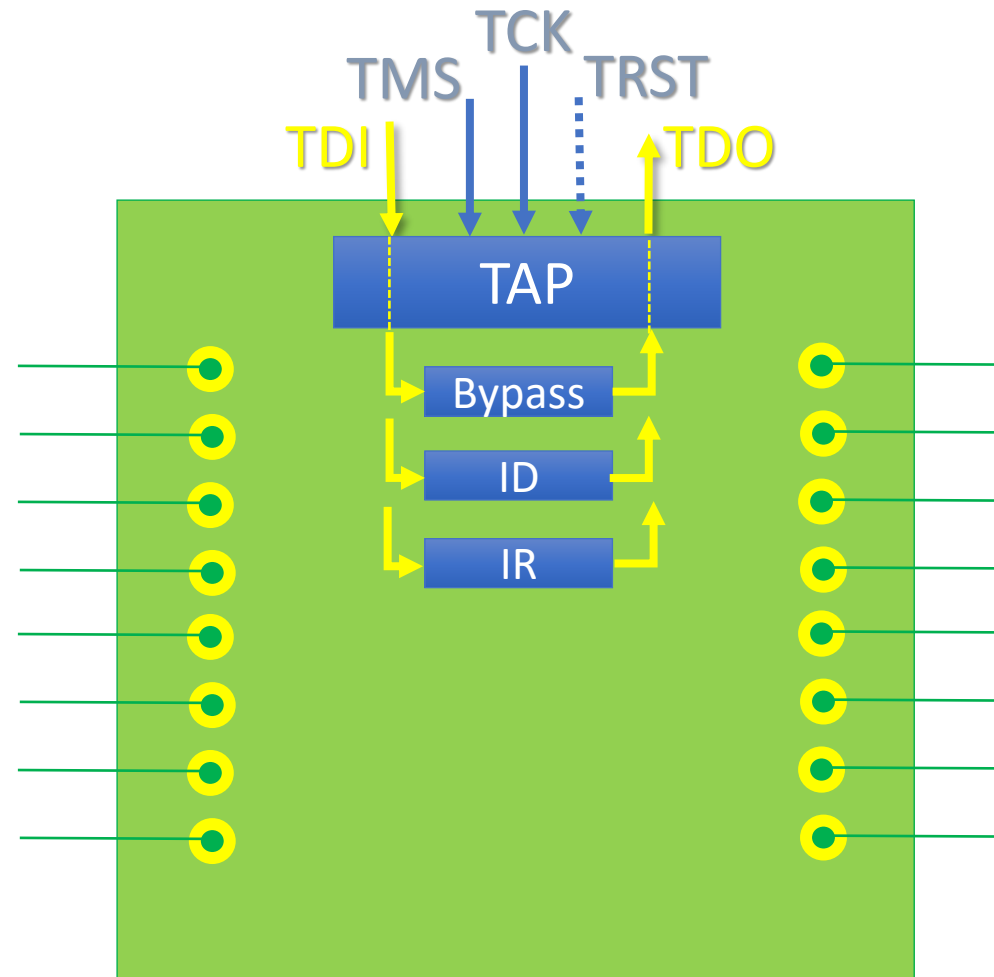
Basics – Chip Level

- ◆ Test Access Port (TAP)
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 - ◆ Test Data Input
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 - ◆ Test Mode Signal
 - ◆ Test Clock
 - ◆ Test Reset
- ◆ Bypass register
- ◆ Identification register



Basics – Chip Level

- ◆ Test Access Port (TAP)
- ◆ TAP Signals:
 - ◆ Test Data Input
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 - ◆ Test Mode Signal
 - ◆ Test Clock
 - ◆ Test Reset
- ◆ Bypass register
- ◆ Identification register
- ◆ Instruction register



Basics – Chip Level

◆ Test Access Port (TAP)

◆ TAP Signals:

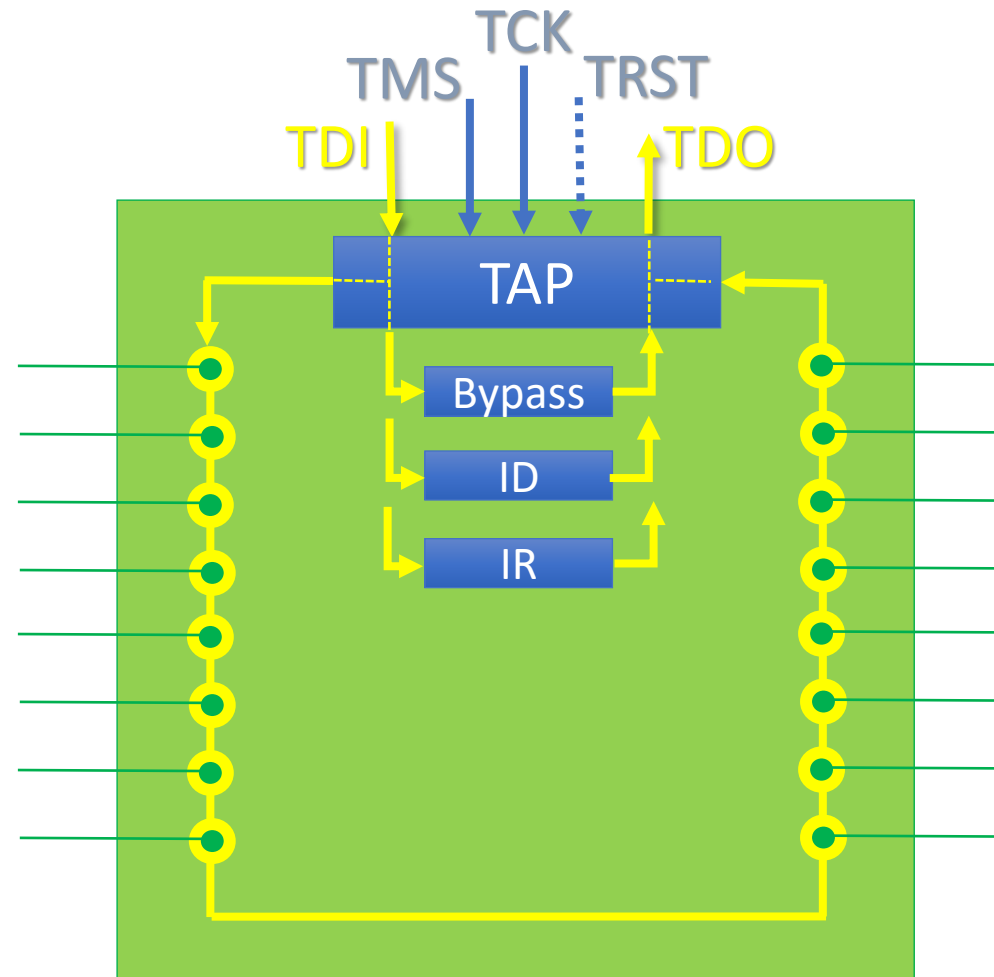
- ◆ Test Data Input
- ◆ Test Data Output
- ◆ Test Mode Signal
- ◆ Test Clock
- ◆ Test Reset

◆ Bypass register

◆ Identification register

◆ Instruction register

◆ Boundary Scan register



Basics – Chip Level

- ◆ Test Access Port (TAP)

- ◆ TAP Signals:

- ◆ Test Data Input
- ◆ Test Data Output
- ◆ Test Mode Signal
- ◆ Test Clock
- ◆ Test Reset

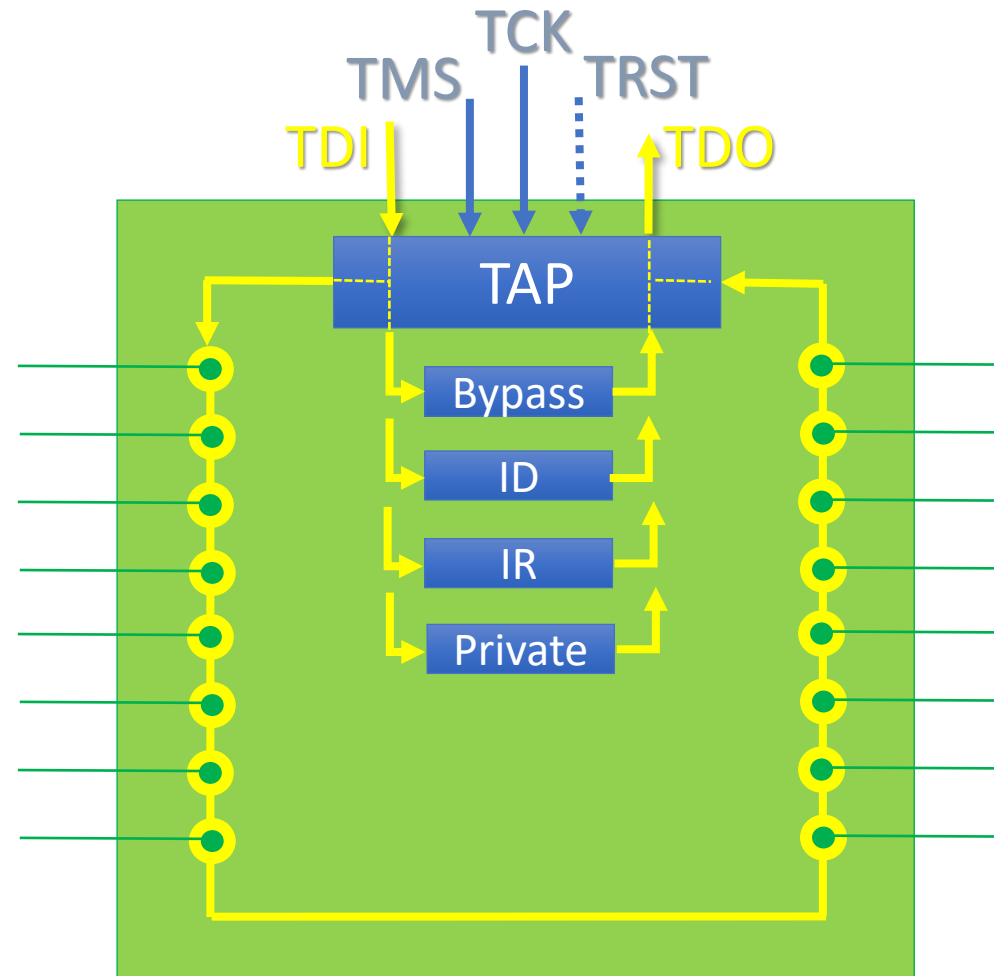
- ◆ Bypass register

- ◆ Identification register

- ◆ Instruction register

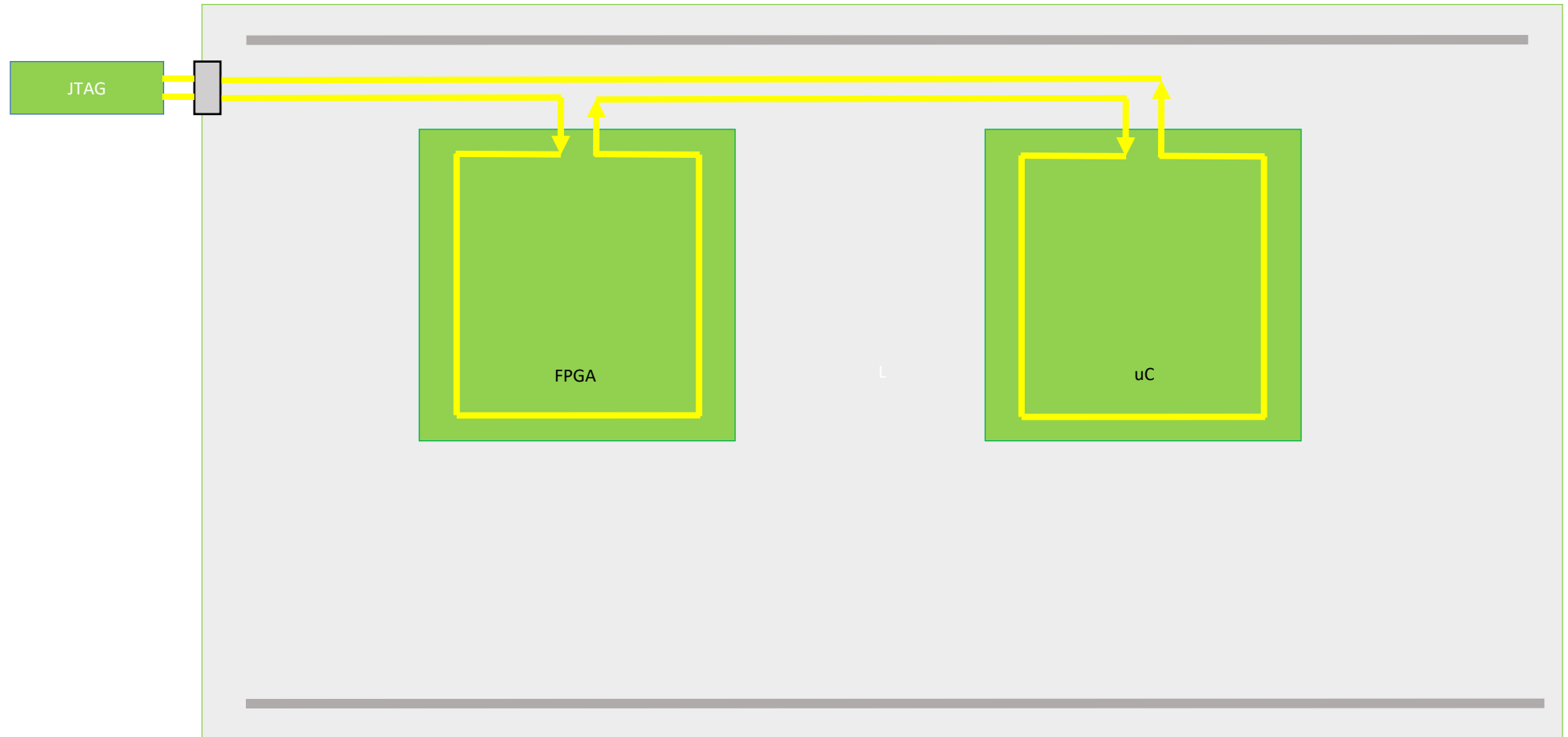
- ◆ Boundary Scan register

- ◆ Private



Basics - Test Applications

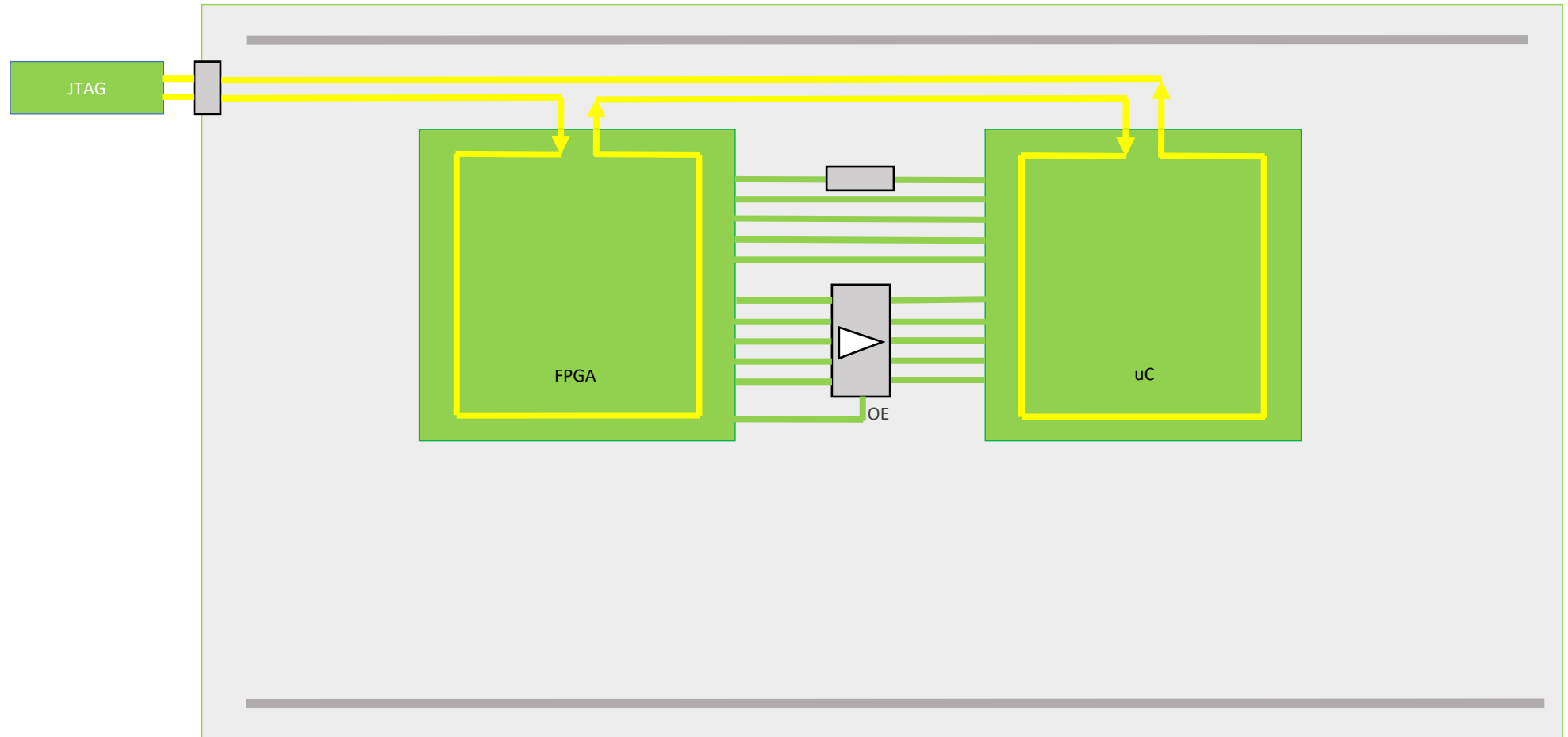
Chain



Capture value | Identification value | TRST connection | Boundary Scan Register length

Basics - Test Applications

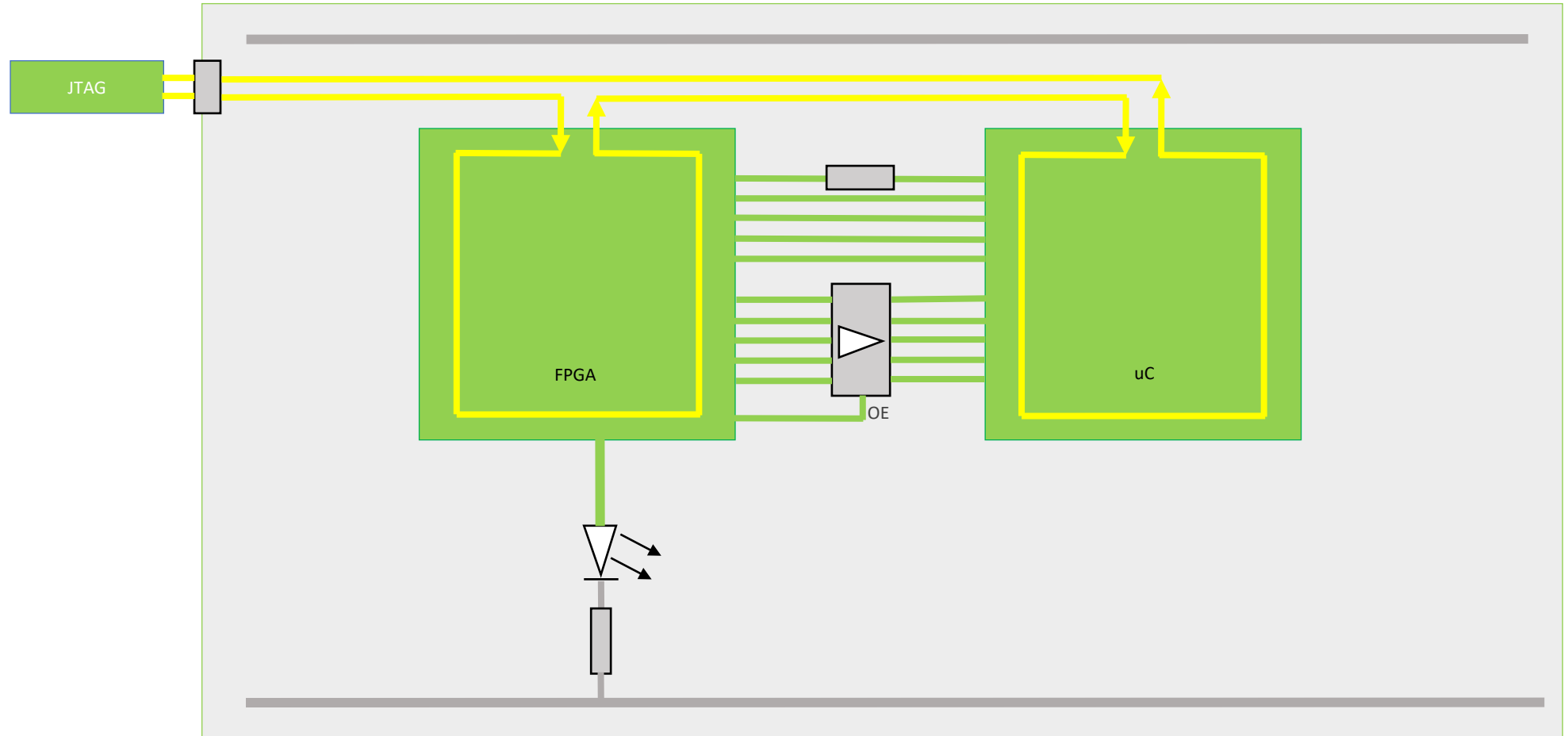
- ◆ Chain
- ◆ Interconnect



Testing on: Opens, Shorts , Stuck at 1 (SA1), Stuck at 0 (SA0)

Basics - Test Applications

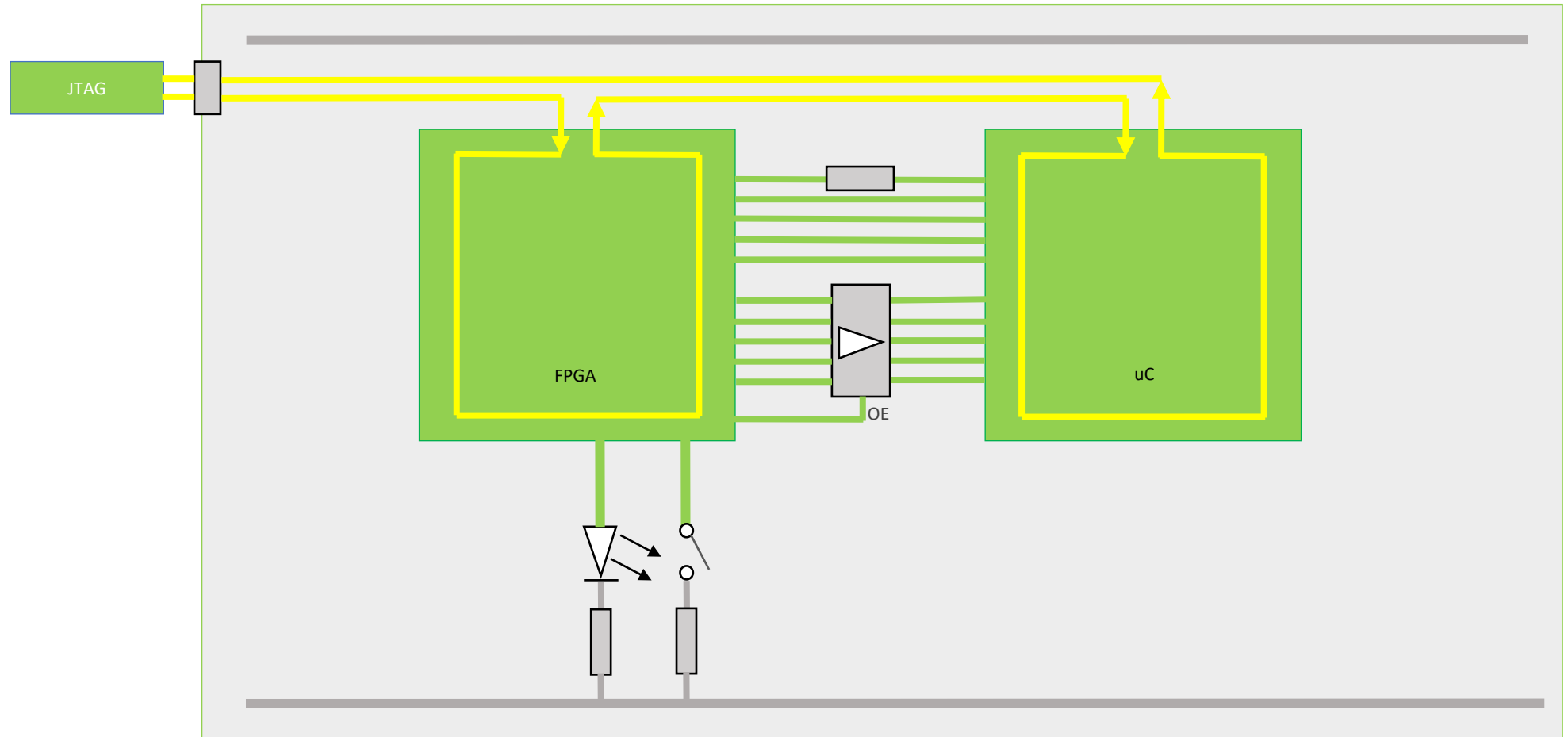
- ◆ Chain
- ◆ Interconnect
- ◆ LEDs



Drive LEDs – observe LEDs manually or by LED analyzer

Basics - Test Applications

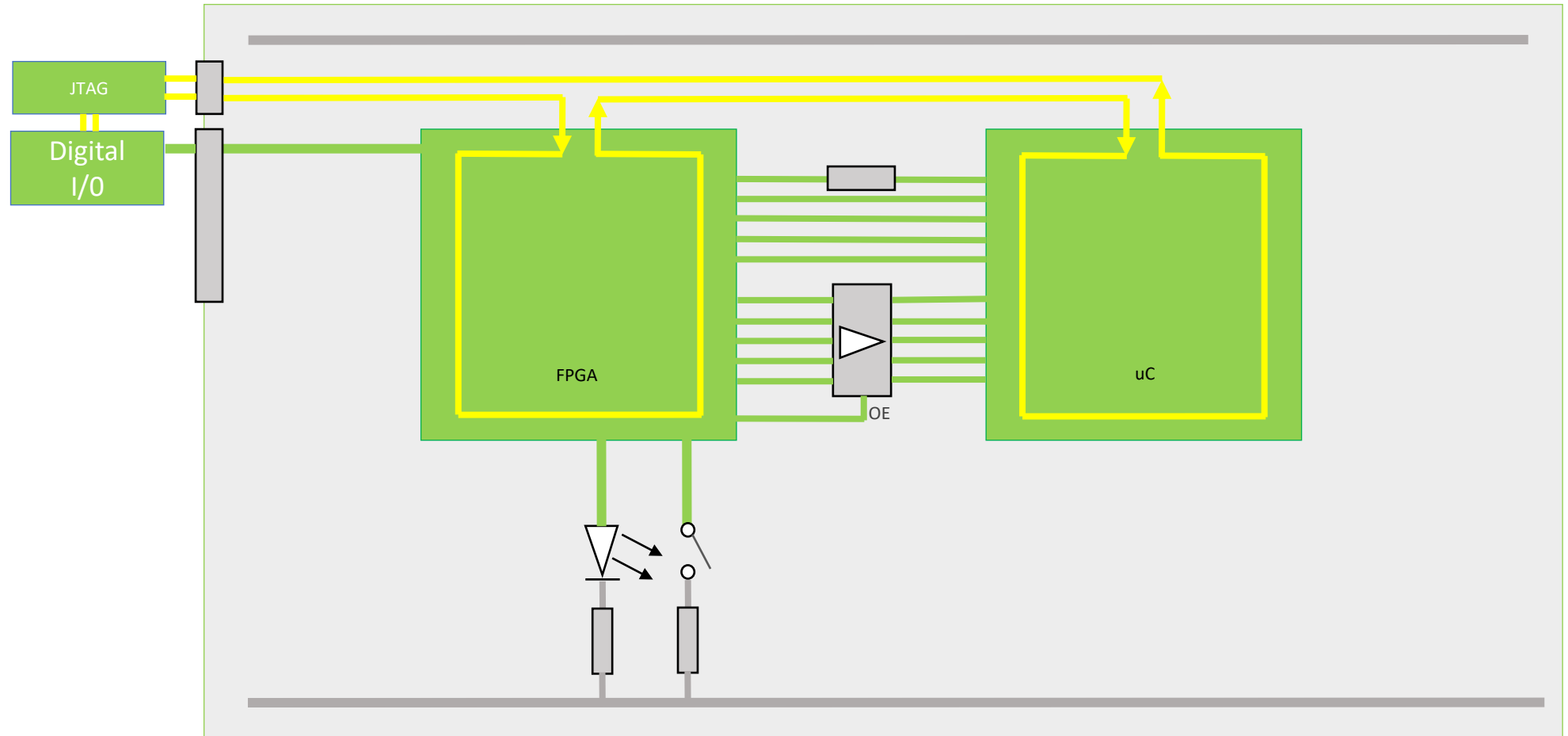
- ◆ Chain
- ◆ Interconnect
- ◆ LEDs
- ◆ Switches



Testing switch positions

Basics - Test Applications

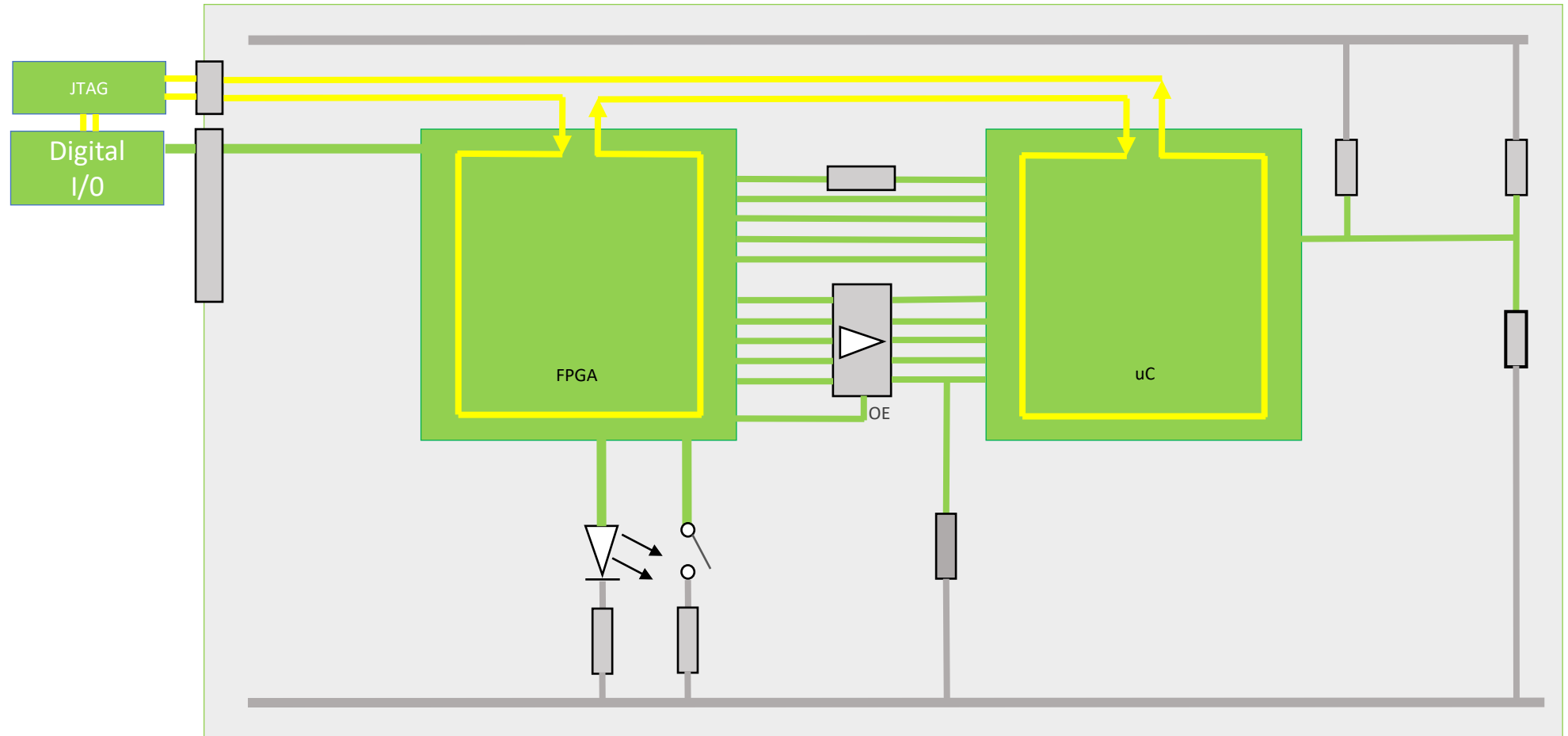
- ◆ Chain
- ◆ Interconnect
- ◆ LEDs
- ◆ Switches
- ◆ Connectors



Testing connections through connectors and via physical test points

Basics - Test Applications

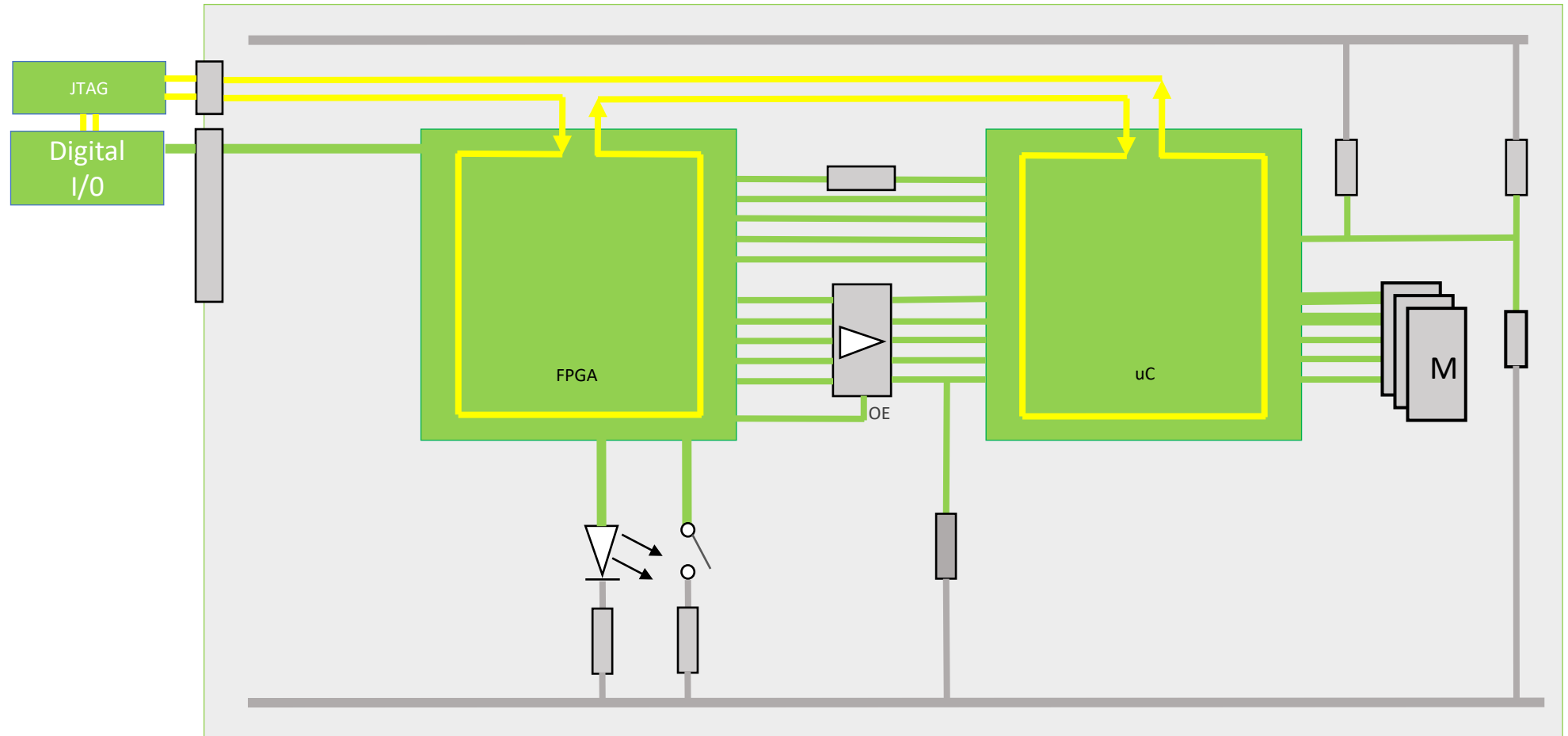
- ◆ Chain
- ◆ Interconnect
- ◆ LEDs
- ◆ Switches
- ◆ Connectors
- ◆ Resistors presence



Check presence of Pull up / Pull down resistors

Basics - Test Applications

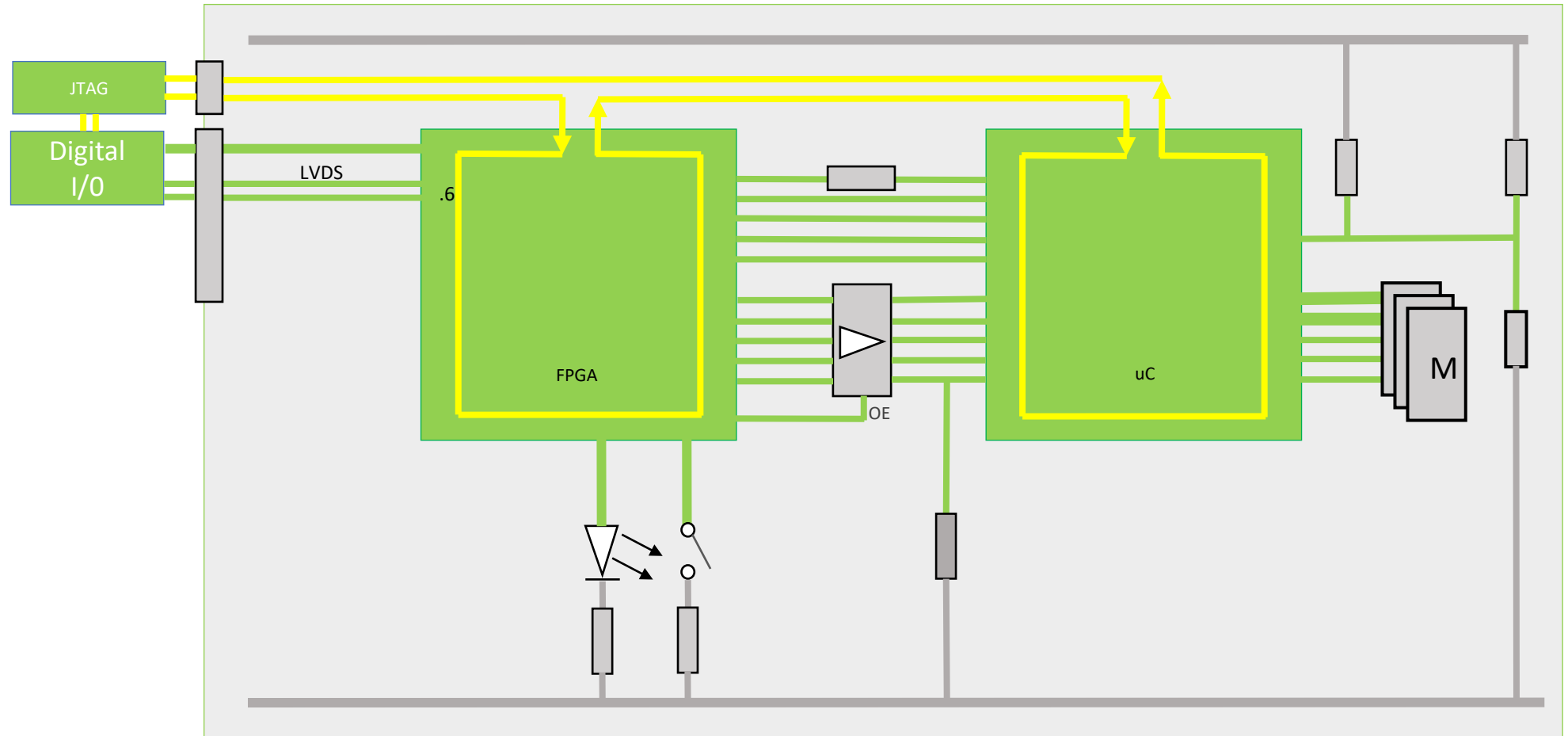
- ◆ Chain
- ◆ Interconnect
- ◆ LEDs
- ◆ Switches
- ◆ Connectors
- ◆ Resistors presence
- ◆ Memory connections



Test address - , data – and control lines of SRAM, DRAM, SDRAM, DDR2/3/4 etc.

Basics - Test Applications

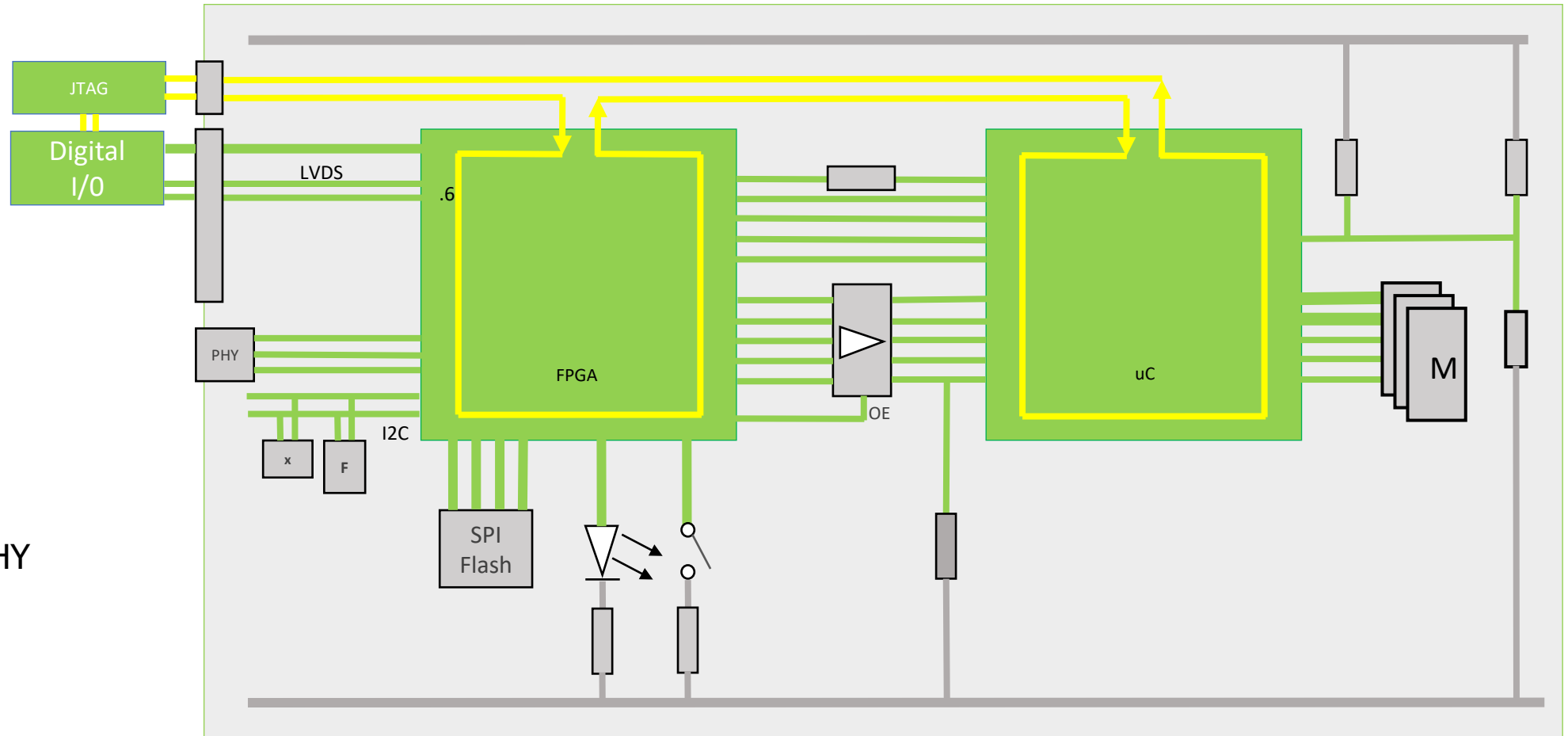
- ◆ Chain
- ◆ Interconnect
- ◆ LEDs
- ◆ Switches
- ◆ Connectors
- ◆ Resistors presence
- ◆ Memory connections
- ◆ LVDS



LVDS connections (IEEE 1149.6)

Basics - Test Applications

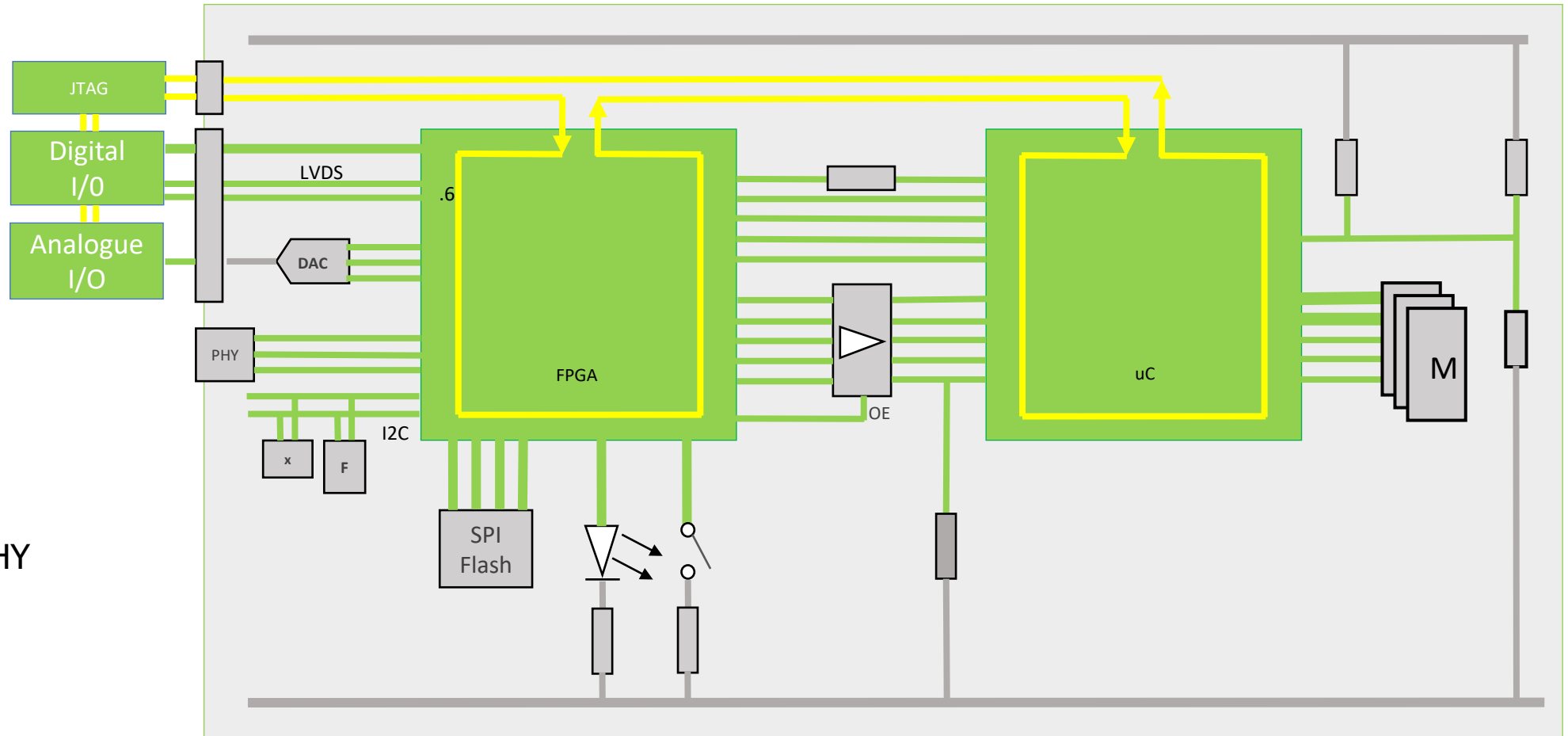
- ◆ Chain
- ◆ Interconnect
- ◆ LEDs
- ◆ Switches
- ◆ Connectors
- ◆ Resistors presence
- ◆ Memory connections
- ◆ LVDS
- ◆ Presence I²C, SPI, PHY



Serial bus tests (I²C, SPI ect.)

Basics - Test Applications

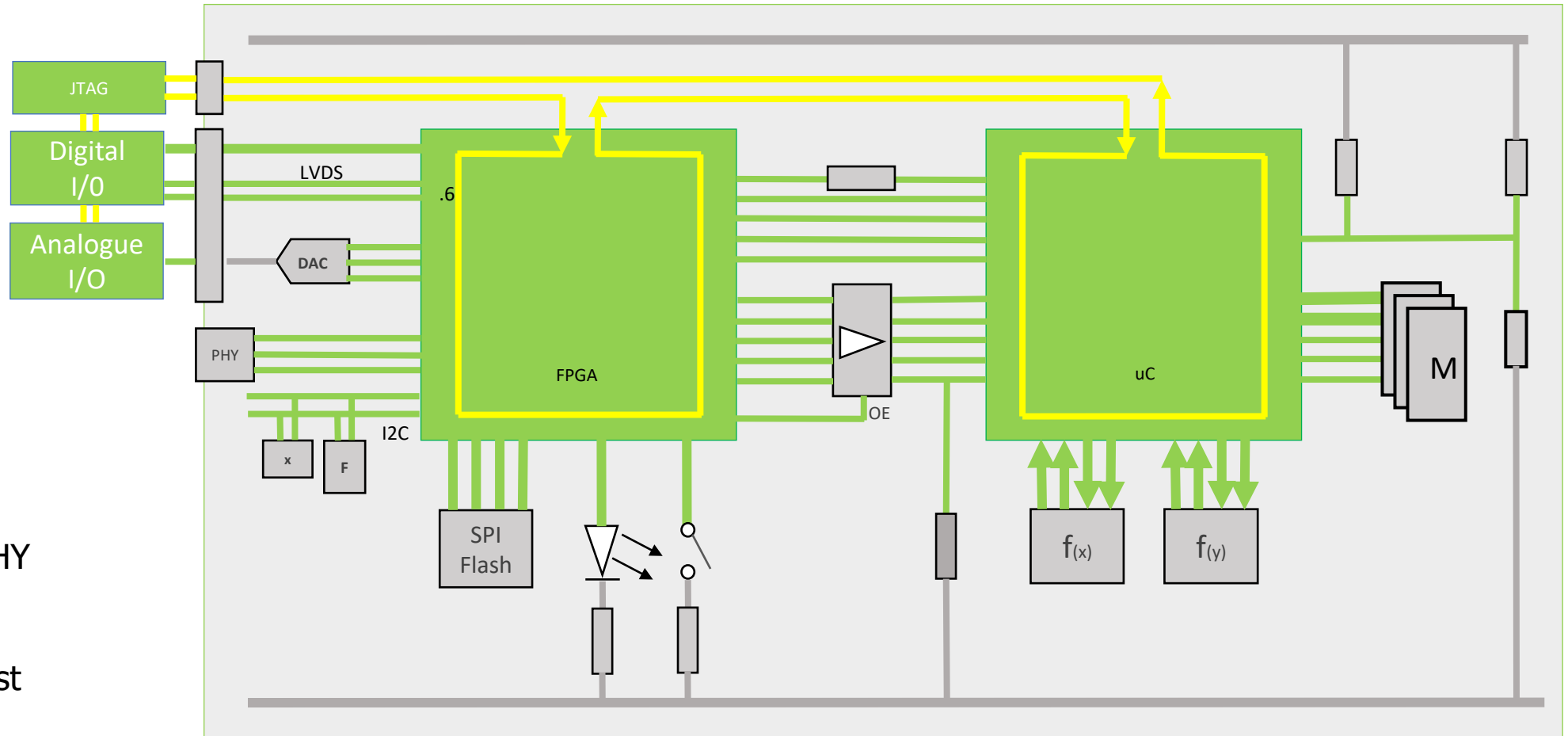
- ◆ Chain
- ◆ Interconnect
- ◆ LEDs
- ◆ Switches
- ◆ Connectors
- ◆ Resistors presence
- ◆ Memory connections
- ◆ LVDS
- ◆ Presence I²C, SPI, PHY
- ◆ Voltage, Freq, PWM



Increase Test coverage with external analogue driving and sense capabilities (ADC/DAC, PWM ect.)

Basics - Test Applications

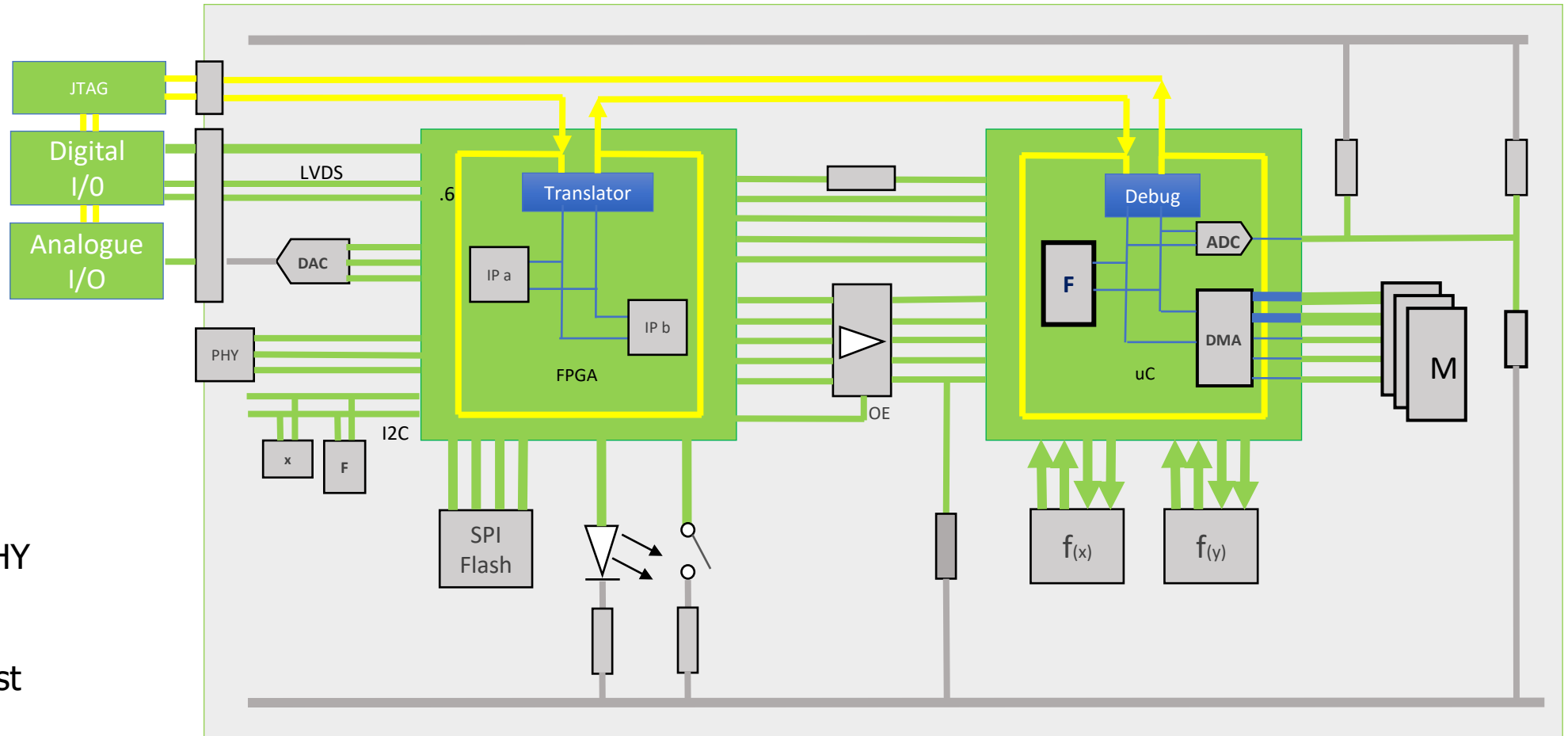
- ◆ Chain
- ◆ Interconnect
- ◆ LEDs
- ◆ Switches
- ◆ Connectors
- ◆ Resistors presence
- ◆ Memory connections
- ◆ LVDS
- ◆ Presence I²C, SPI, PHY
- ◆ Voltage, Freq, PWM
- ◆ Python Functional Test



Testing functions with Python based scripts, using Bscan accessible nodes as variable

Basics - Test Applications

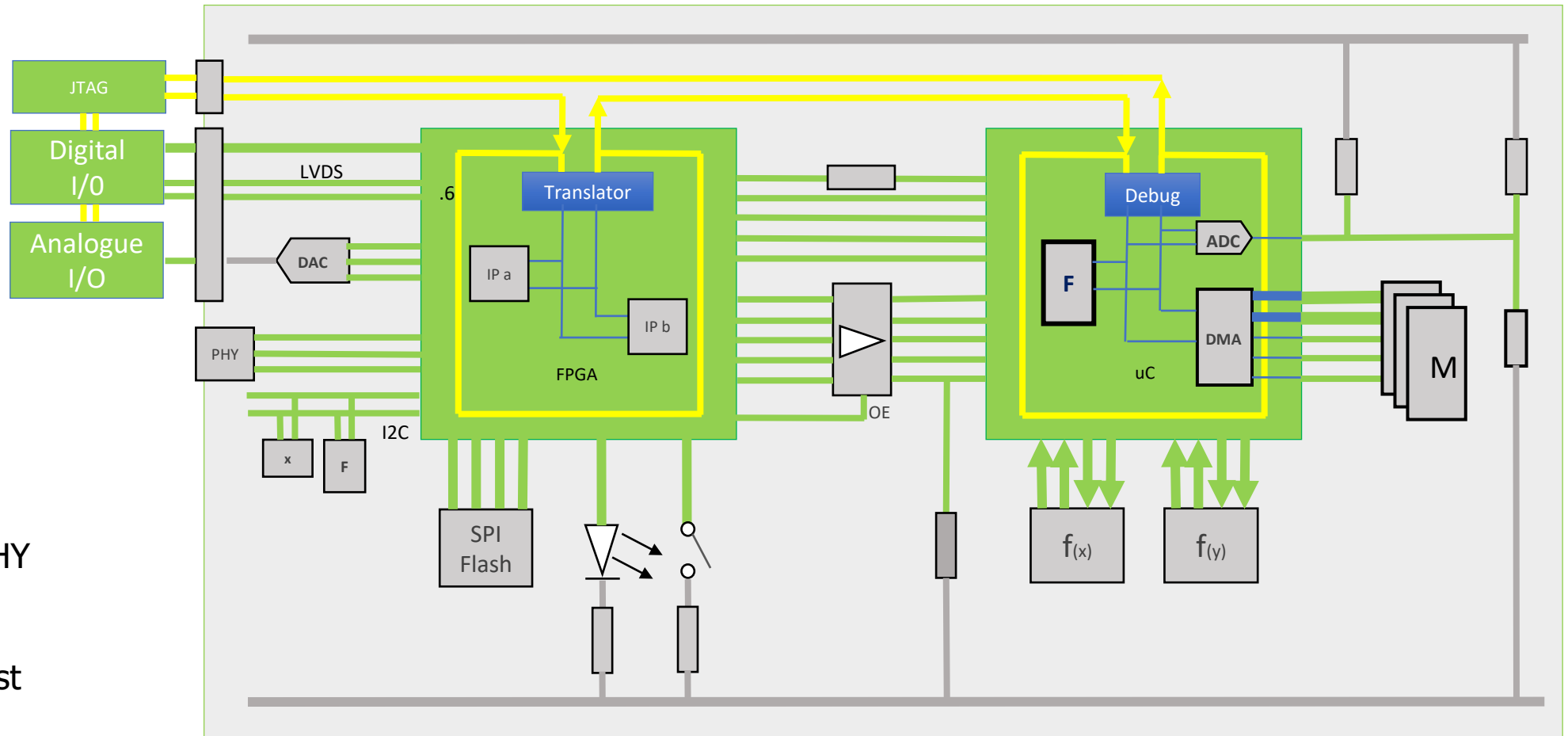
- ◆ Chain
- ◆ Interconnect
- ◆ LEDs
- ◆ Switches
- ◆ Connectors
- ◆ Resistors presence
- ◆ Memory connections
- ◆ LVDS
- ◆ Presence I²C, SPI, PHY
- ◆ Voltage, Freq, PWM
- ◆ Python Functional Test
- ◆ Emulative



Emulative Test for firmware independent @speed Test

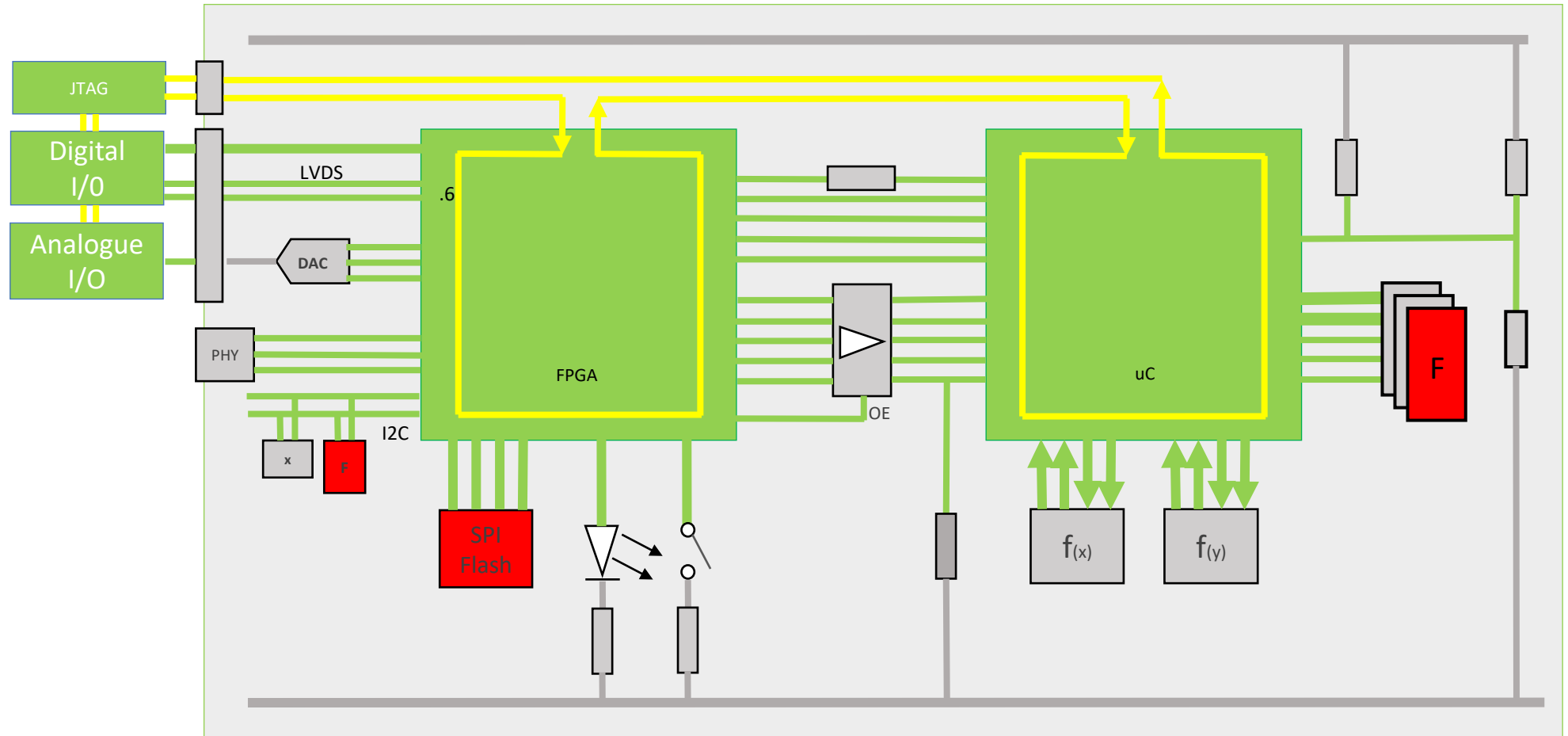
Basics - Test Applications

- ◆ Chain
- ◆ Interconnect
- ◆ LEDs
- ◆ Switches
- ◆ Connectors
- ◆ Resistors presence
- ◆ Memory connections
- ◆ LVDS
- ◆ Presence I²C, SPI, PHY
- ◆ Voltage, Freq, PWM
- ◆ Python Functional Test
- ◆ Emulative



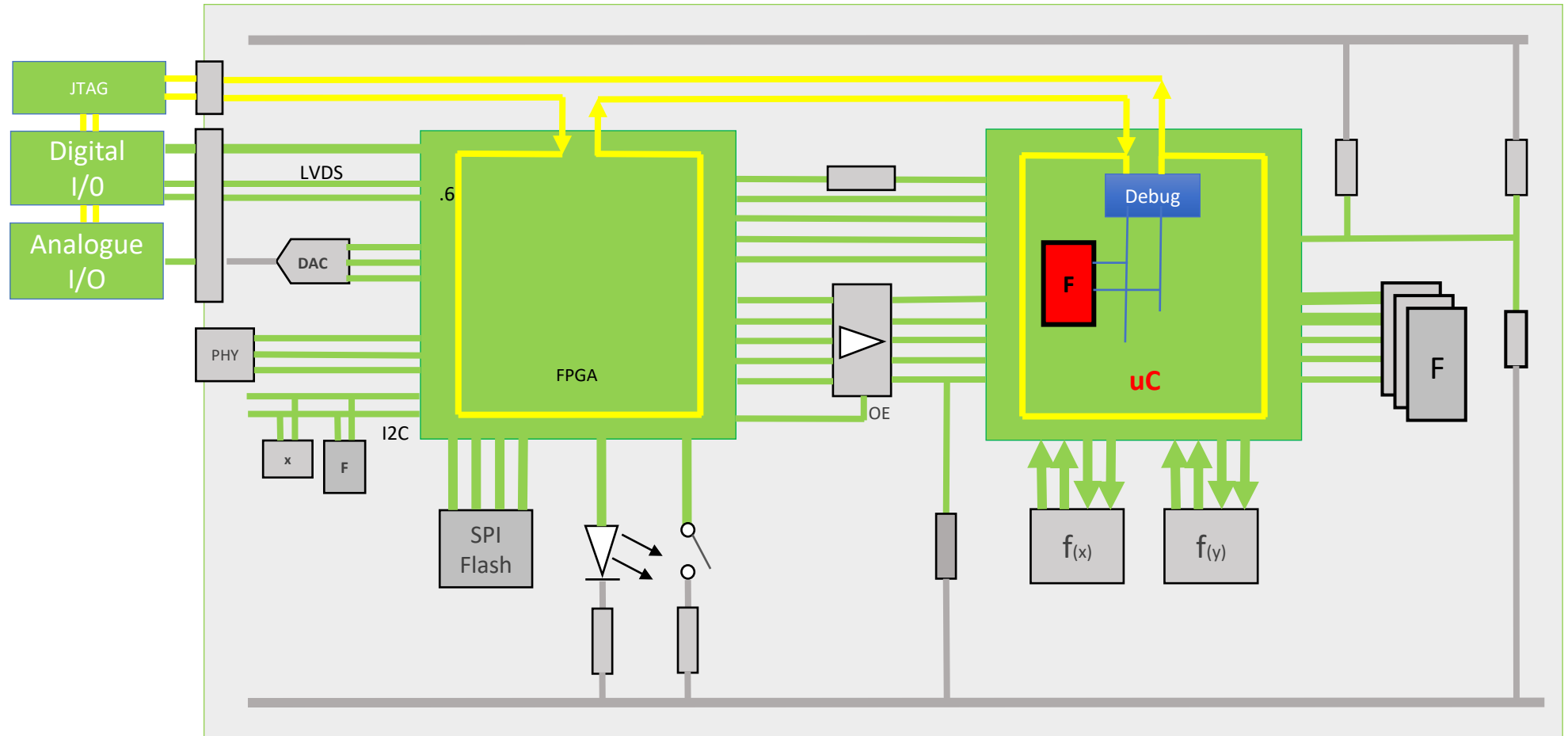
In-System Programming – via Bscan register

- ◆ Flash
- ◆ I²C Flash
- ◆ SPI Flash



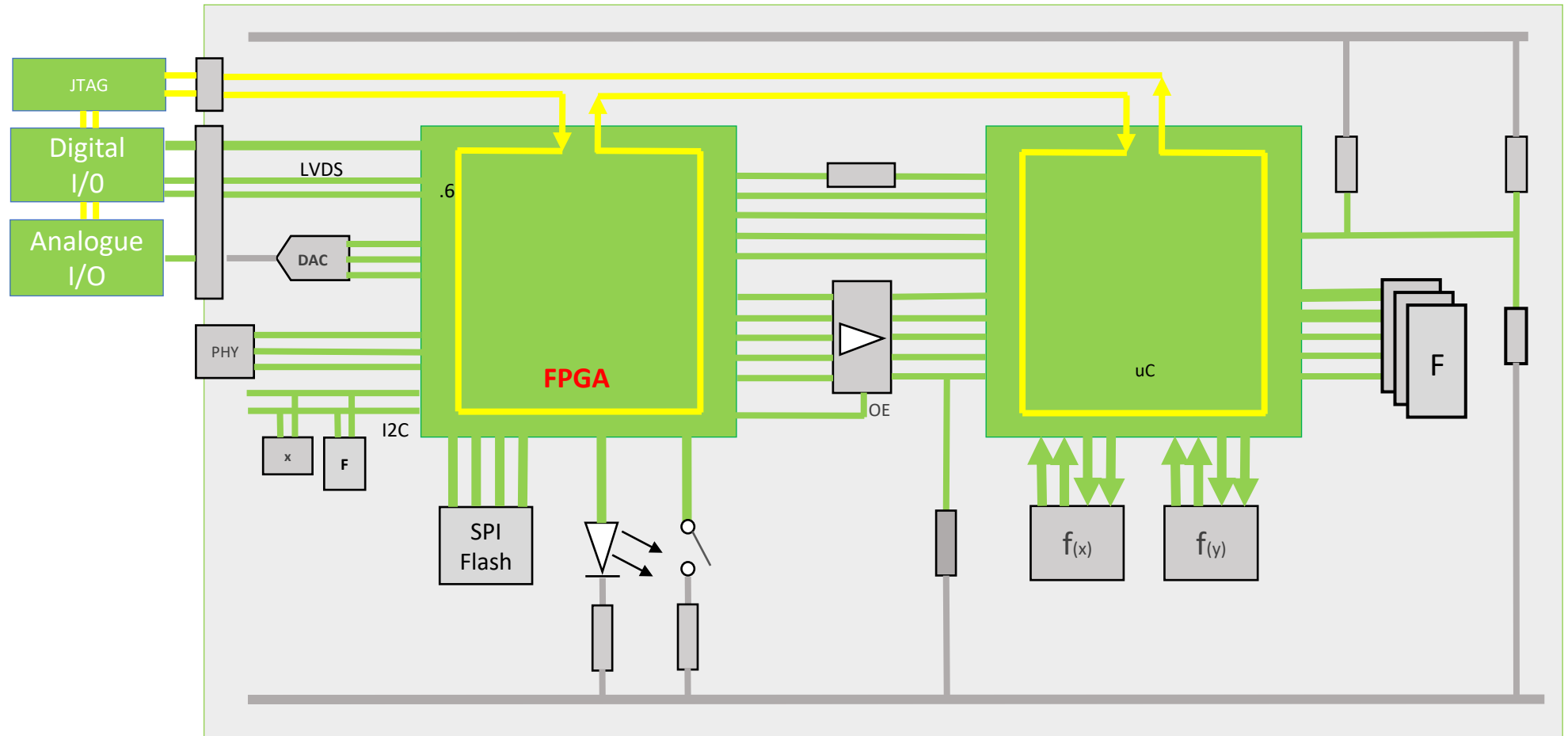
In-System Programming – micro controllers

◆ Internal uC Flash



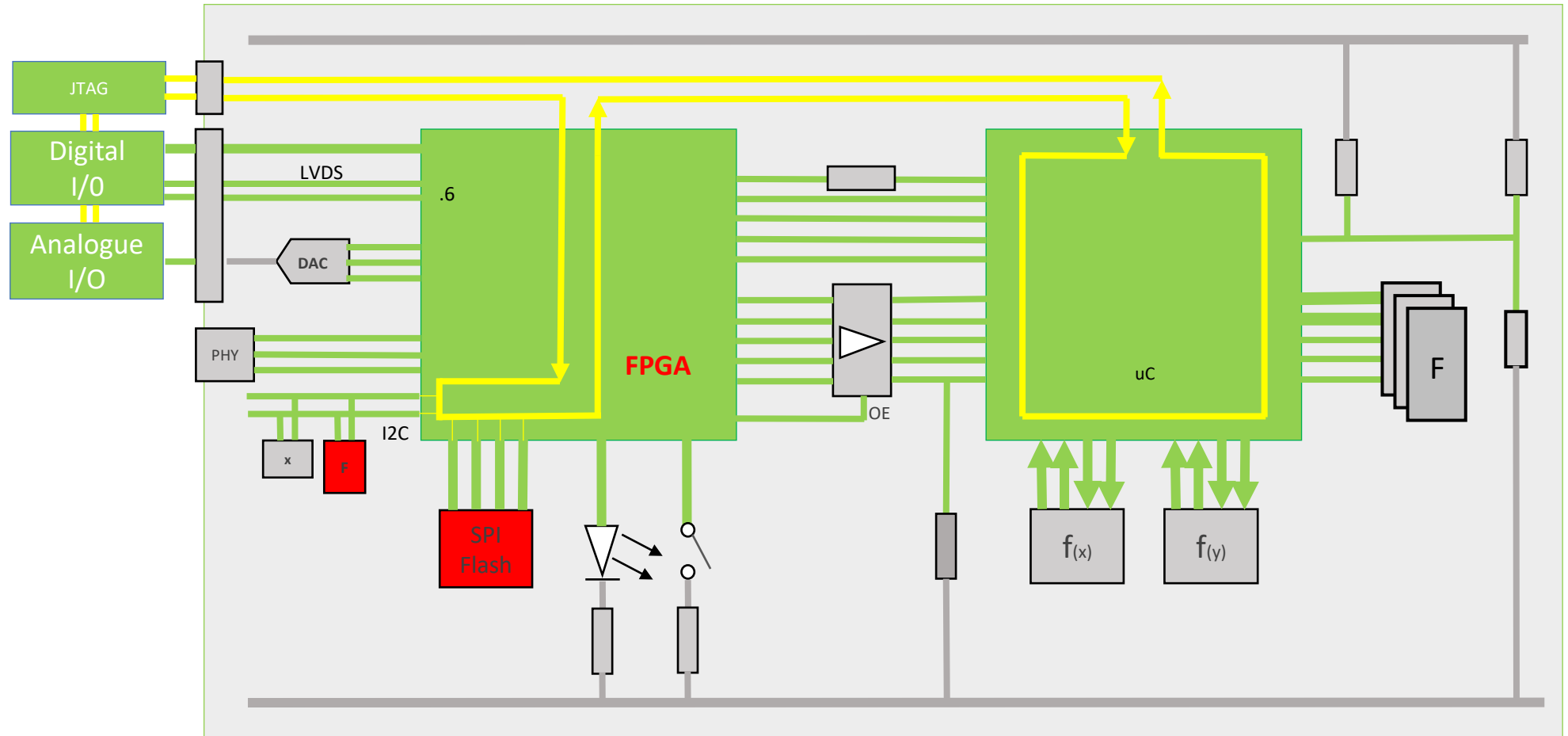
In-System Programming – logic devices

- ◆ SVF
- ◆ JAM
- ◆ STAPL
- ◆ Jedec
- ◆ IEEE 1532



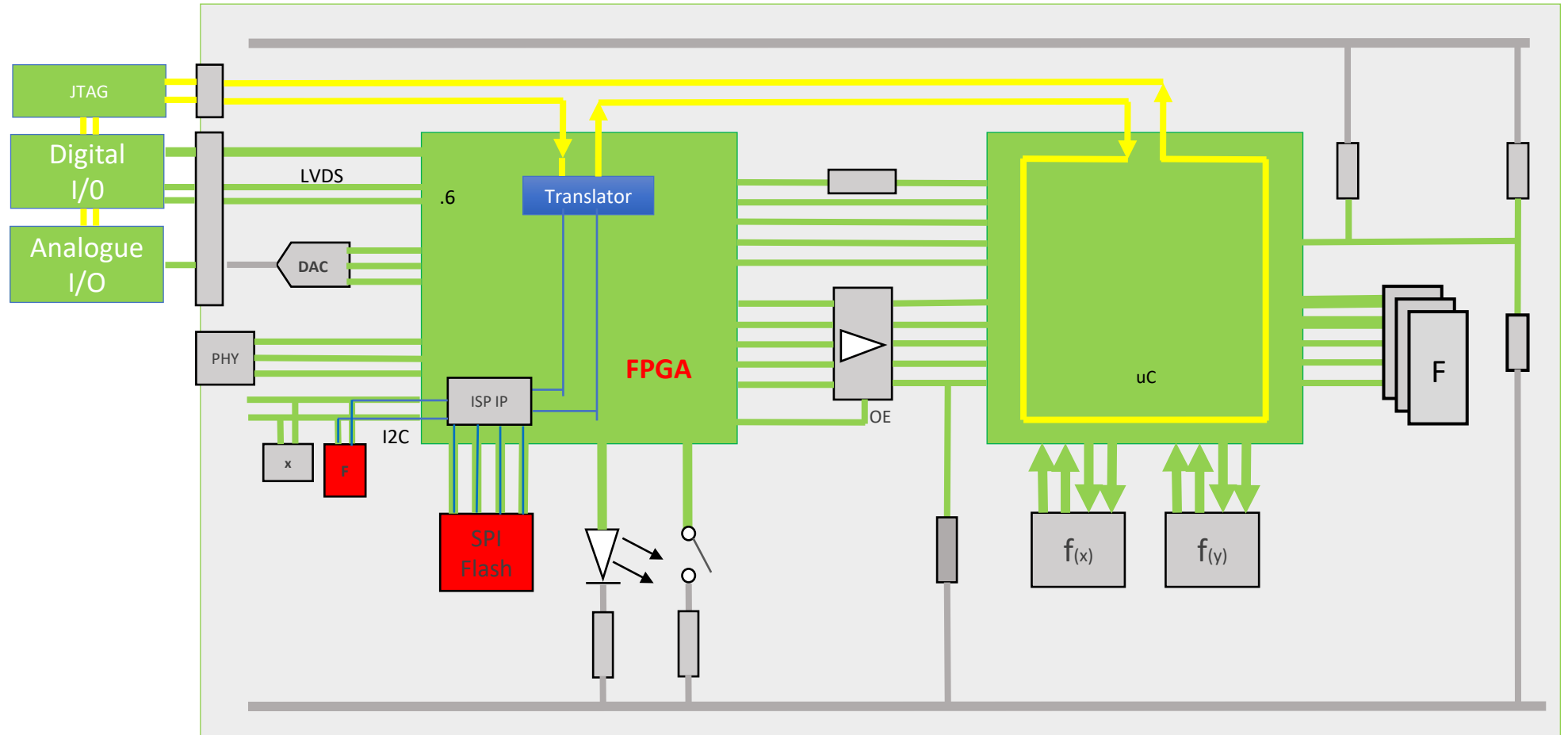
In-System Programming – via short chain

- ◆ Flash
- ◆ I²C Flash
- ◆ SPI Flash

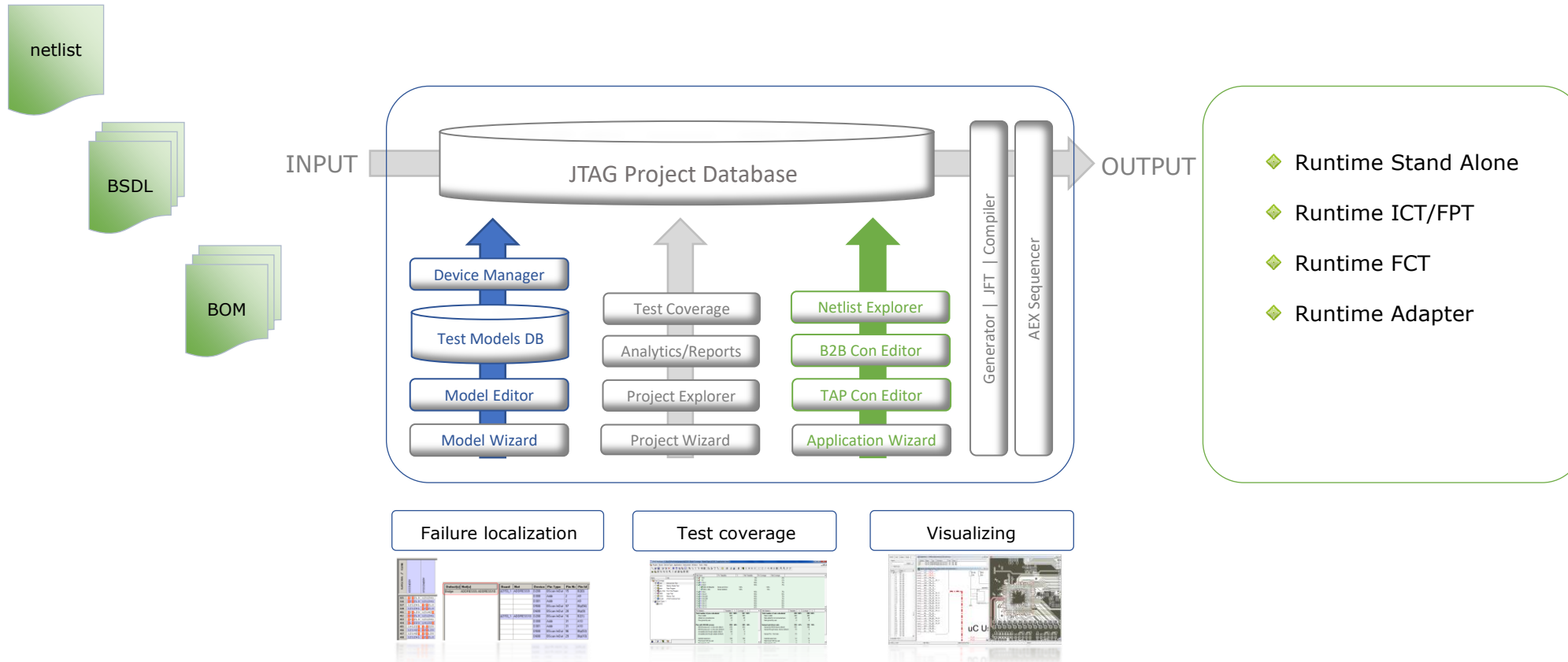


In-System Programming – via embedded programmer

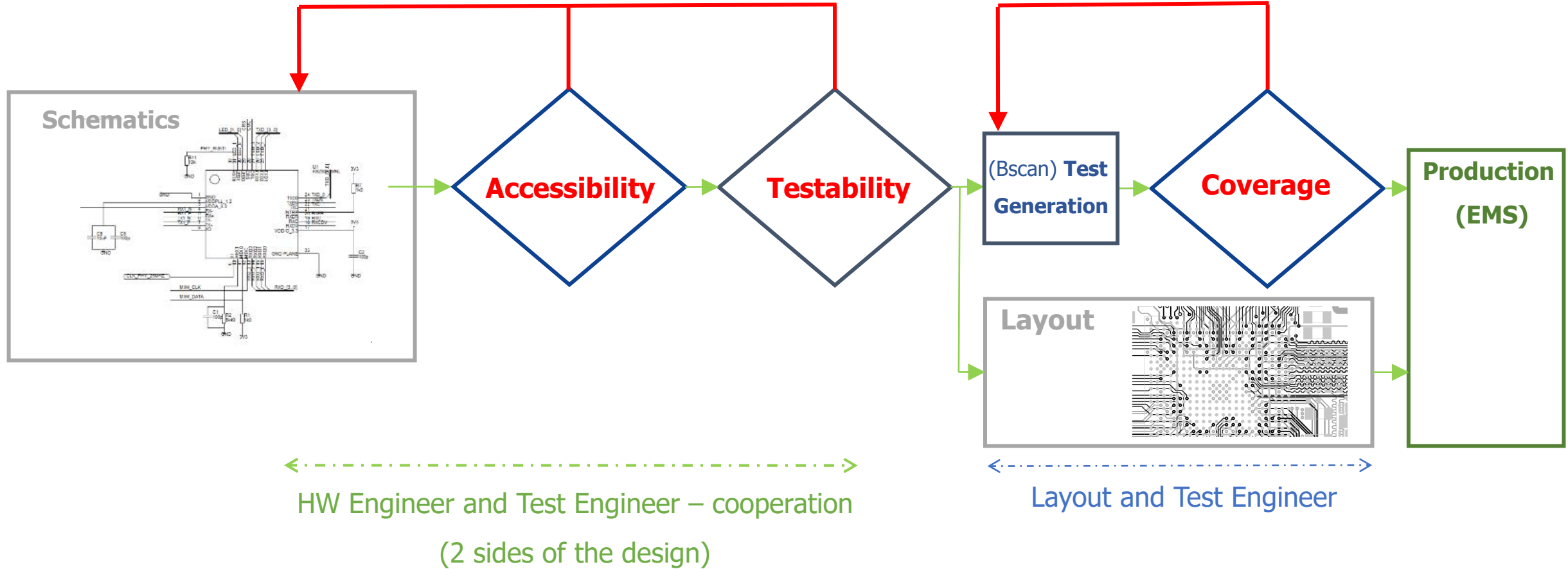
- ◆ I²C Flash
- ◆ SPI Flash
- ◆ Other...



JTAG applications development process



HW engineering process with JTAG



JTAG benefits for engineering

HW Engineer:

- ◆ Prototype boards tested on production failures
- ◆ No firmware required to proof that HW design is correct
- ◆ Less DFT rules
- ◆ Less or no assistance required for repairs during production process or field returns
- ◆ Less or no test pads required

Test Engineer:

- ◆ Faster production test development
- ◆ Higher and known fault coverage
- ◆ Better failure localization

JTAG benefits for the company

Time to market:

- ◆ One Test method that can be used for all product life cycle stages:
 - Prototype
 - Pre-Production
 - Production
 - Field returns
- ◆ Minimizes risk on design iterations

Lower cost:

- ◆ JTAG test equipment can be used for all board types with at least 1 JTAG device
- ◆ Less unrepairable boards

JTAG Technologies B.V.

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