New Possibilities by Heterogeneous Multicore CPUs

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FS Elektronik Systeme

Adelco Electronics bv

- Founded in April 2003
- Specialized in the distribution of high-end electronic components
- Solution provider for Displays, Embedded Computing and Wireless Products
- Experienced and technically skilled sales team providing application support
- Headquarter in Capelle aan den IJssel/NL
- Sales office in Belgium

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F&S Elektronik Systeme GmbH

- 20 years of experience in the embedded market
- COM/SOM modules and Single Board Computers
  - 60% medical applications
  - Our customers value our quality, ruggedness, innovation, long-term availability and price-performance ratio
- Development and Production in Germany
  - ISO 9001 certified
  - Freescale Proven Partner

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Agenda

- Introduction
- Heterogeneous Multicore Processors
- Freescale Vybrid
- Freescale i.MX 6SoloX
- Freescale Internal Architecture
- Interprocessor Communication
- Fast Boot
- Power Consumption
- Security Features
- Real-time
- Memory Protection
- Summary

Introduction

- Requirements changed dramatically

- High-resolution displays
- Touch with gesture control
- Voice control
- Cloud Connection
- Security

Powerful Processor and modern OS needed

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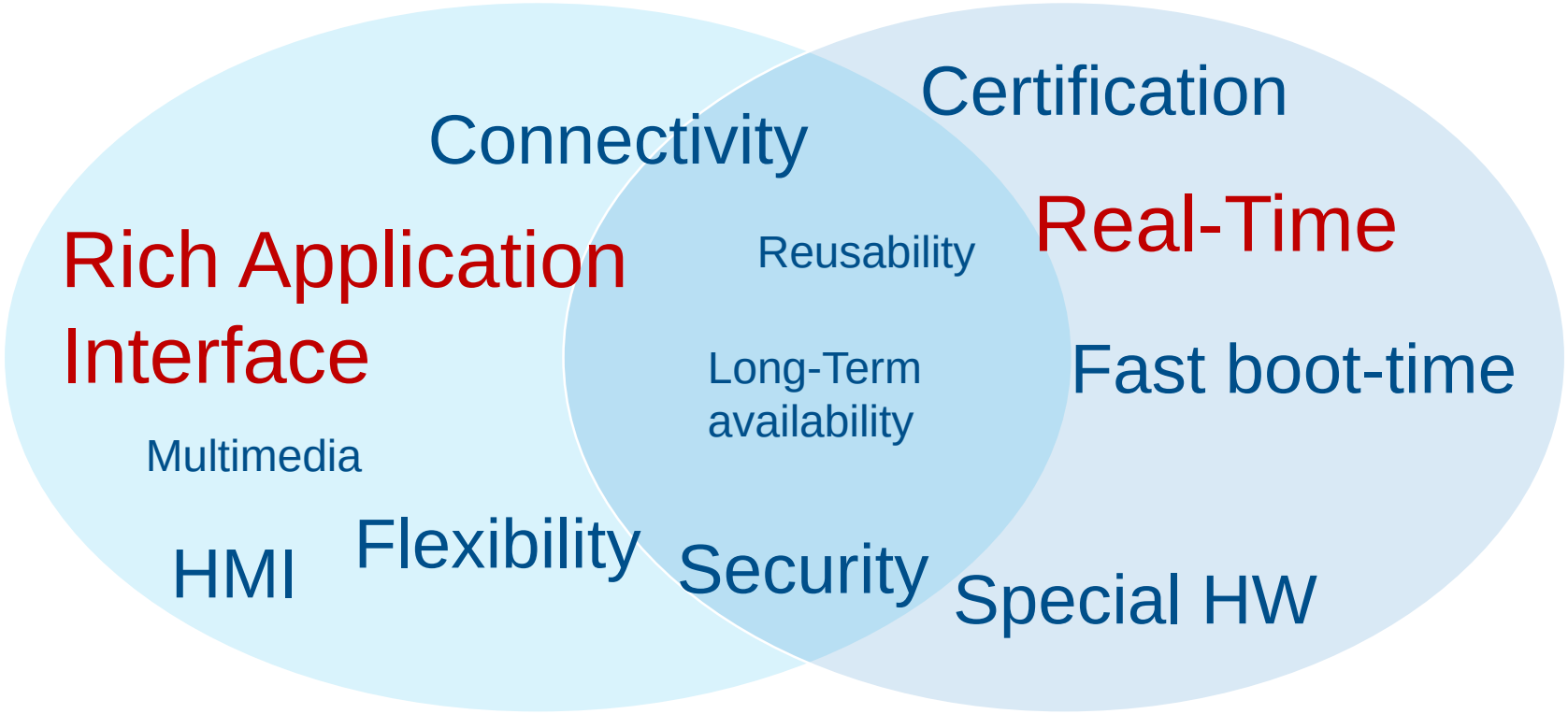
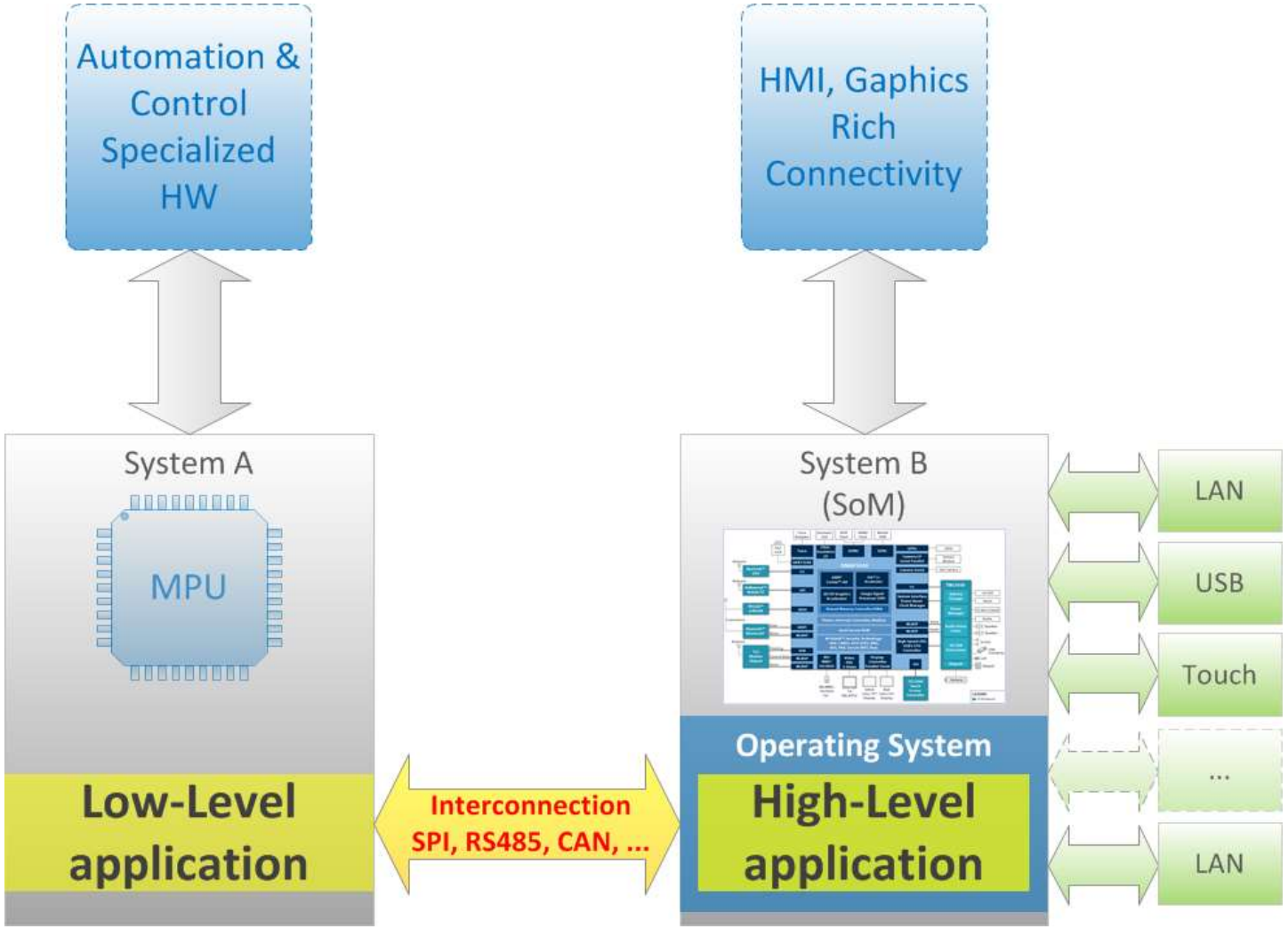
Introduction

How to integrate all these challenges?



One single system is not able to meet all these requirements

Introduction



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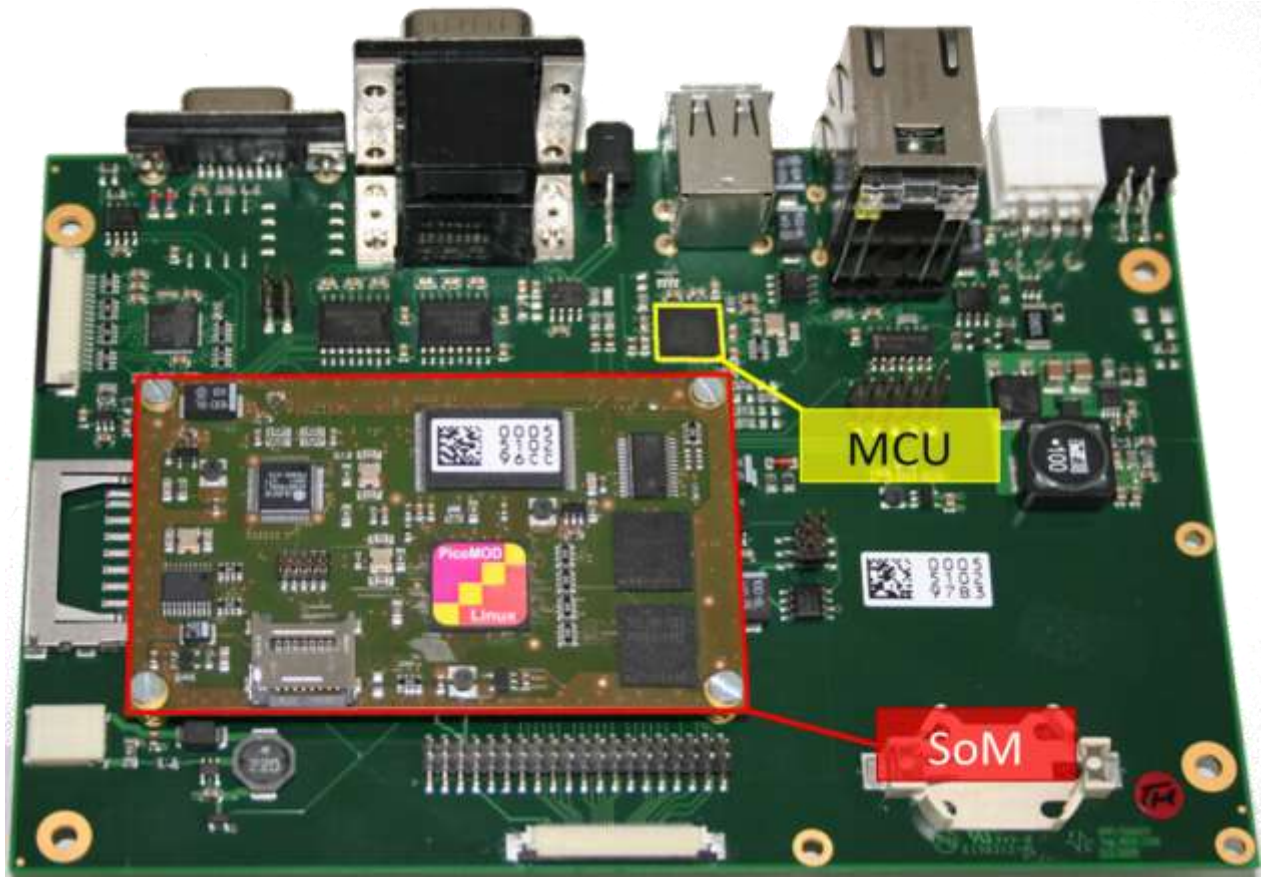
Introduction



Carrier Board with Interfaces, Microcontroller and ARM Module

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Introduction

Disadvantages of a two-part solution:

- 2 systems ⇨ 2 sources of error
- Longevity?
- Increasing in complexity
  - Hardware development
  - Different development environments
- Slower time to market
- Increased price
- Compactness
- Limited interconnection

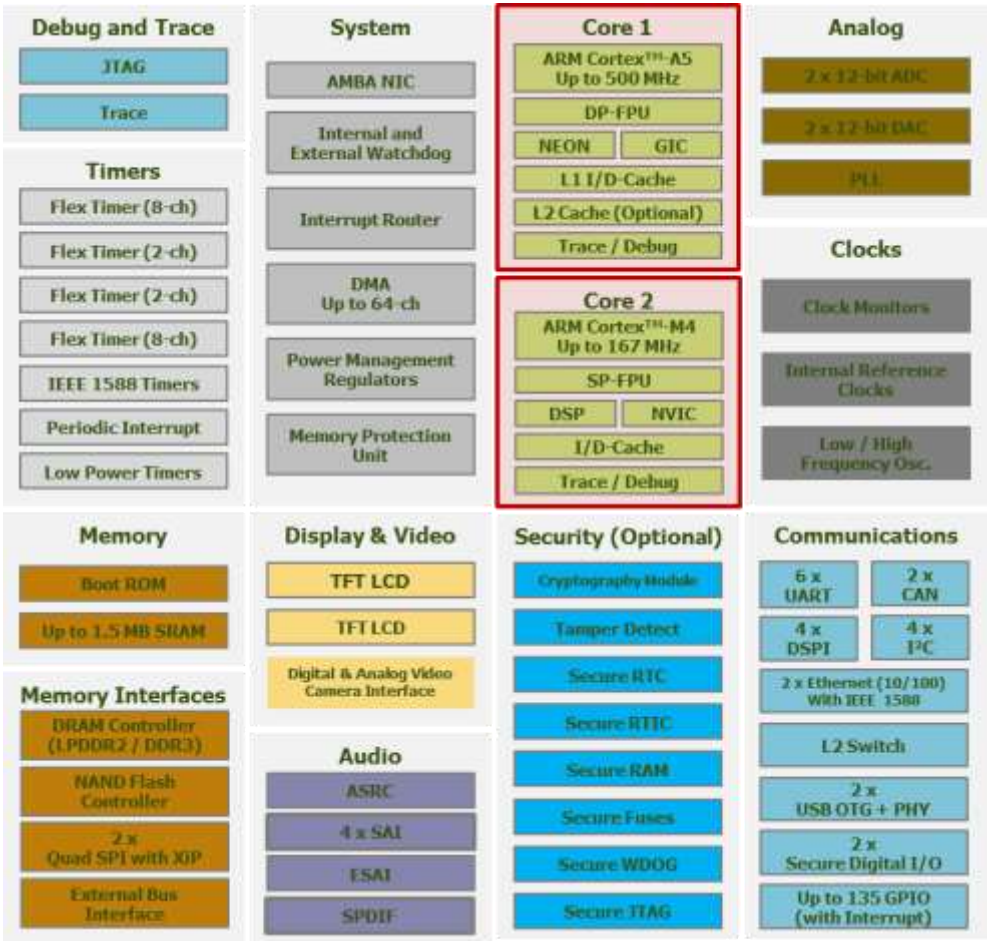
Solution: Multicore Processor?

Heterogeneous Multicore Processors

- Different types of cores in one processor
- Shared Bus Topology
- Asymmetrical processors are not binary compatible
  - ➲ Each core needs its own software execution environment

- Motivation for this concept
  - Real-Time performance
  - Power consumption
  - Fast boot
  - System integrity → Memory protection
  - Security

Freescale Vybrid



- Two cores
  - Cortex-A5
  - Cortex-M4
- Extensive periphery
  - CAN, USB, SDIO
  - I^2C, UART, LAN
- Integrated memory
  - 512kB SRAM with ECC
  - 512kB Graphic SRAM

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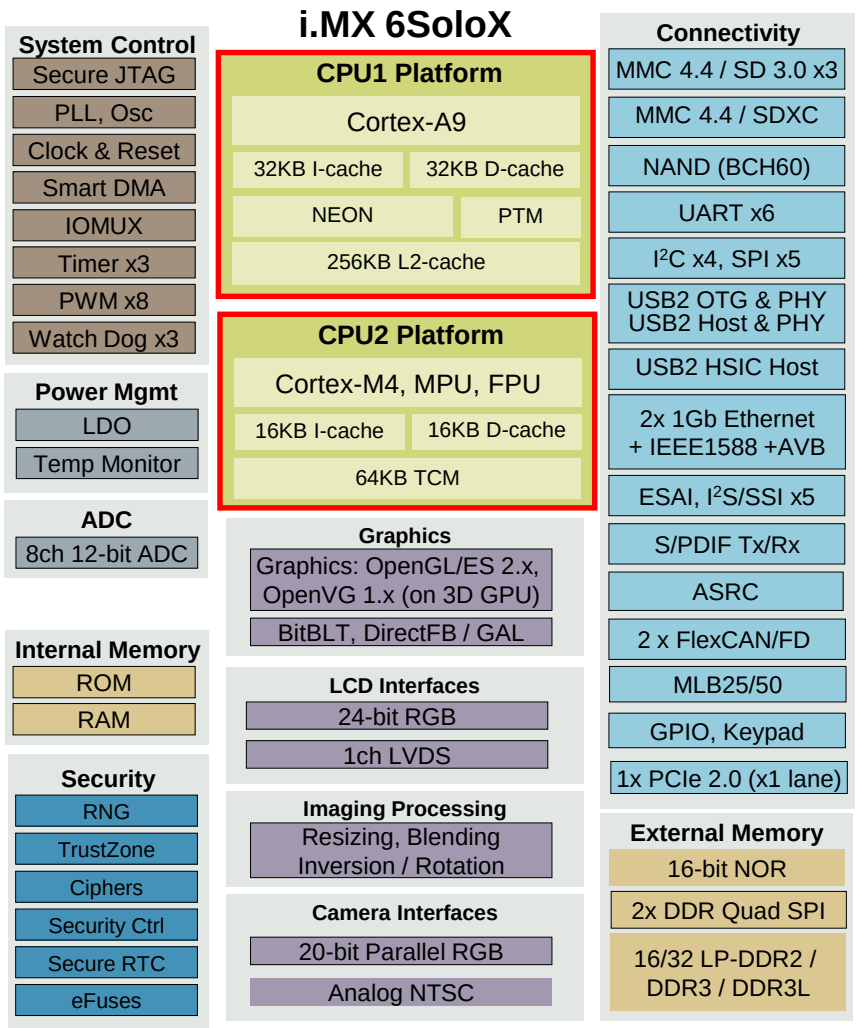
Freescale i.MX 6SoloX



- Two cores
  - Cortex-A9
  - Cortex-M4
- Extensive periphery
  - CAN, USB, SDIO
  - I^2C, UART, 2x Gb LAN
- Graphics
  - OpenGL
  - RGB and LVDS

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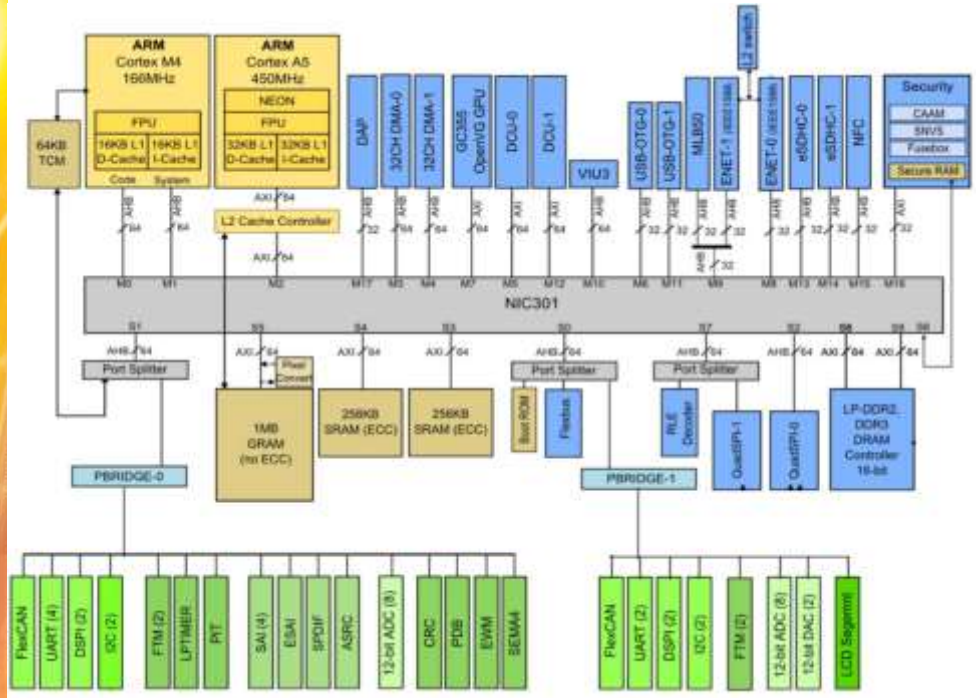
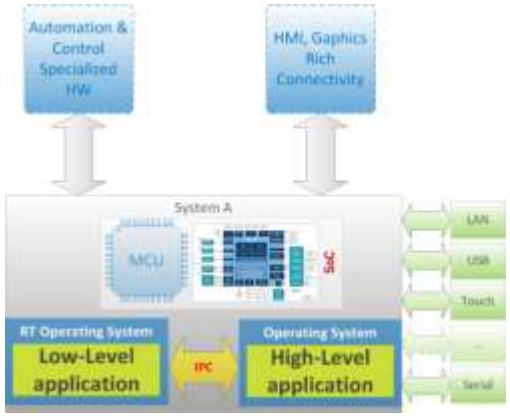
Freescale Internal Architecture



- Central Interconnect Matrix
  NIC 301 connects Masters and Slaves
- Master:
  Cores and interfaces with DMA
- Slaves:
  Peripherals and memory
- NIC 301:
  only 1:1 connections possible
  - ➲ Important masters/slaves have two interfaces to limit re-configuration of bus matrix

Interprocessor Communication Fast and Secure

- Shared Memory
  - Internal SRAM
  - External RAM
- Hardware Semaphore Unit
  - Easy to use hardware mechanism to safely share resources between the two cores
- Messaging Unit
  - Send messages from one core to the other
  - Interrupts for send and receive
  - Four RX/TX registers per core
- Interprocessor Interrupts (IPI)
- ARMv7/ Idrex/ strex
  - Exclusive memory access instructions



- ➲ Very fast communication channels
- ➲ Communication is inside of the device

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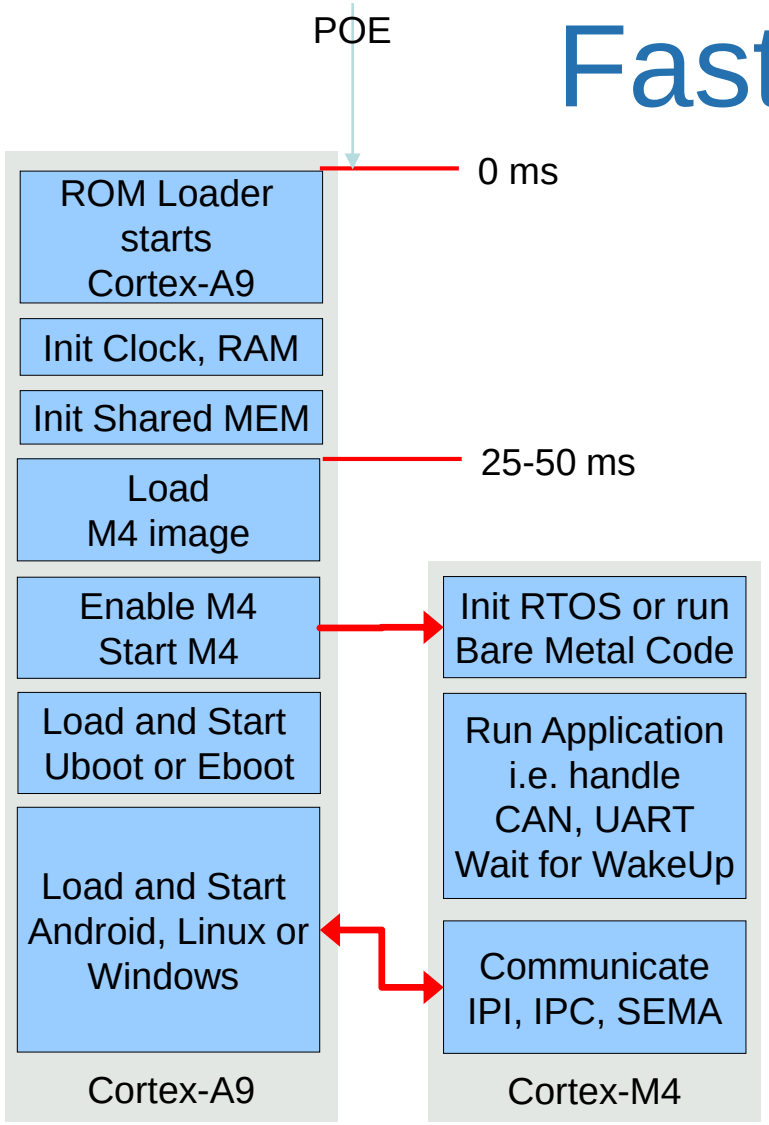
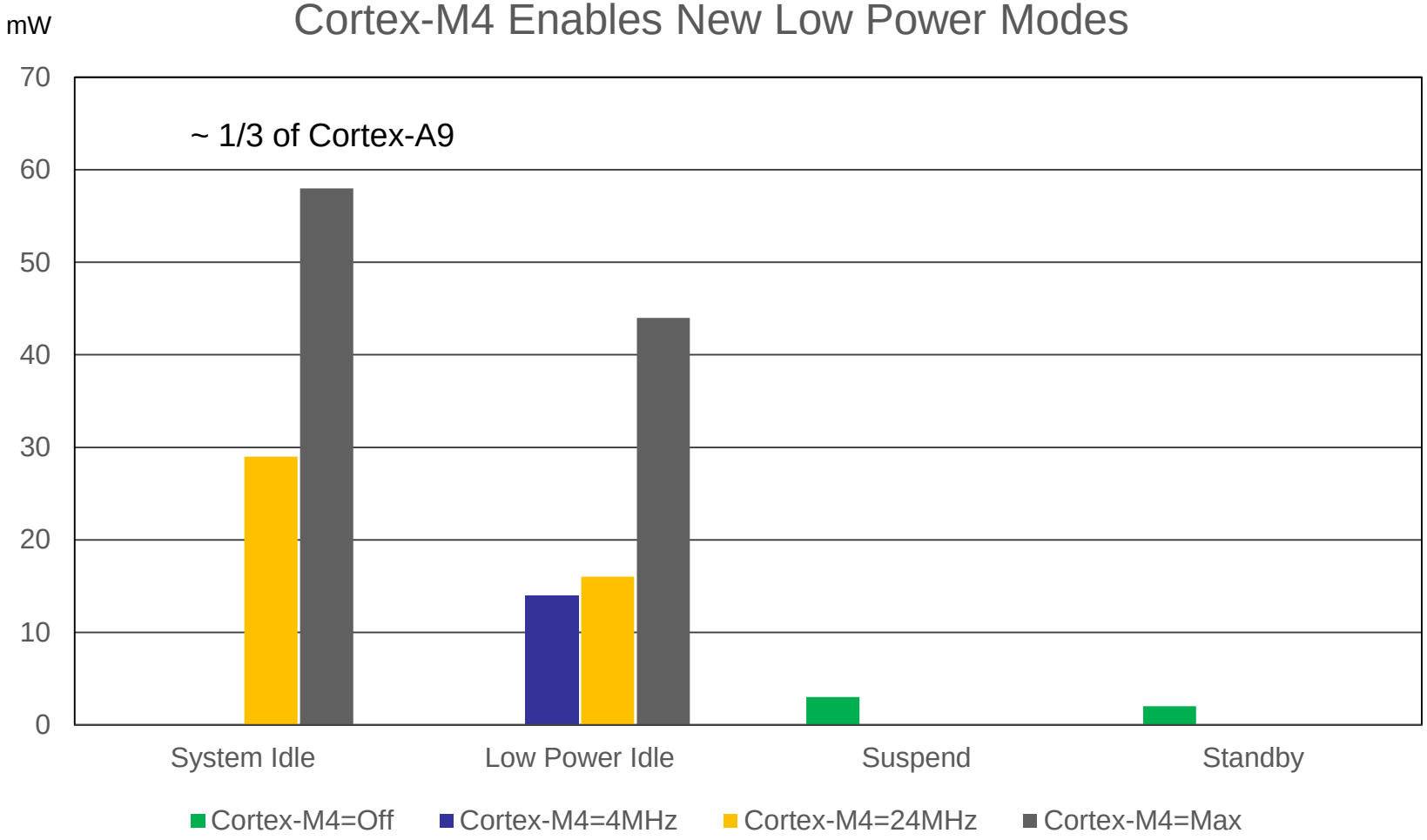
Fast Boot



- Cortex-A always boots first
- Boot medium is set by eFUSES
- Booting from NAND or NOR Flash
  - recommended in industrial environments
- M4 stays in reset after chip reset
- M4 program can be loaded in TCM
  - fast execution and good real-time capabilities
- Secure and/or encrypted boot is supported for Cortex-A9 and Cortex-M4

Power Consumption



* Cortex-A9 is power gated, Cortex-M4 is running and can wake up Cortex-A9

Security Features

- Requirements
  - Protection of intellectual property
  - Protection against manipulation
  - Protection of personal data

- Cortex-M4 can re-use security features of Cortex-A9

- High Assurance Boot is possible for all SW parts of the system

Security Features

- Freescale i.MX 6SoloX Security Components:
  - Secure High Assurance Boot (HAB)
  - AES, DES/3DES, SHA-1, SHA-224, SHA-256 encryption
  - Watchdog timing of Image for changes
  - Random generator in accordance with NIST SP800-90
  - Safe real-time clock (no manipulation possible)
  - Unique device number, saved in eFUSES (UUID)
  - Protection against manipulation of hardware (Tamper Detection) with Memory Erase
  - ARM TrustZone Architecture

Small microcontrollers do not have these components

Real-time Behavior of Both Cores

Which core is better for real-time applications?

Cortex-A

+ Cortex-A has a faster clock rate than M4 (1GHz to 200MHz)
– Data/Code need to be in cache to get quick access to DRAM (→ hard when OS runs)

Cortex-M4

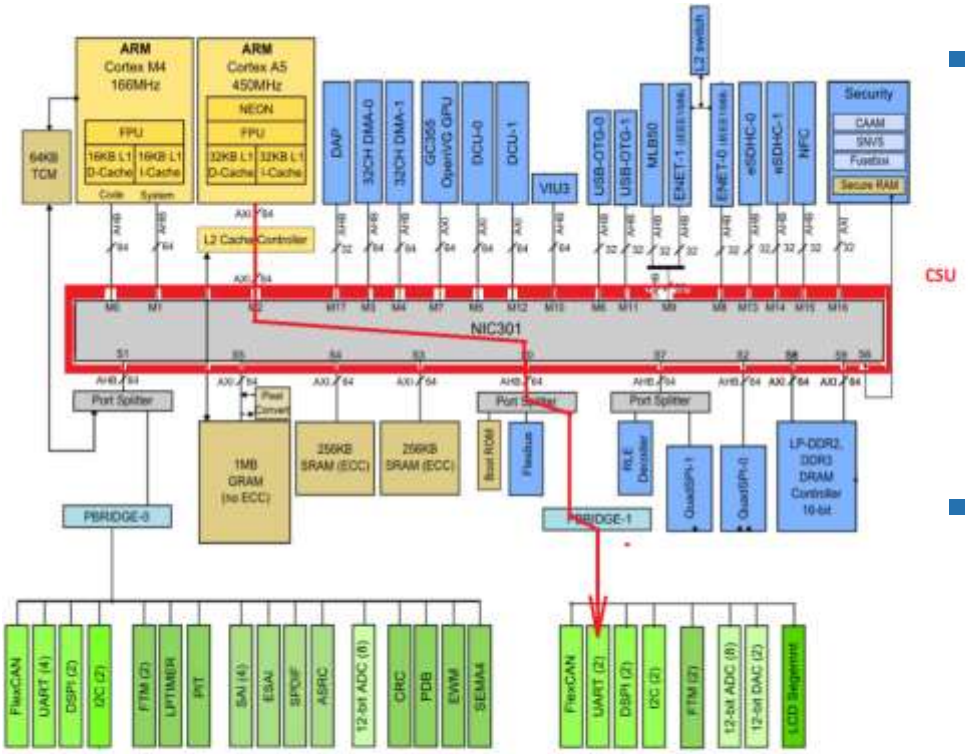
+ fast, if data and code are in TCM (64kB), M4 can access program/data without crossing interconnect Matrix (NIC301)
– Slower clock rate

Memory Protection

- Problem with safety-critical tasks:
  - Software must not be influenced by each other
- Both cores can access the same memory areas and periphery
  - ➲ Limitation by Hardware

- Solution:
  - CSU Firewall
  - Trust Zone Controller
  - NIC
  - RDC Resource Domain Controller

Memory Protection



- Settings for Master
  - User/Supervisor
  - TrustZone/non TrustZone
  - „which slave can be accessed“
- Settings for Slave
  - Who can access TrustZone/nonTrustZone
  - Read/Write

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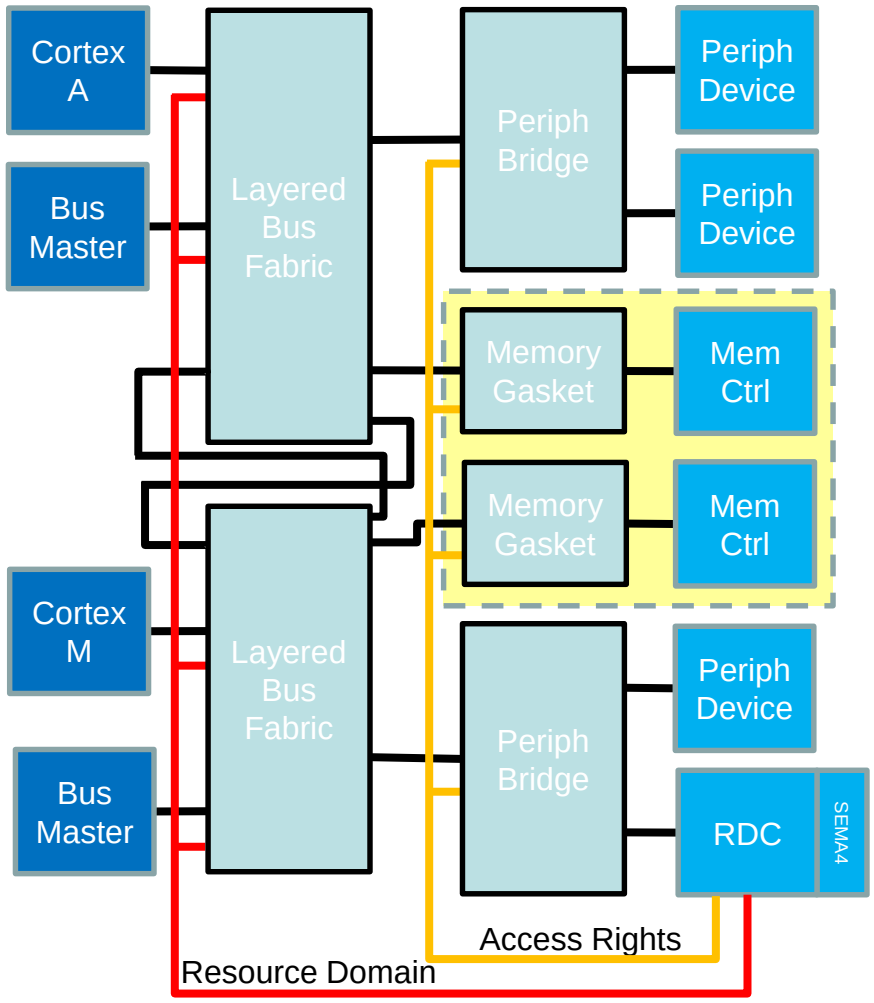
Memory Protection Resource Domain Controller

- Assign Bus Masters to Domain
- Add Peripherals (read only or read/write)
- Add memory Regions (read only or read/write)



Summary

Pros and cons of a heterogeneous multicore processor:

Pro

+ Fast communication possibilities between both systems
+ Better MTBF, since less components
+ Price reduction, since only one processor system
+ µC can access all interfaces of the application processor
+ Easy SW Update of µC in field
+ Flexibility to enable low-power processing

Contra

- Complex programming of RDC/CSU/TrustZone
- Separation of resources requires in-depth knowledge of architecture

Summary

- Heterogeneous multicore processors are an alternative to classic structures
- Future:
  - More heterogeneous CPU families
    - ➲ Freescale i.MX SoloX/Vybrid know-how stays relevant

Questions?

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