DESIGN AUTOMATION EMBEDDED SYSTEMS
SECURITY/FPGA - EMBEDDED - INTERNET OF THINGS - ELECTRONIC DESIGN/PRODUCTION - TESTING
4 NOV
1931 CONGRESCENTRUM BRABANTHALLEN DEN BOSCH
D&E event 2015

Advanced PCB checks without being a Signal Integrity Expert

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CB Distribution bv
www.cb-distribution.nl

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CB Distribution

- Started 2004
- Cadence Channel Partner Netherlands, Belgium, Luxembourgh, Spain and Portugal
- Located in Hengelo (Netherlands) and Tres Cantos – Madrid (Spain)
- Sales and Support of
  - Cadence IC-, PCB- and Packaging-Tools
  - OrCAD
  - WISE GerbTool
  - Nextra three-dimensional PCB design
  - Dassault, Enovia DDM/PLM environment

Training and Services

- Training
  - Tool and methodology
- CAD Support
  - Availability of software binaries
  - Setup and maintenance of licenses
  - Project environment setup
  - Scripts
  - Setup and maintenance of data transfer
  - Conversions
- IT Support
  - Setup, maintenance and support of
  - VPN, Remote Desktop Machine(s), Virtual servers

Agenda

- The gap between DRC and SI simulations
- Introducing new PCB checks
- Applications and examples
- Conclusion

More PCB designs require SI analysis

- Higher design frequencies
- Rising/falling edges getting smaller.
  - With a rising edge of 1ns you already see reflections on traces longer then 2.5 cm.
  - Longer than 7.5 cm you see significant reflections.
- This also applies to crosstalk and EMI.

DRC is the starting point of a good PCB design

- Good PCB SI design starts with adequate DRCs in layout tools.
- Today's designs are getting complicated, DRCs are getting complicated too.
- General limitations for complicated DRCs.
  - Complicated DRCs are normally harder to set up.
  - PCB designs are still measured in mil/mm, so the rules tend to be more conservative.

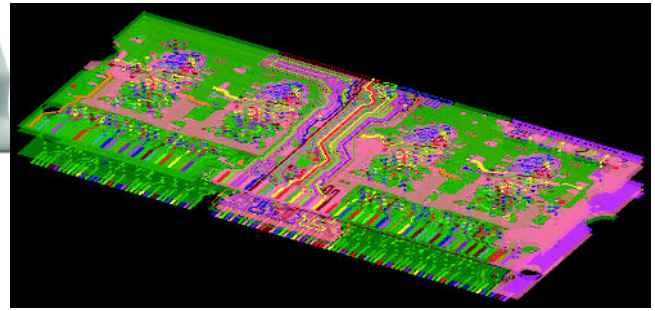
The gap between DRC and SI performance

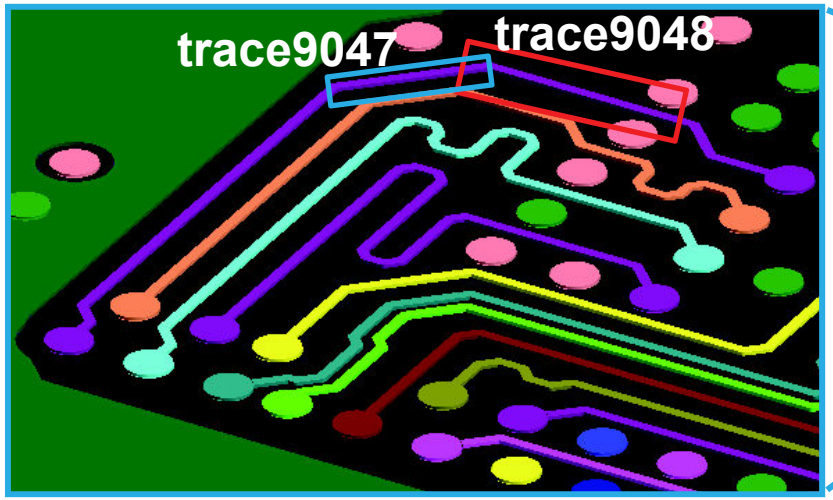
- The gap between layout designers and SI engineers is huge.
  - Have different design expertise.
  - Using different tools.
  - Measured by different units.

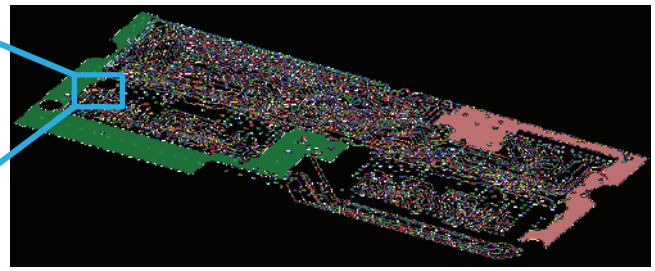
Two trace segments example DDR3 SODIMM

- 2 trace segments for net DQ0 on layer3 of an 6-layer board.

Zoom in on 2 trace segments on Layer3

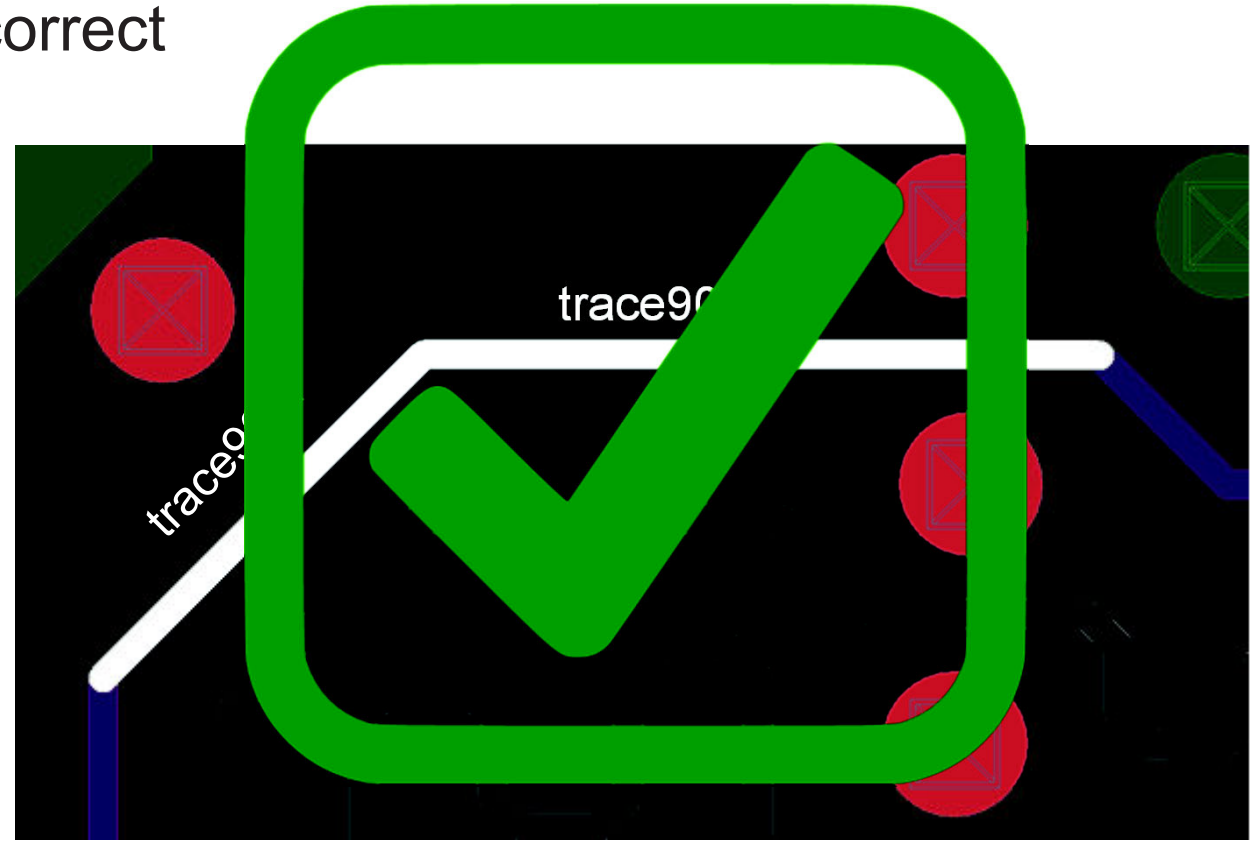






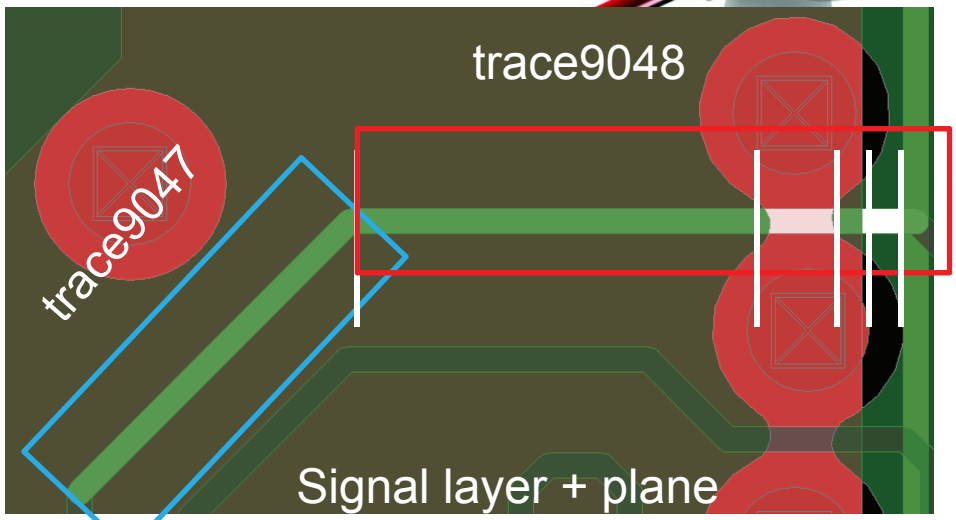
DRC – Simplified impedance view

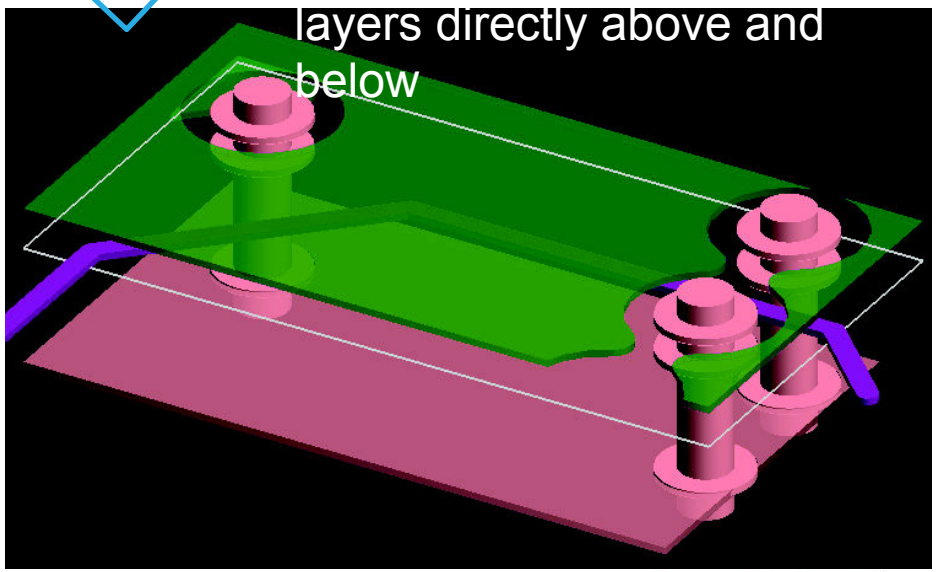
- 2 trace segments, same trace width, same impedance
- You can also see trace segment length
- DRC correct



If you look close enough…

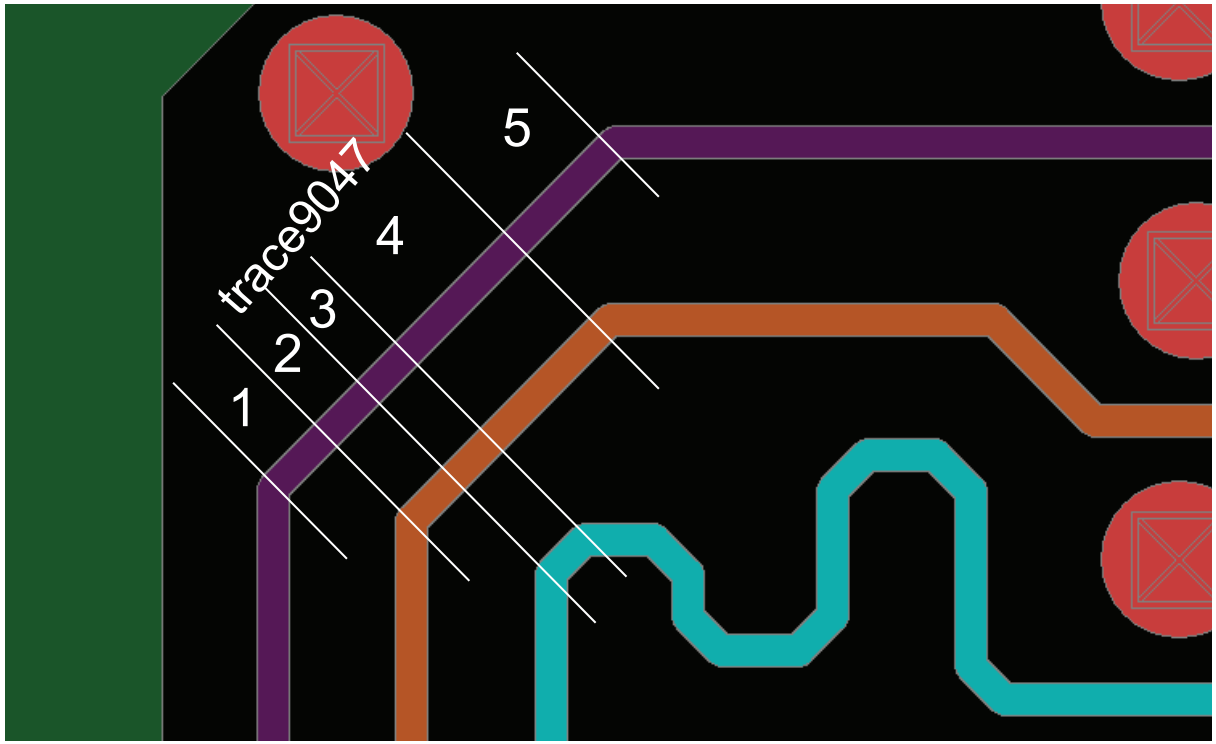
- Trace9047: one uniform impedance section
- Trace9048: 4 impedance sections





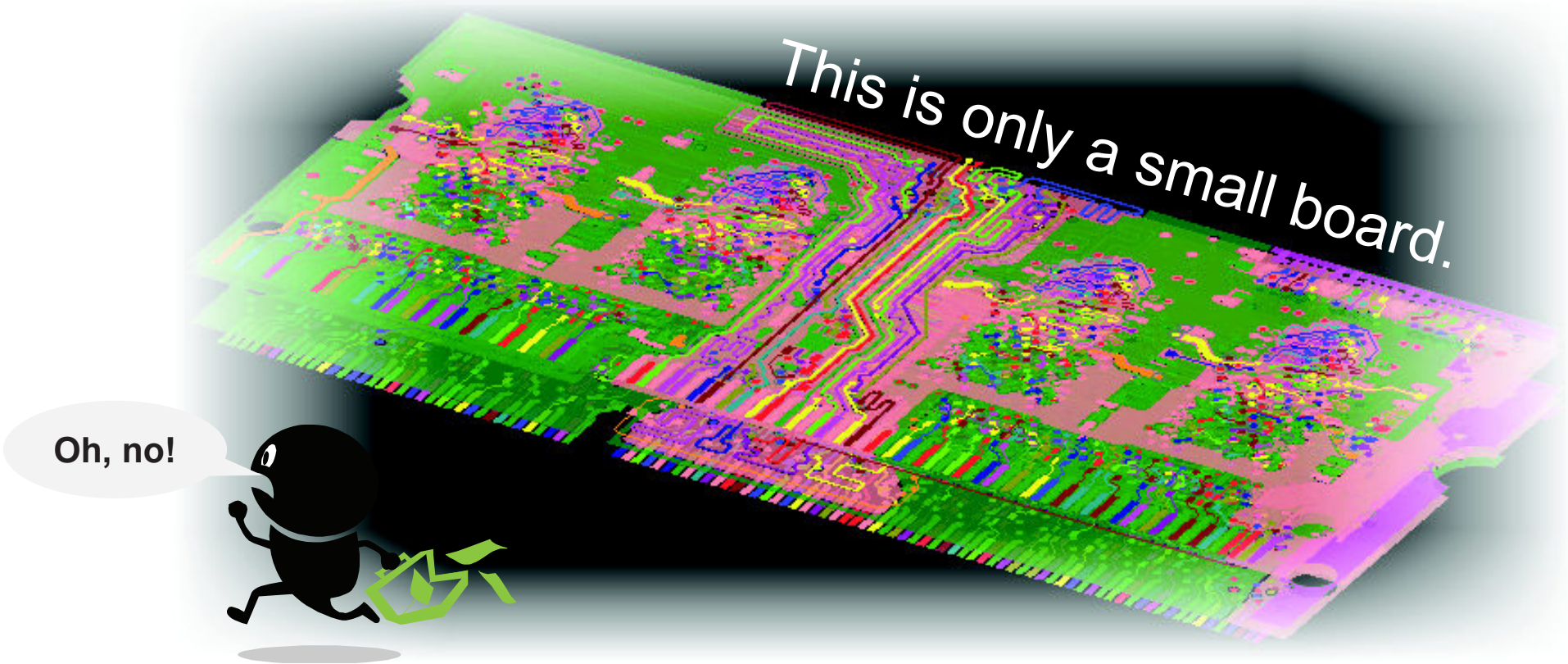
Trace coupling

- Trace9047 broken into 5 sections based on trace coupling
  - two no coupling sections (1 & 5)
  - two 2-line coupling sections (2 & 4)
  - one 3-line coupling section (3)



From 2 trace segments to entire board

- How to analyze the entire SODIMM?



Agenda

- The gap between DRC and SI simulations
- Introducing new PCB checks
- Applications and examples
- Conclusion

ERC and SRC filling the gap

- ERC and SRC filling the gap between layout designers and SI engineers
  - Expanded expertise
  - Using same tools
  - Measured by same units

Layout/Board designer

Layout tools

Geometry domain (mil/mm)

SI Engineer

Simulation tools

Electrical domain (mv, ps)

What is ERC ?

- ERC – Electrical Rule Check
- ERC is individual, segment-level view in geometry domain for PCB's SI performance with
  - Trace reference
  - Trace reference-aware impedance
  - Trace reference-aware coupling
  - Differential pair routing phase
  - # of vias and via locations, ….

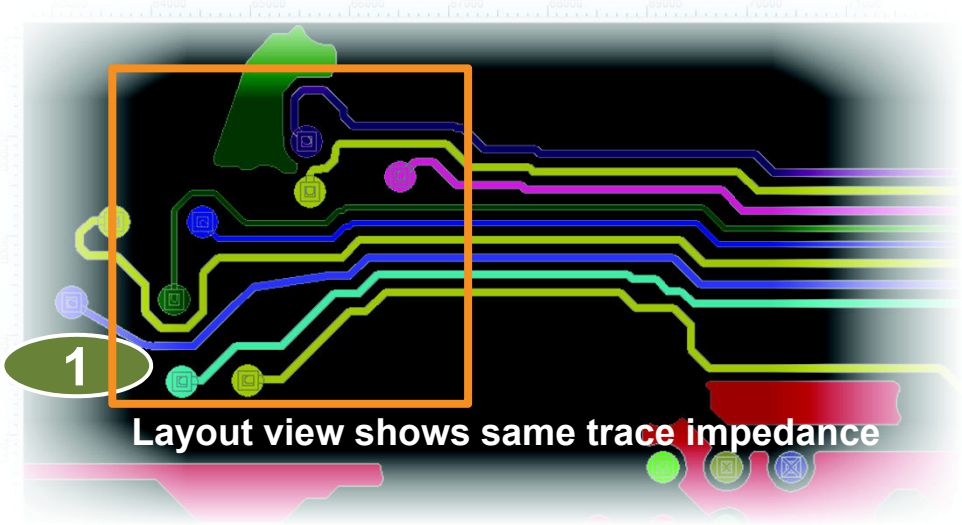
1

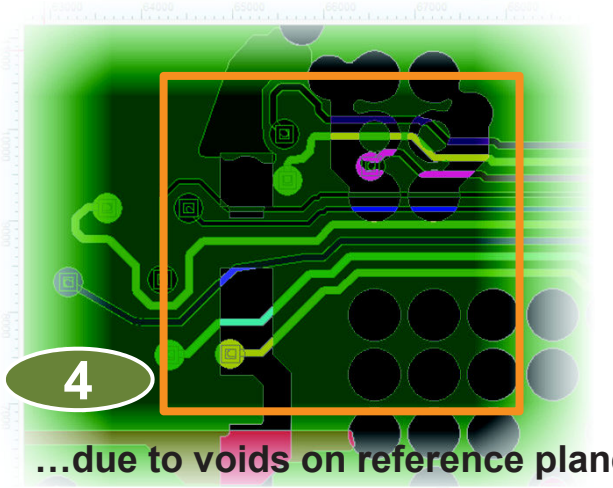
  - Organized for easy SI performance interpretation
  - Practical for board level check (setup, simulation, report)

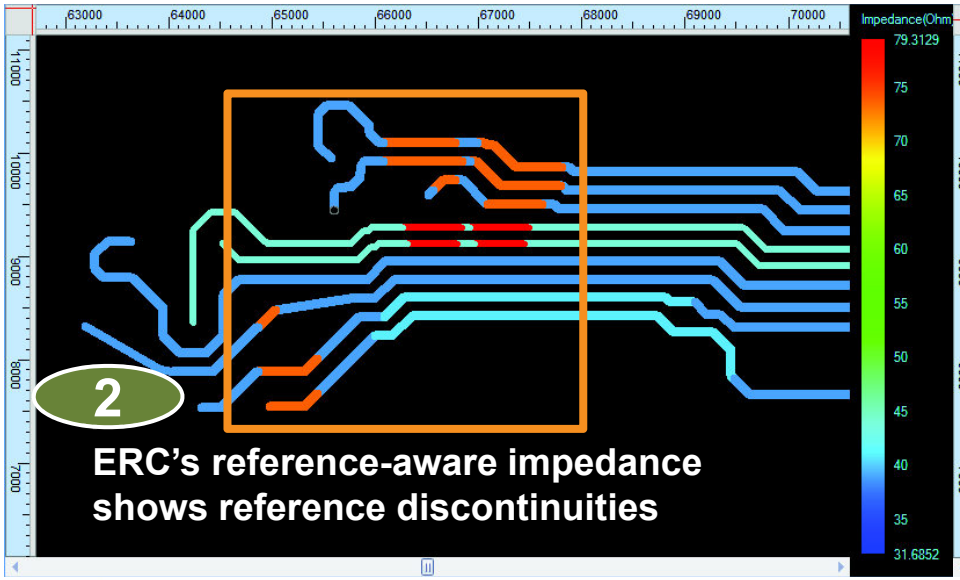
2

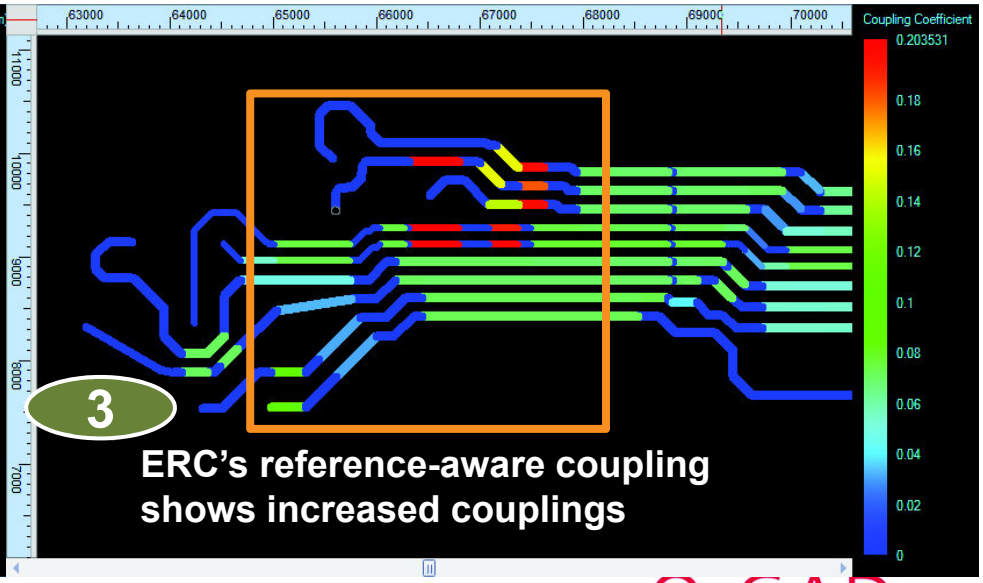
< 2min 10-20min auto

ERC’s reference-aware impedance/coupling check

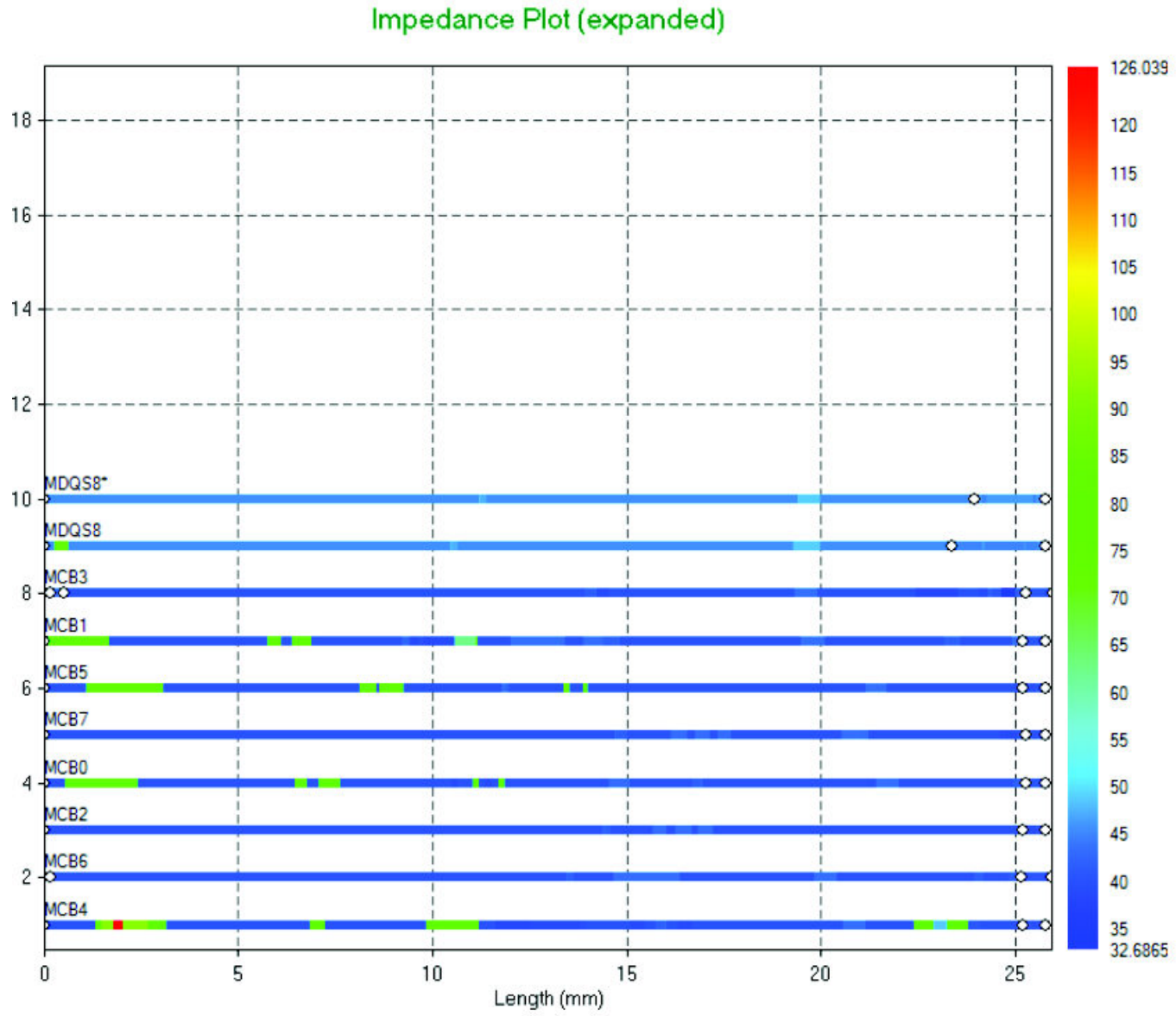




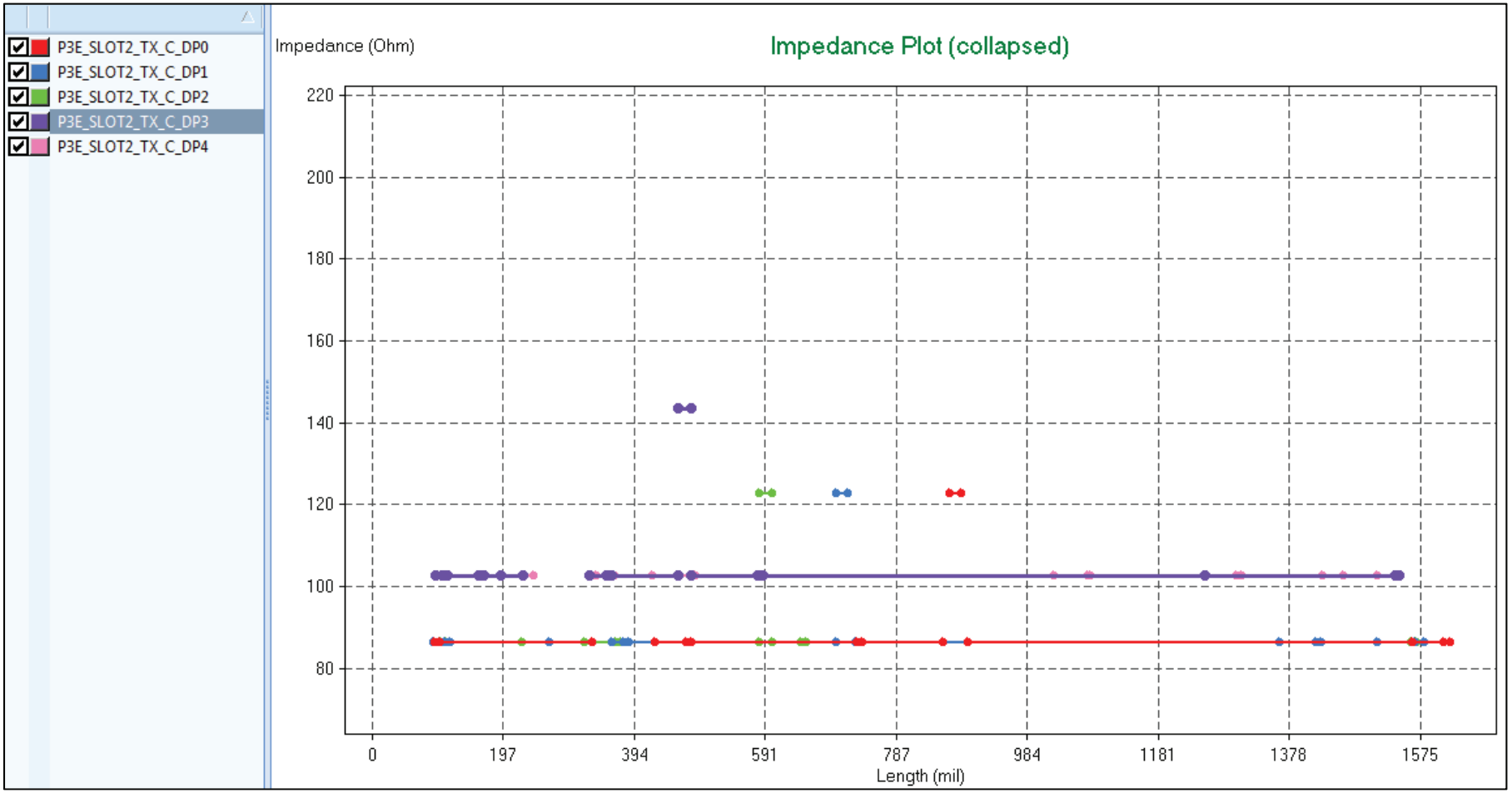




ERC result view



ERC result view



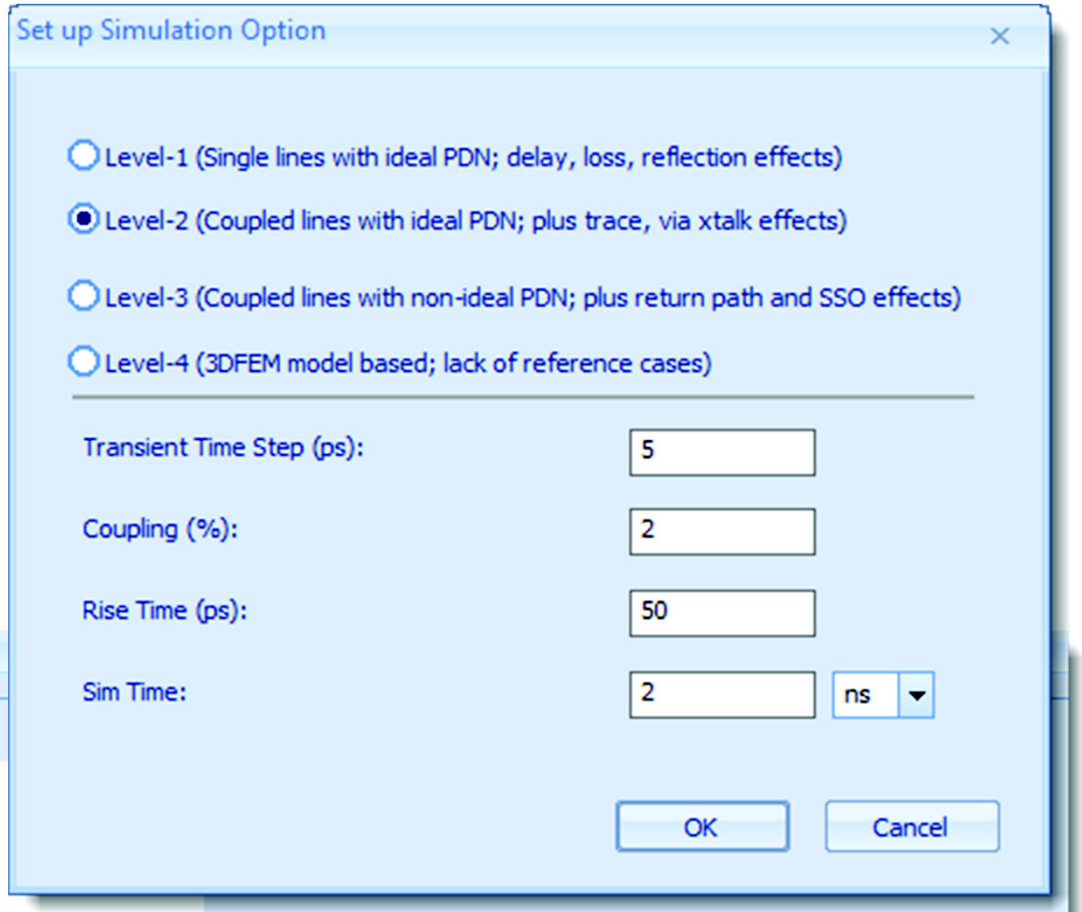
What is SRC?

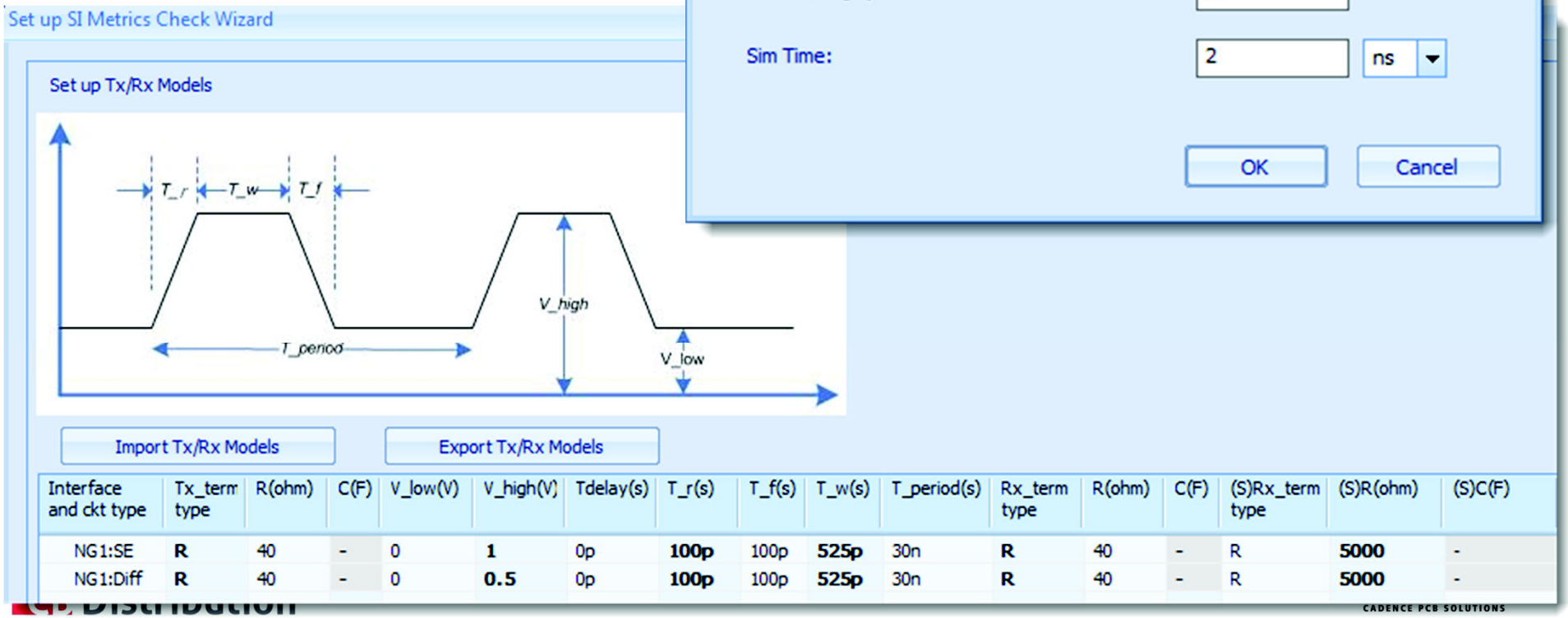
- Simulation Rule Check
- SRC is a net-level view in time-domain of impact due to ERC violations measured in mv&ps.
- No device model needed (no IBIS, Spice)
  - Setup considering termination impedance, data rate (pulse width, rise/fall time) and amplitude
  - Results with Tx/Rx/NEXT/FEXT waveforms, SI performance metrics
  - Organized to easy SI performance interpretation along with ERC
- Practical for board level check (setup, simulation, report)

< 2min ~ 20min auto

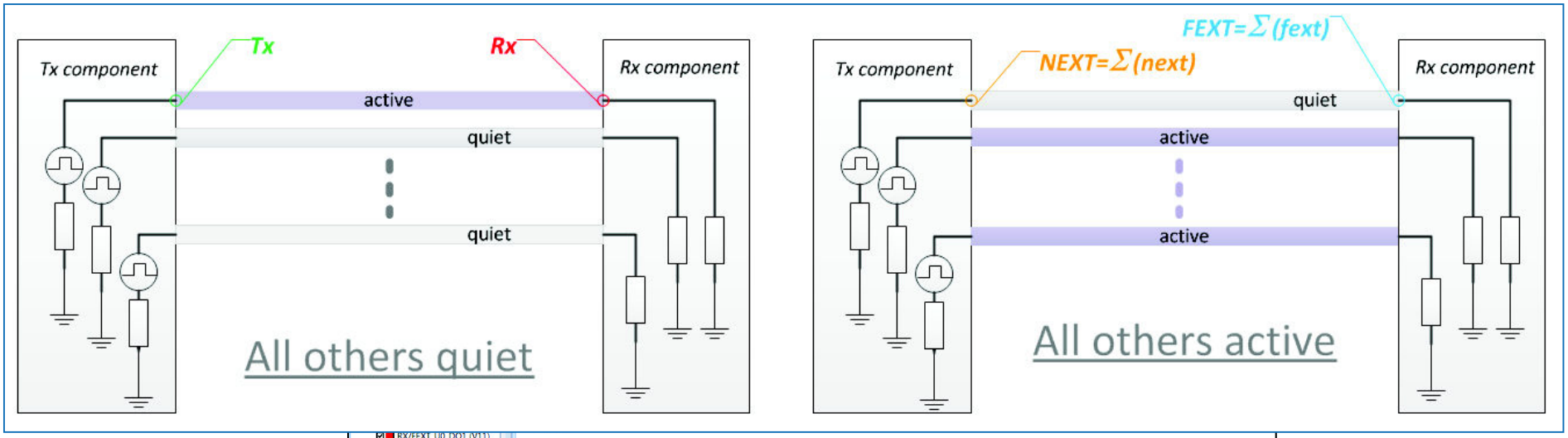
SRC setup

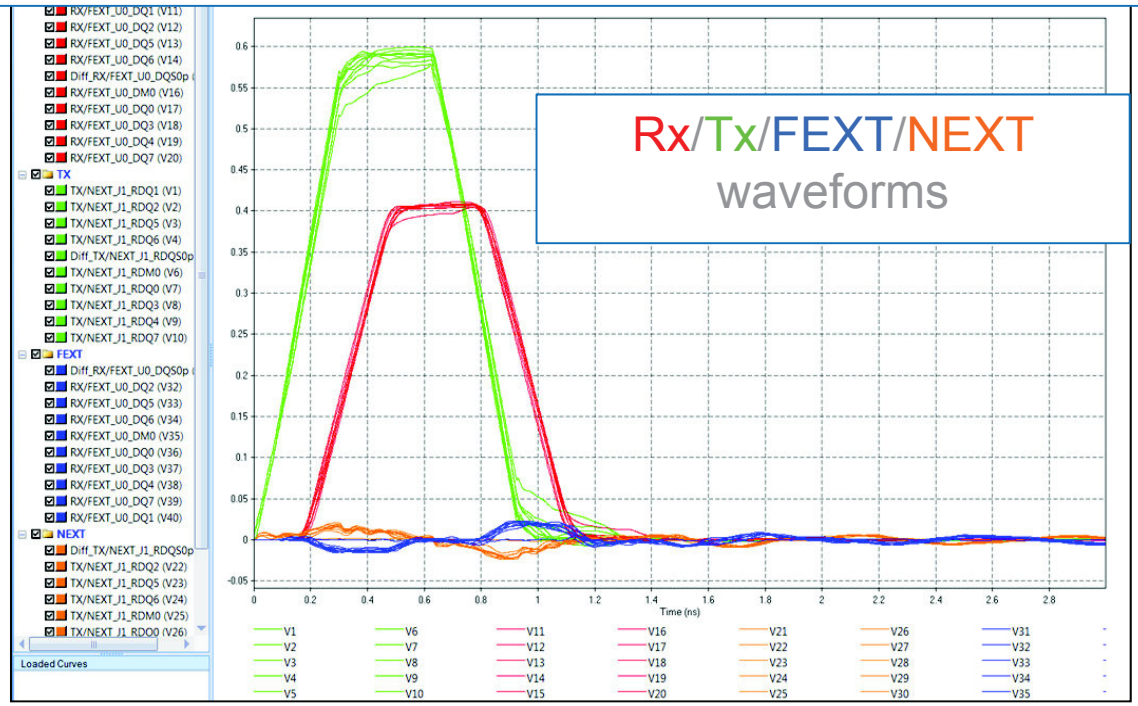
- Device models not needed
- Voltage pulse as stimulus, users can specify
  - Amplitude
  - Data rate (pulse width, rise/fall time)
  - Termination





Time-domain waveforms





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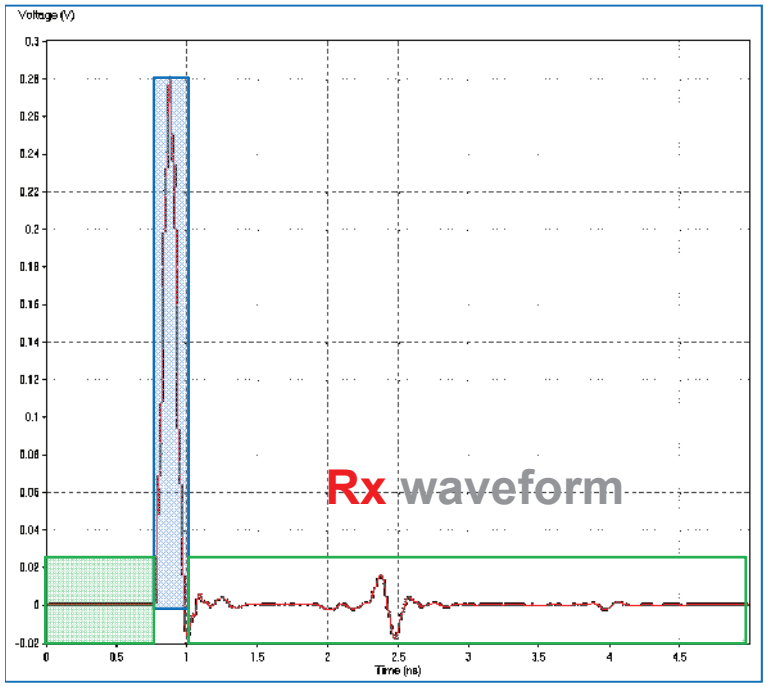


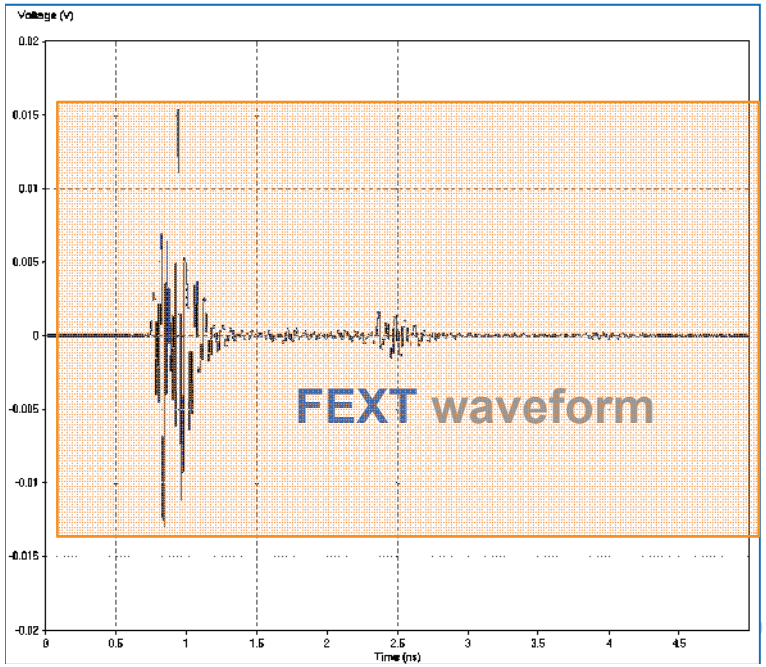
SRC – SI metrics check

- SI metrics are defined using magnitudes of Rx and FEXT

$$Int\_sig = \int_{t_1}^{t_2} |Rx(t)|dt$$

$$Int\_ISI = \int_{0}^{t_1} |Rx(t)|dt + \int_{t_2}^{t_{max}} |Rx(t)|dt$$

$$Int\_xtk = \sum \int_{0}^{t_{max}} |fext_i(t)|dt$$



$$SN\_difference = (Int\_sig) - (Int\_ISI) - (Int\_xtk)$$

$$SN\_ratio = \frac{Int\_sig}{(Int\_ISI) + (Int\_xtk)}$$

Where

t_1 and t_2 are starting and ending time for the received pulse (1 UI width)

t_{max} is maximum time-domain simulation time

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SRC – SI metrics check

Net-level performance ranking

- Ranking by SI Metrics

Net name	INT_Sig (V*ps)	INT_ISI (V*ps)	INT_XTK (V*ps)	SN_difference (V*ps)	SN_ratio
DQ19	287.97	22.96	3.7	261.31	10.8029
DQ17	288.15	22.79	3.12	262.24	11.1223

- Ranking by xtalk levels

Net name	NEXT Vmax (mv)	NEXT Vmin (mv)	NEXT pk-2-pk (mv)	FEXT Vmax (mv)	FEXT Vmin (mv)	FEXT pk-2-pk (mv)
DQ9	19	-18	37	14	-15	29
DQ12	17	-15	32	16	-16	32
DQ8	2	-2	5	3	-3	6

ERC and SRC HTML Report

cadence

OrCAD Sigrity ERC SI Performance Metrics Check Report

Date: 12:11 July 30, 2014

this is a tutorial

1 General information

1.1 Spd file name and location

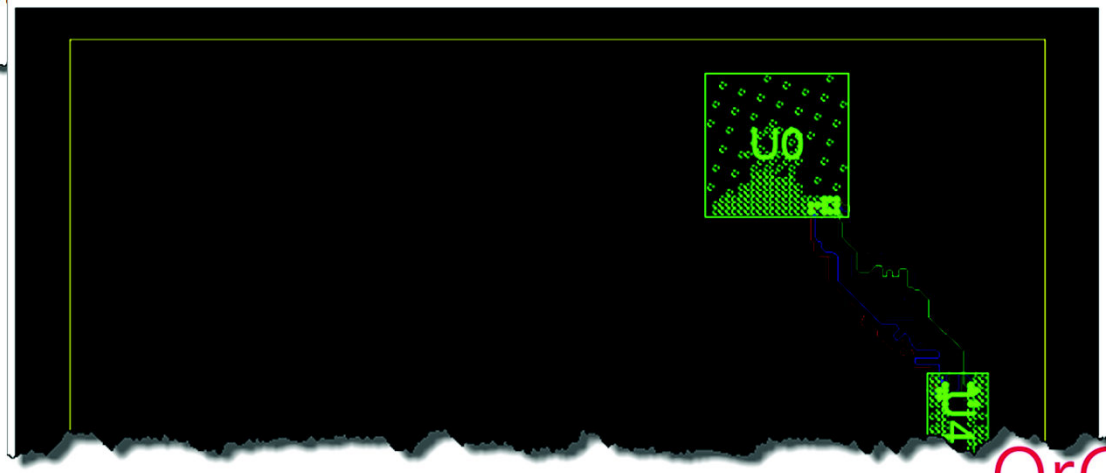
SPDGEN version: 14.0.2.07112

File names and locations:

- Layout spd file
  - D:/Backup/3_Training/SIM/Movie/SIM_movie_sim/
- SI metrics check results file
  - D:/Backup/3_Training/SIM/Movie/SIM_movie_sim/

2.2 Net group Data_U0_U4

Tx component	Net name	Passive component	Net name	Passive component	Net name	Rx component (active)	Rx component (standby)	Rx component (notpopulated)	FIR filter	Pulse ca
U0	DQ29	-	-	-	-	U4	-	Not populated		v-edg
U0	DQ31	-	-	-	-	U4	-	Not populated		v-edg
U0	DQ30	-	-	-	-	U4	-	Not populated		v-edg
U0	DQS3_N	-	-	-	-	U4	-	Not populated	no	v-max
U0	DQS3_P	-	-	-	-	U4	-	Not populated	no	v-max
U0	DQ28	-	-	-	-	U4	-	Not populated		v-edg
U0	DQ26	-	-	-	-	U4	-	Not populated		v-edg
U0	DQ24	-	-	-	-	U4	-	Not populated		v-edg
U0	DQ27	-	-	-	-	U4	-	Not populated		v-edg
U0	DM3	-	-	-	-	U4	-	Not populated		v-edg
U0	DQ25	-	-	-	-	U4	-	Not populated		v-edg



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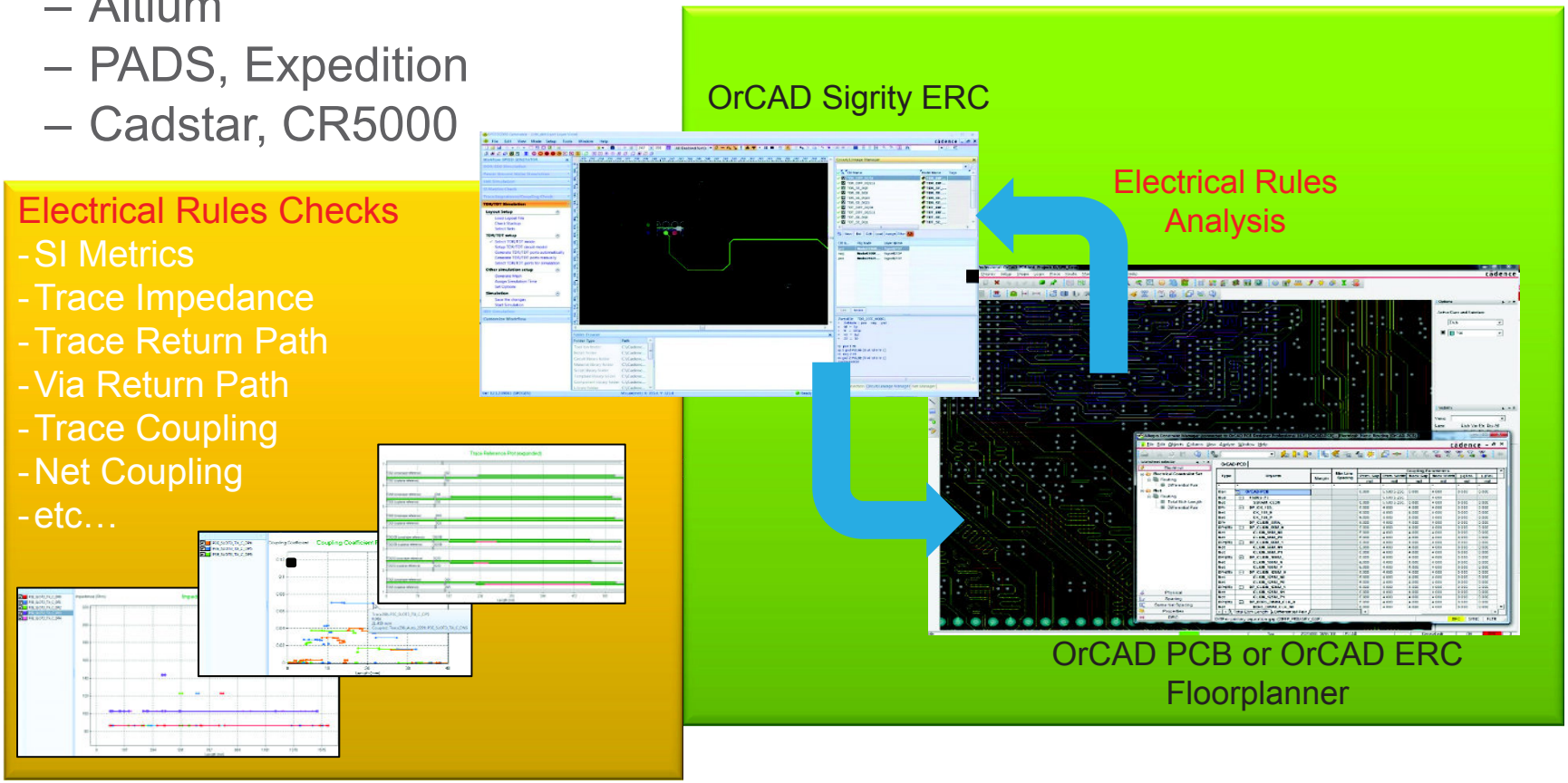
OrCAD Sigrity ERC

- Sigrity quality SI electrical checking for the PCB designer.
- Other PCB formats supported.
  - Altium
  - PADS, Expedition
  - Cadstar, CR5000



Agenda

- The gap between DRC and SI simulations
- Introducing new PCB checks
- Applications and examples
- Conclusion

ERC/SRC applications (1)

- To screen board and to identify worst case for further analysis
- To investigate SI impact of design rule violations and trade-offs

Problems found in layout design

What is the impact in mV & ps?

To fix, or not to fix?

If layout problems can be quantified using mv/ps, it is much easier to decide

ERC/SRC applications (2)

- To find out how to fix SI problems shown in SRC simulation

How to fix them in layout

If problems can be root caused in layout, it is much easier to fix

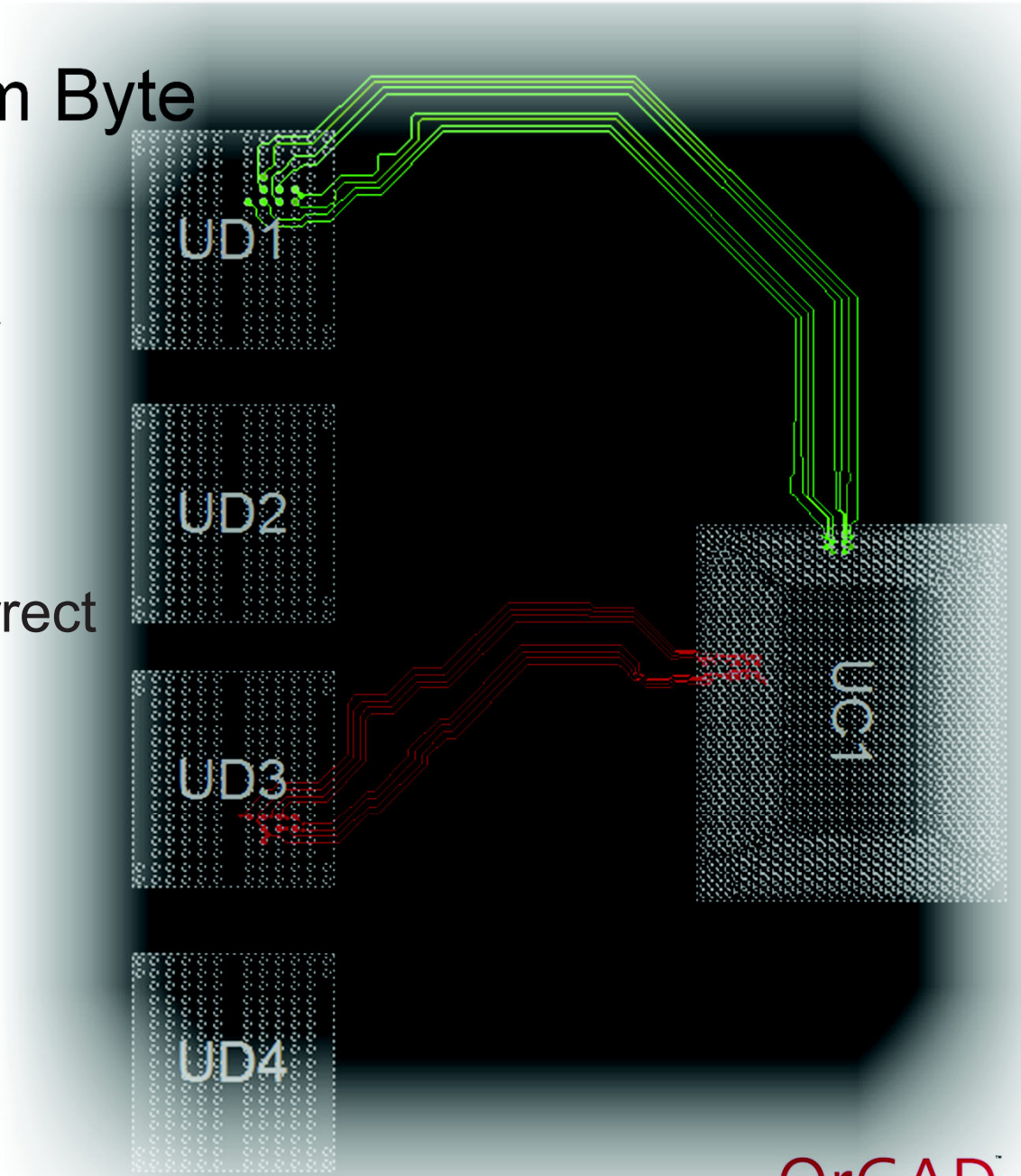
How to fix it in layout?

Problems found in simulation results

ERC/SRC Example

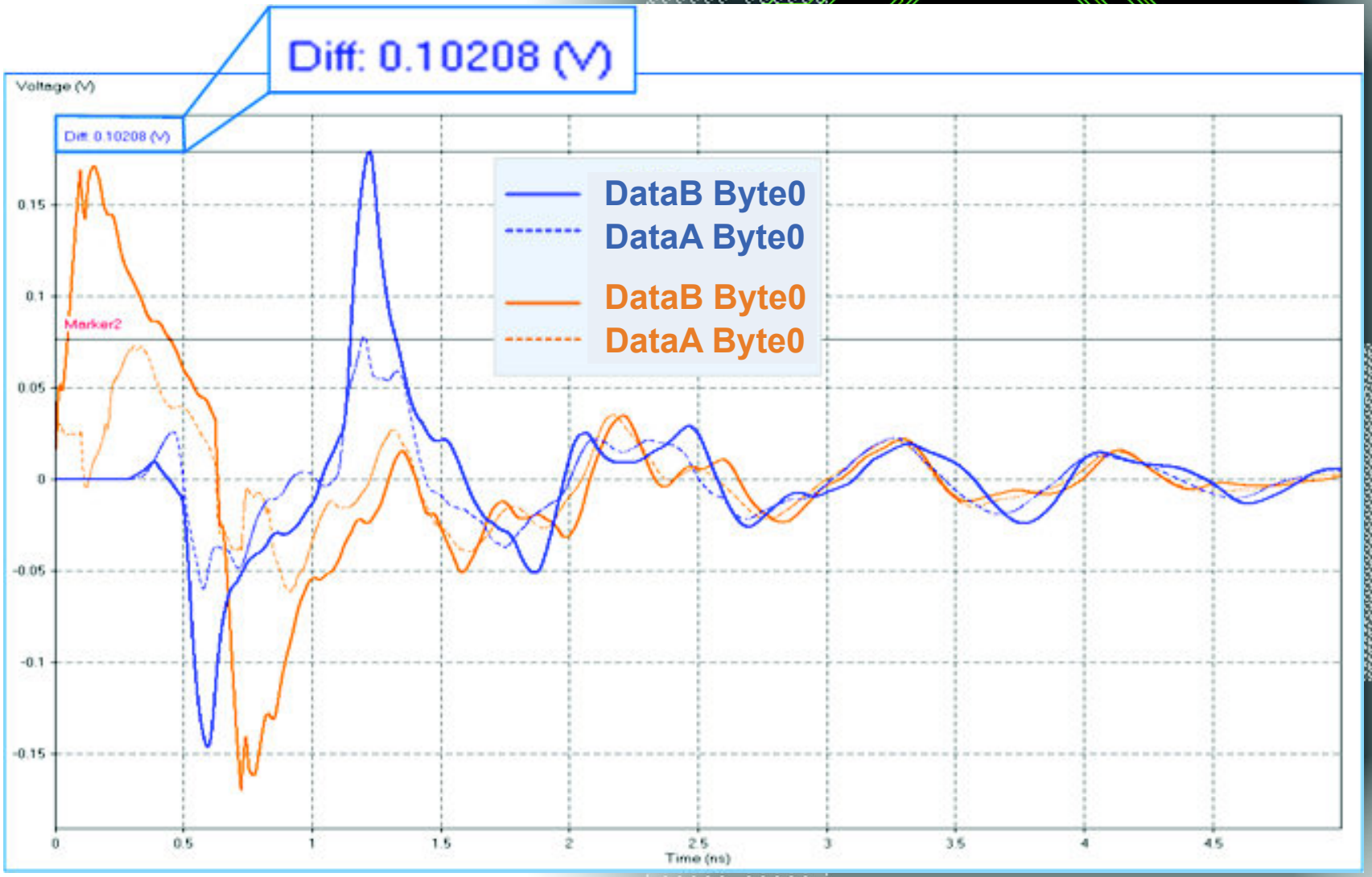
SRC – the problem Byte

- One of the problems identified is Byte0 for channel B has large xtalk
- PCB routing
- Design was DRC correct



ERC/SRC Example

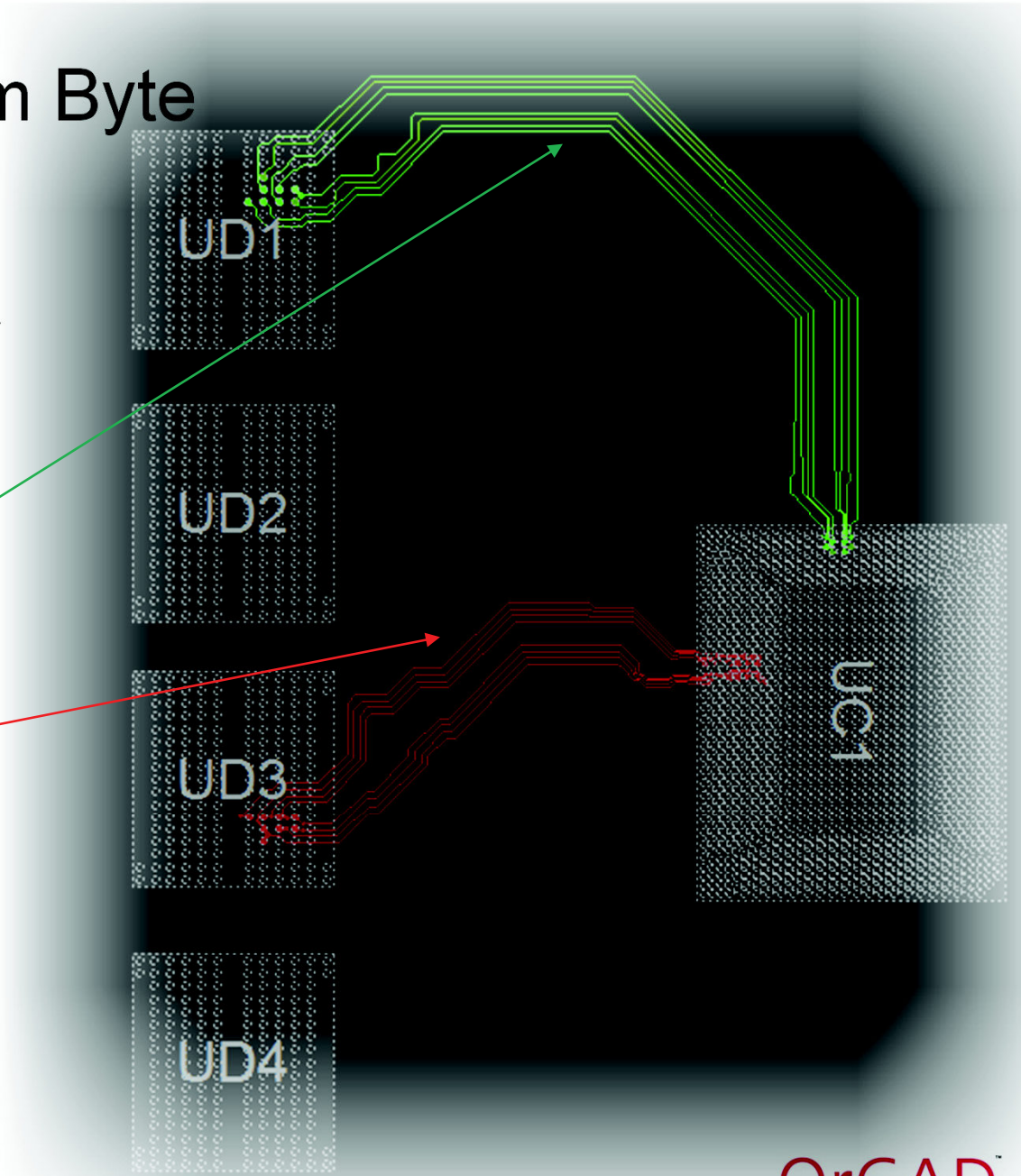
SRC – the problem Byte



ERC/SRC Example

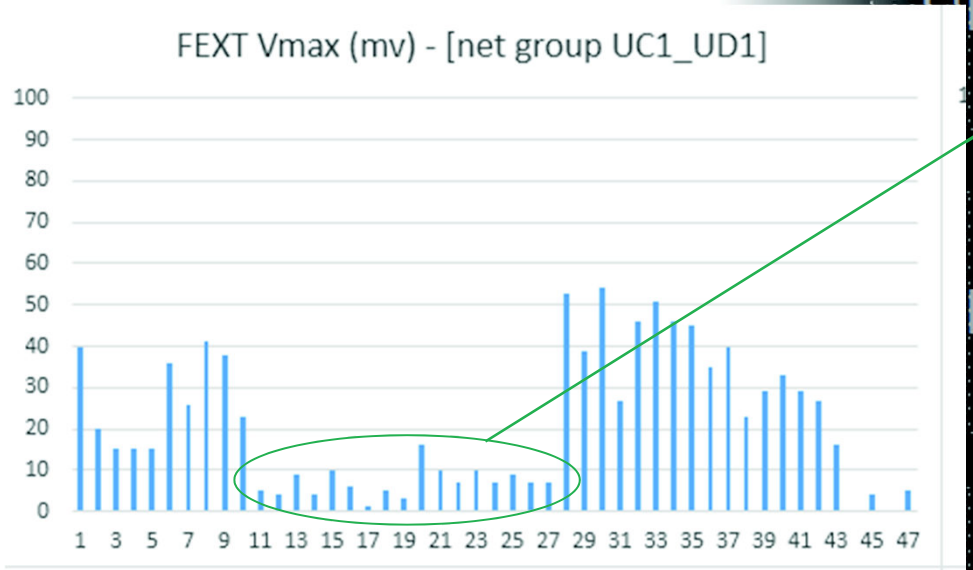
SRC – the problem Byte

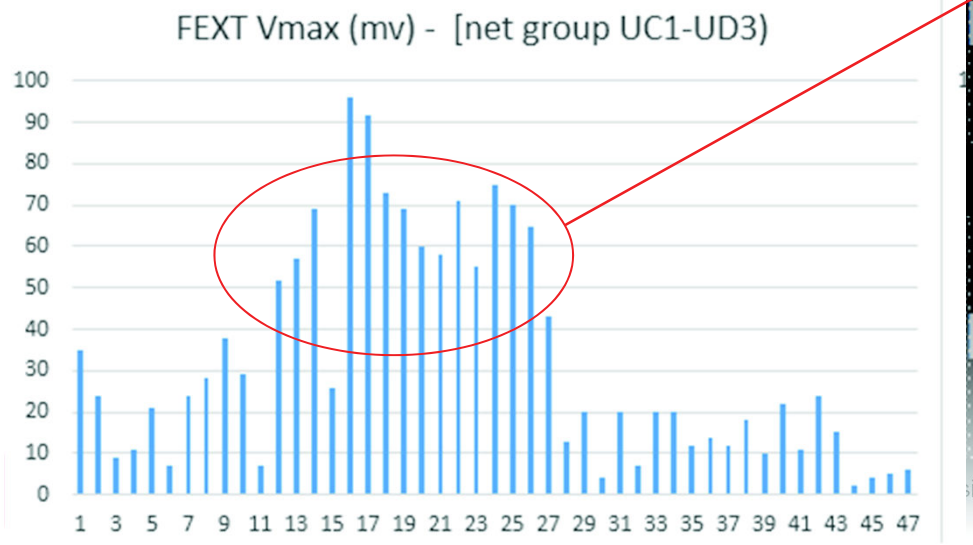
- One of the problems identified is Byte0 for channel B has large xtalk
- PCB routing
  - Data_A Byte0
    - Smaller FEXTs
  - Data_B Byte0
    - Larger FEXTs

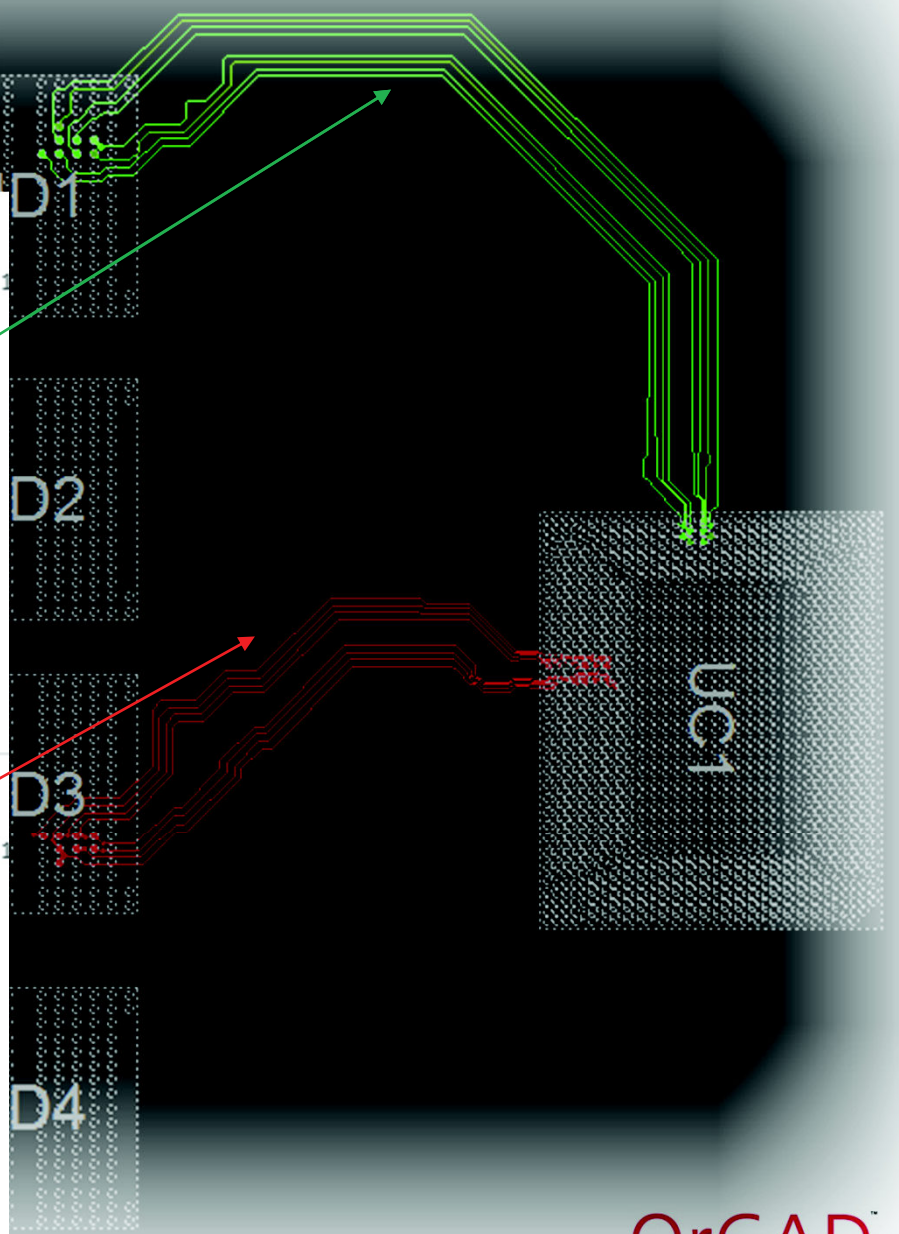


ERC/SRC Example

SRC – the problem Byte







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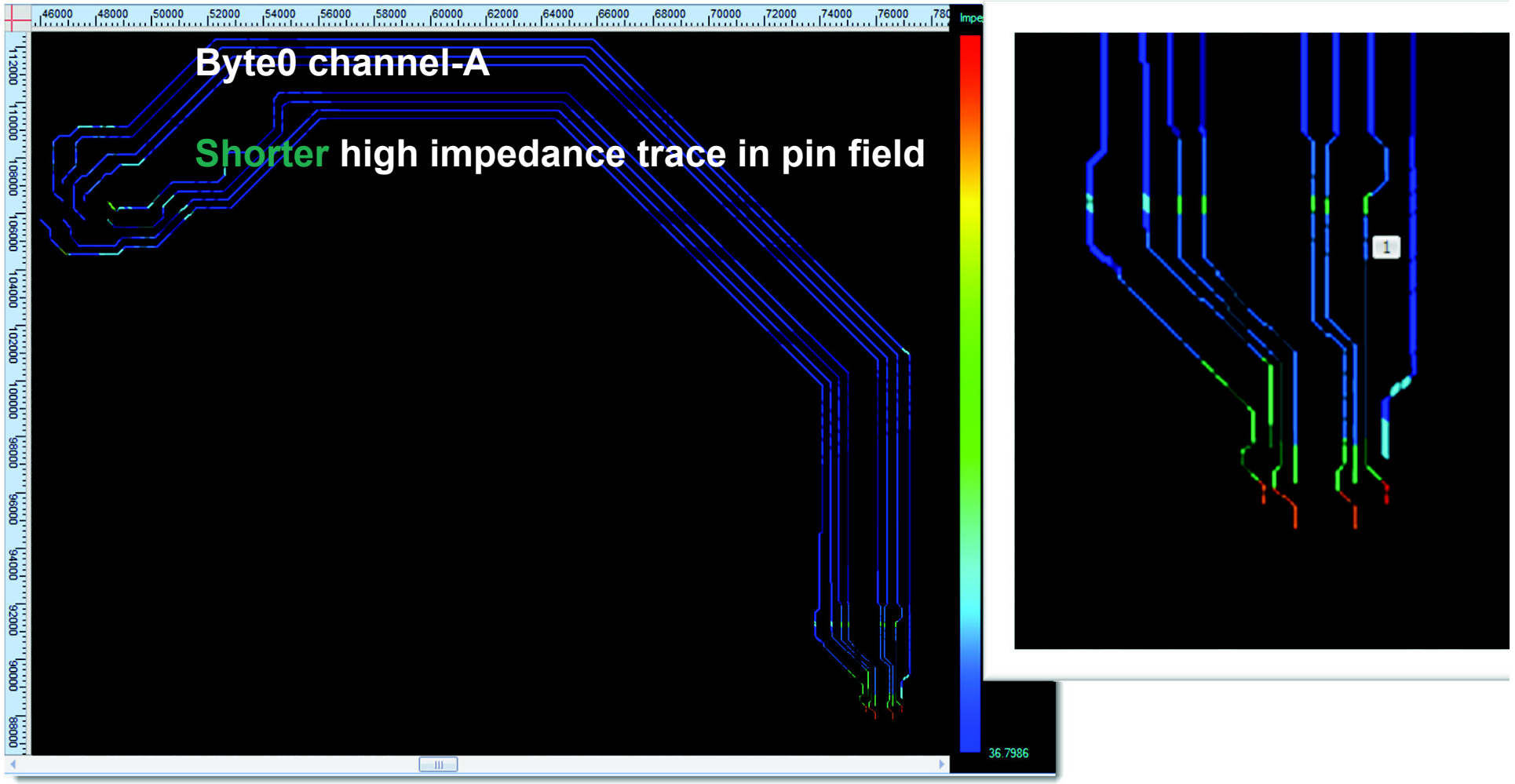
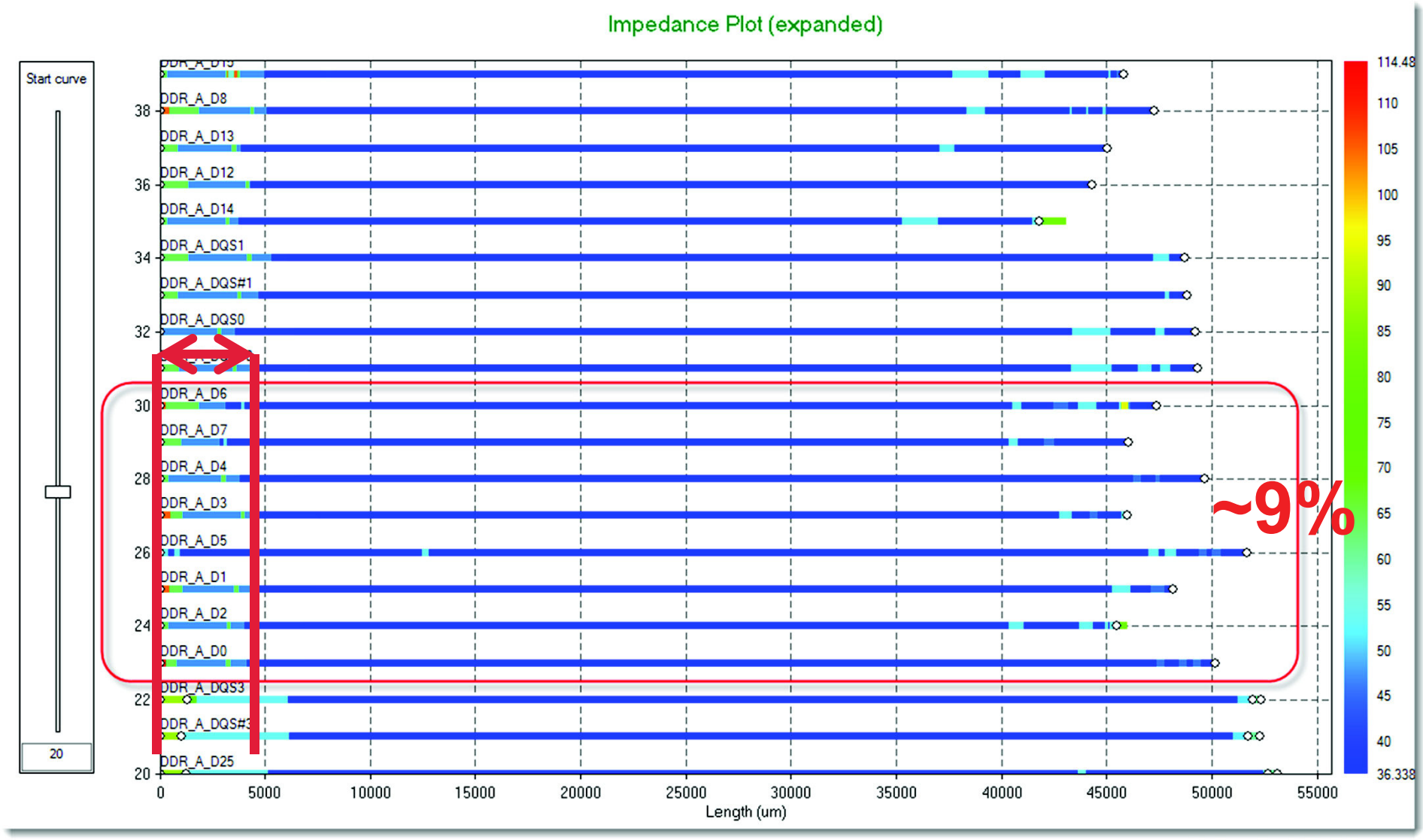
ERC/SRC Example

ERC – DataA Byte0 impedance



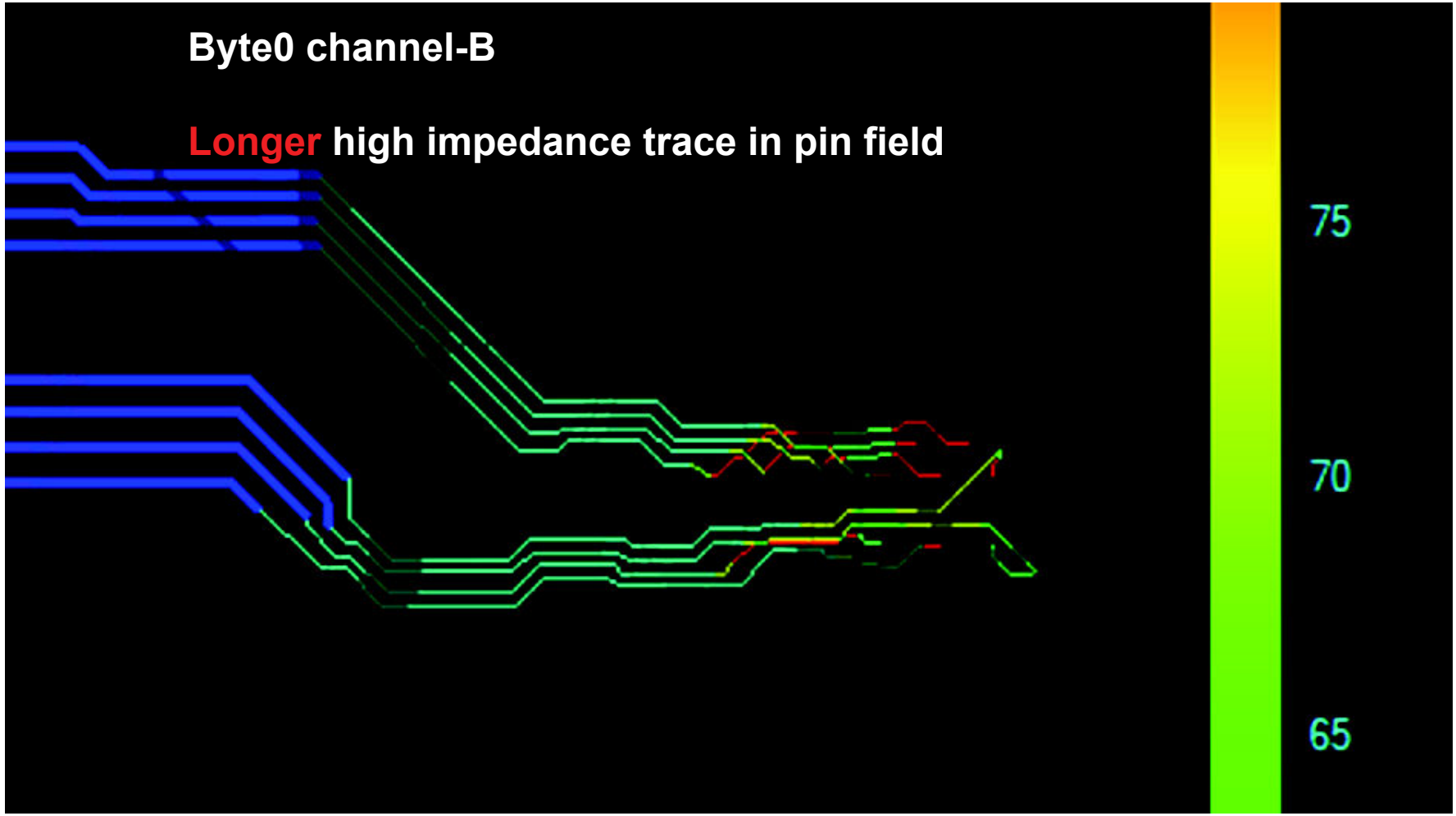
ERC/SRC Example

ERC – DataA Byte0 impedance



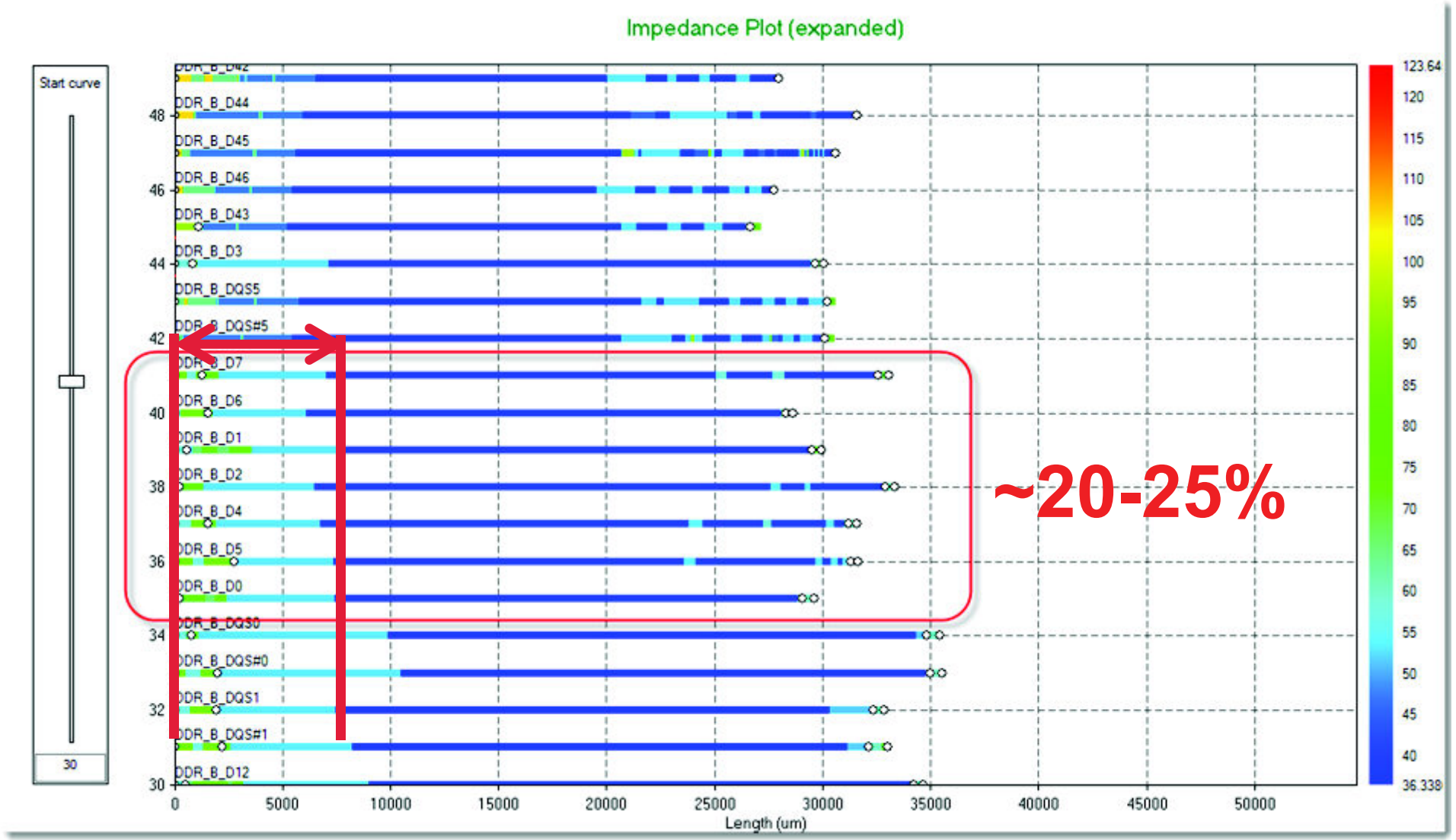
ERC/SRC Example

ERC – DataB Byte0 impedance



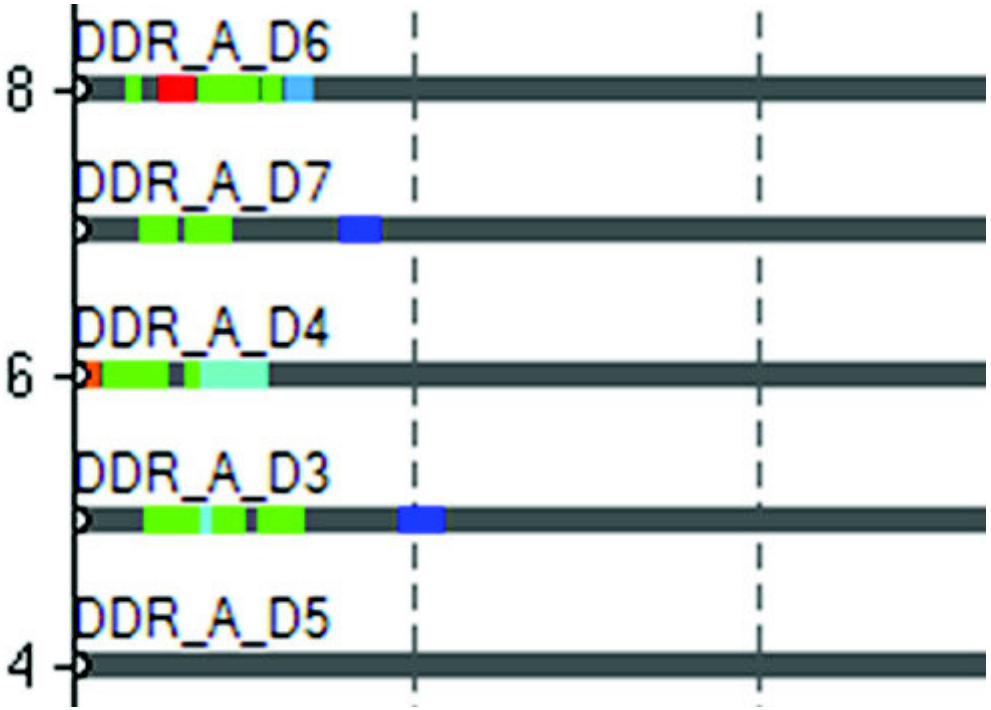
ERC/SRC Example

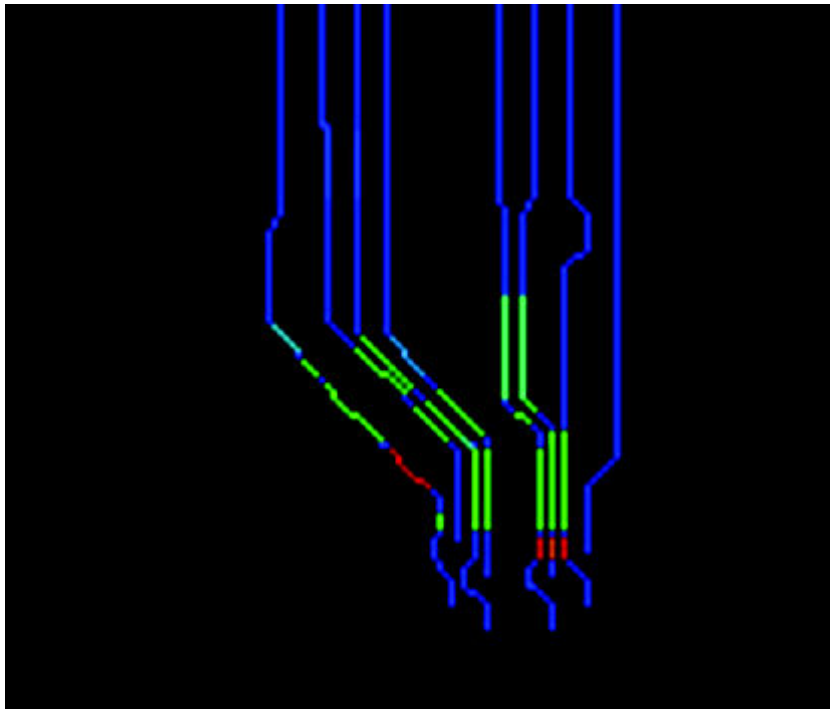
ERC – DataB Byte0 impedance



ERC/SRC Example

ERC – DataA Byte0 coupling

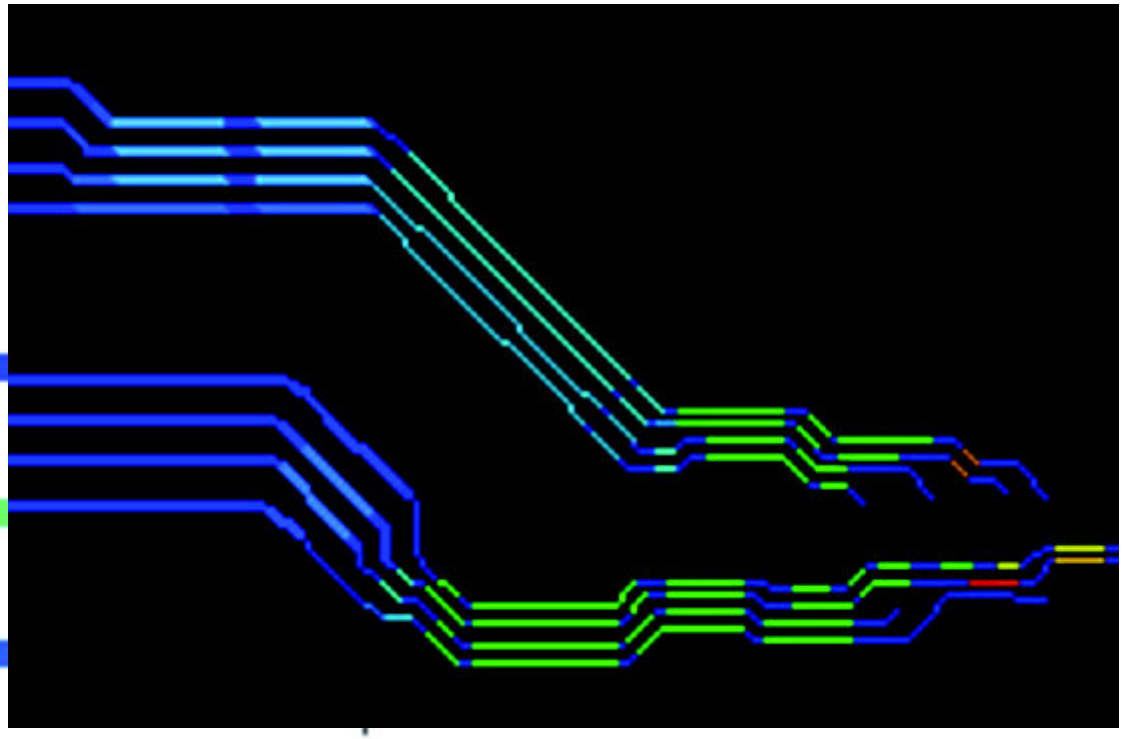




ERC/SRC Example

ERC – DataB Byte0 coupling

- Higher trace coupling in pin field



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ERC/SRC Example

ERC – # of vias

- DataA Byte0: 2 vias
- DataB Byte0: 4 vias

Net name	No. of vias
DDR_A_D0	2
DDR_A_D1	2
DDR_A_D2	2
DDR_A_D3	2
DDR_A_D4	2
DDR_A_D5	2
DDR_A_D6	2
DDR_A_D7	2

Net name	No. of vias
DDR_B_D0	4
DDR_B_D1	4
DDR_B_D2	4
DDR_B_D3	4
DDR_B_D4	4
DDR_B_D5	4
DDR_B_D6	4
DDR_B_D7	4

ERC/SRC Example

How to fix

To reduce the xtalk level of channel B Byte0, user can consider one, or combination, of the following improvements:

- Impedance
  - reduce the impedance discontinuities in pin field routing length
- Coupling
  - reduce the coupling in pin field routing
- Via
  - reduce via number

Agenda

- The gap between DRC and SI simulations
- ERC/SRC filling the gap
- ERC/SRC applications and examples
- Conclusion

Conclusion

- DRC's alone cannot validate the interconnects electrical characteristics
  - Examples: signals crossing split or different reference planes causing impedance changes.
- ERC/SRC are signal quality checks at the individual, segment-level in the geometry domain.
  - ERC: Shows why low performance happened and how to fix it .
  - SRC: Shows what happened and its effect on performance.
- ERC/SRC designed for use by the PCB layout designer, NOT the signal integrity (SI) expert.
- SI Expert can focus on other complex problems.