#### **Quadra Solutions Limited**

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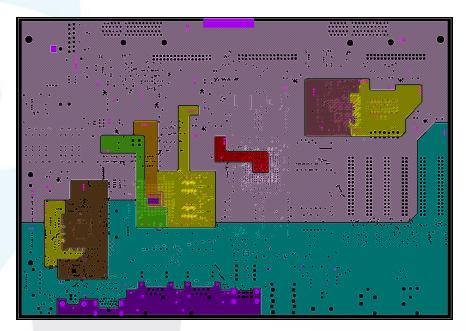
#### Why Should I Care About Power Integrity?

**D&E 2015** Presenter: Bob Sadowski Applications Consultant



## **Power Integrity**

- > What Is Power Integrity?
- > Why Should I Care?
- > When Should I Be Concerned?
- > What Can I Do About It?







## What Is Power Integrity?



> Power Integrity provides a measure of the quality of the power distribution network

- > Minimise the DC voltage drop across power planes
- > Minimise the propagation of IC switching currents by optimising decoupling capacitance
- > .. and thereby reduce EMC emissions





# Why Should I Care?

#### > Technology trends

#### THE DIFFERENCES BETWEEN SIGNAL INTEGRITY AND POWER INTEGRITY

	Signal integrity	Power integrity
Became mainstream	~20 years ago	~5 years ago
Analysis based on	Transmission lines	Transmission planes
Typical impedance targets	~50 Ω	~mΩ
Subsets of analysis	Signal quality Timing Crosstalk	dc drop Decoupling Noise
Models needed	IBIS, Spice	Capacitors with parasitics
PCB design changes driven	Trace width Trace length Trace spacing	Amount of metal to carry current Number, value, mounting of caps Power/ground plane pairs, stackup





### **A Real-World Example**

#### A Xilinx FPGA with 456 pins:

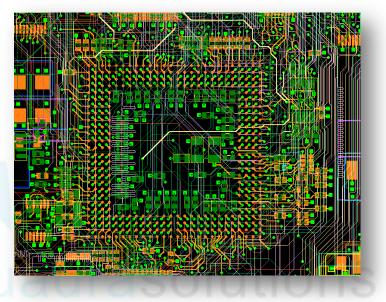
- Controls a video grabber card
- 64 bits can switch in parallel
  - worst case, rise time of 750ps
- Output pin drives into a load of 15pf

The maximum switching current can be determined by:

$$\Delta I = n * C * \frac{Vcc}{t} = 64 * 15 pf \frac{2.5V}{0.75ns} = 3.2A$$

Based on this maximum current, the impedance limit to guarantee a ripple of less than 125 mV (5% of 2.5 V) :

$$Z = \frac{U}{I} = \frac{125mV}{3.2A} = 0.039\Omega$$





# **Should I be Concerned?**

- > If you need high performance or reliability
  - > High utilisation
  - > Thermal stability
- > If you are using leading edge controllers ...
  - > CPU, FPGA, DSP
    - > Low voltage
    - > High power
    - > Fast edge rates
    - > Low noise margins
    - > Requiring multiple power distribution networks
- > Yes!





#### An Example .....



- 1 or 2 failures (hang-ups, black screen) per month
- Shutdown and reboot required



# What are Typical PI Symptoms?

> Physical

- > CPU/FPGA/memory device failure
- > PCB Vias or Tracks go open circuit (fuses!)
- > Blistering, delamination or discolouration of PCB
- > ...

> ...

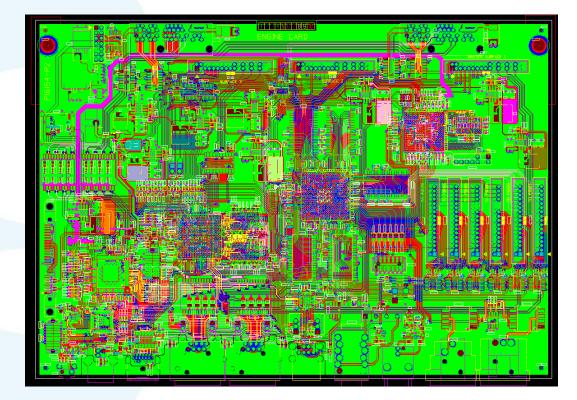
- > Electronic
  - > CPU reset on high utilisation address of utions
  - > Memory fails or data corruption
  - > Analog circuits go out of spec.





## What Can I Do About It?

- > Simulate your PCB Design!
  - > Run Power Integrity Analysis on the virtual layout before manufacture and assembly of an expensive prototype









## What Data is Required?

- > Fully Defined Layer Stack
  - > Electrical
  - > Construction
  - > Materials
- > Classified Power nets
  - > Reference voltages
  - > Series interconnects
    - > Resistor
    - > Inductor
    - > FET

- Part data
  - > Values
  - IBIS models (useful)
  - > Pin types
  - > Power requirements
- Net data > Type
  - > Bus, Data, Analog, etc
  - Target frequency





#### **Layer Stack & Power Nets**

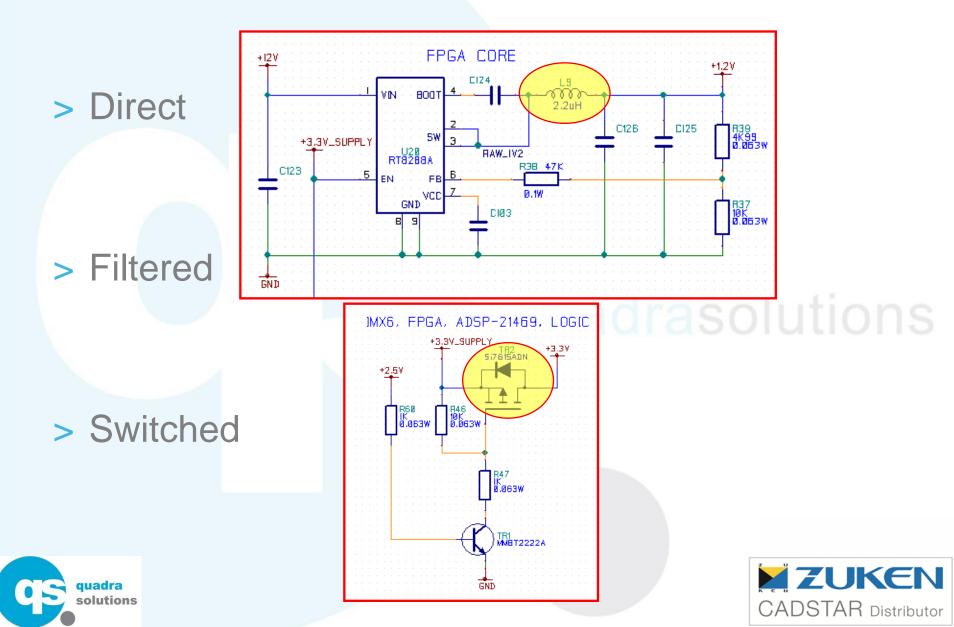
			Layers	;					rou	ting bias O	( 0 10	→ , , ,	swap layers
Name	Туре	Physical Layer	Thickness (Thou)	Material	Embedding	Referen	ce Plane	Sub Type	Physical	Board Thickness =	9.32th		
p Resist Construction	Construction		0.01	Resist	None			(None)					
p Elec	Electrical	1	1.40	Copper Foil	Above			(None)					Top Elec (1.40)
reg1	Construction		4.00	Prepreg	None			(None)					Prepreg1
ver 2	Electrical	2	1.40	Copper Foil	Above		/	(None)					Layer 2 (1.40)
re1	Construction		4.00	FR4	None			(None)					Core1 (4.00)
yer 3	Electrical	3	1.40	Copper Foil	Below			(None)					Layer 3 (1.40)
epreg2	Construction		7.10	Prepreg	None			(None)					Layer 5 (1.40)
er 4	Electrical	4		Copper Foil	Above			(None)					
re2	Construction		4.00	FR4	None			(None)					Prepreg2
er 5	Electrical	5	1.40	Copper Foil	Below		/	(None)					
preg3	Construction		7.10	Prepreg	None			(None)			_		Layer 4 (1.40)
ver 6	Electrical	6	1.40	Copper Foil	Above		/	(None)					
e3	Construction		4.00	FR4	None			(None)					Core2 (4.00)
ver 7	Electrical	7	1.40	Copper Foil	Below			(None)					Layer 5 (1.40)
preg4	Construction		7.10	Prepreg	None			(None)			ŭ		
er 8	Electrical	8	1.40	Copper Foil	Above			(None)			g		D2
e4	Construction		4.00	FR4	None			(None)			h		Prepreg3
er 9	Electrical	9	1.40	Copper Foil	Below		/	(None)					
preg5	Construction		4.00	Prepreg	None			(None)			н		Layer 6 (1.40)
ttom Elec	Electrical	10		Copper Foil	Below			(None)			0		Core3 (4.00)
ttom Resist Constructio	Construction		0.01	Resist	None			(None)					Cores (4.00)
													Layer 7 (1.40) Prepreg4
													Layer 8 (1.40)
													Core4 (4.00)
													Layer 9 (1.40)
													Prepreg5 Bottom Elec
									Blind Via U	navailable 🔹			
									Buried Via U	aavailablo –	Сору	,	
									Duneu vid	available *	copy		

E Power Nets 🗄 🕇 +1.2V ± +1.8V 🗄 🕇 +1.8VA 🗄 🕇 +1V05 🗄 🕆 🕇 +2.5V ± +3.3V . +3.3V SUPPLY E CHASSIS E TODR3 VCC 🗄 🕆 DDR3\_VREF 🗄 🕂 🕇 GND E TRAW\_1V0 🗄 🕆 RAW 1V2 . RAW\_1V05 🗄 🕆 RAW 1V8 🗄 🕆 RAW\_1V35 🗄 🕆 🕇 RAW\_2V5 🗄 🕆 RAW\_3V3 🗄 🕆 🕇 RAW 5V . RAW\_DDR3\_1V5 🗄 🕂 🕇 USB 5V E VDDARM\_CAP 🗄 🕆 VDDHIGH\_CAP 🗄 🕆 VDDPU\_CAP E VDDSOC CAP 🗄 🕆 🕇 VDDUSB\_CAP





#### **Power Interconnects**



#### **Part Data**

> Active

<mark>quadra</mark> solutions

- > Models
  - > Device
  - > Pin types

#### All Constraints | Crosstalk | Distortion | Impedance | Delay | Skew | Misc | Modeling | Lengthening | Multi-board ⊕... ■ U25 🗄 🛯 U26 No. of Pins Capacitance Inductance DeviceType Vendor Device Source Part Name Resistance 🗄 🕲 U27 (Ohm) (pF) (nH) 🕀 🔟 U28 🛱 U28-625 HH C1 2 100N 10% 16V B 100000.0 🛱 U28-626 HH C2 2 100N 10% 16V B 100000.0 🖁 U28-A2 -IF C18 2 22U 20% 25V J 22000000.0 🛱 U28-A3 -IF C19 2 100N 10% 50V C 100000.0 上 U28-A4 W [1 2 FB 600R C 1.0 PWR U28-A5 ·W 12 2 ASPI-7318-3R3M 1.0 U28-A6 10 L3 2 ASPI-8040S-2R2N 2.2 🛱 U28-A7 -୦୦° L4 2 ASPI-8040S-1R5N 1.5 ± U28-A8 4# R1 2 100R1%B 100.0 U28-A9 -W- R2 2 100R1%B 100.0 U28-A10 -Wh R31 2 10K1%B 10000.0 🛱 U28-A11 Wh R32 2 10K1%B 10000.0 🛱 U28-A12 U19 UK RT8288A Project 9 RT8288AZSP Digital IC 🛱 U28-A14 1 U26 MICRON MT41K256M16HA Site 98 MT41K256M16HA-125 Digital IC 🛱 U28-A15 U28 MCIMX6Q5EYM10AC UK iMX6Q Site 626 Digital IC

Discrete

> Value



#### **Part Classification**

- > Identify power sources
- Nominal power
  consumption per
  supply rail per
  device

Comp	onent Ne	t Supply	Via Type	DC Via	Power Bus								
	🐔 Name	4R.	Part N	ame		<b>A</b> 1	Туре	<b>@</b> 0	Value (Ω pF nH)	I Active	🔹 # Pins		Heatsin
U12	U12	RT8288AZSP /	RT8288A			IC					9	no	
U13	U13	RT8288AZSP /	RT8288A			IC					9	no	
U14	U14	RT8288AZSP /	RT8288A			IC					9	no	
U15	U15	MT48LC16M1	5M16A2TG	IC					54	no			
U16	U16	MT48LC16M1	6A2P-7E / N	/T48LC16	5M16A2TG	IC					54	no	
U17	U17	ADSP-21469 /		IC					326	no			
U18	U18	MT47H64M16	16HR	IC					86	no			
U19	U19	RT8288AZSP /		IC					g	no			
U20	U20	RT8288AZSP / RT8288A				IC					9	no	
U21	U21	RT8288AZSP / RT8288A				IC					9	no	
U22	U22	DS90C385AMT									56	no	
U23	U23	XC6SLX100-2FGG484C / SPARTAN-6									486	no	
U24	U24	MT48LC16M16A2P-7E / MT48LC16M16A2TG									54	no	
U25	U25	RT8288AZSP / RT8288A									9	no	
1126	1126	MT41K256M16H4-125 / MT41K256M16H4								<u> </u>	QR	-	
•	1	-[]											
Pin	Power Bus												
	🔩 Name	» Power Bus	Source	e 🛷 Po	wer Consur	nptio	n ØR	Packa	age Resistance (Ω)	Min IC	Voltage /)		
U11	U11	+12V_GND	20			5.00	00		0.001		12.000		
	U11	+1.8V_GND	yes						0.001		1.800		
U11	1112	+12V GND		_		8.00	00		0.001		12.000		
U11 U12	012		ho										
U12		+3.3V_GND	yes						0.001		3.300		
U12 U12	U12	+3.3V_GND		]		5.00	00		0.001		3.300 5.000		
U12 U12 U14	U12 U14	+3.3V_GND	yes	]			00						
U12 U12 U14 U14	U12 U14 U14	+3.3V_GND	yes no	]					0.001		5.000		
	U12 U14 U14 U14 U15	+3.3V_GND \$14188_GND +1.35V_GND	yes no yes			5.00	00		0.001		5.000 1.350		
U12 U12 U14 U14 U15	U12 U14 U14 U15 U18	+3.3V_GND \$14188_GND +1.35V_GND +3.3V_GND	yes no yes no			5.00	00		0.001 0.001 0.001		5.000 1.350 3.300		

2.000

+12V GND

+1V0 GND

yes

U25 U25

U25 U25



12.000

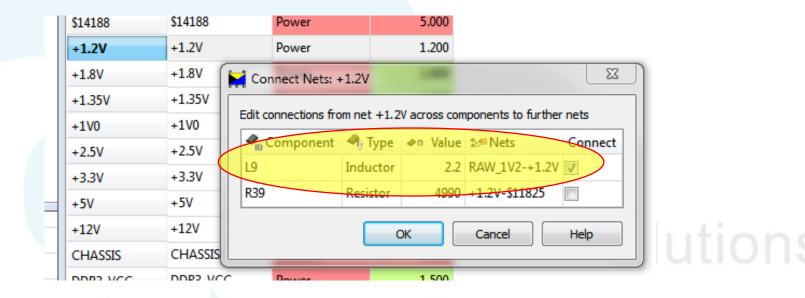
1.000

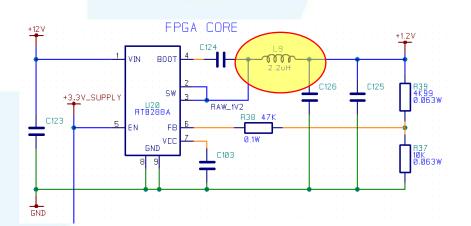
0.001

0.001



#### **Power Interconnects**









# **Net Classification**

- > Signal Type
  - > Bus
  - > Data
  - > Clock
  - > Control
  - > Etc.

#### > Target clock frequency

Classification							
Component Ne	t Supply Via Type	DC Via Powe	er Bus				
	🕬 Name	🐅 Signal Type	\$%. I/O	<sup>≵≪</sup> (MHz)	4		
DRAM3_A13	DRAM3_A13	Bus	no	100.000			
DRAM3_A14	DRAM3_A14	Bus	no	100.000			
DRAM3_CAS_B	DRAM3_CAS_B	Control	no	100.000			
DRAM3_CS0_B	DRAM3_CS0_B	Control	no	100.000			
DRAM3_D0	DRAM3_D0	Data	no	233.000			
DRAM3_D1	DRAM3_D1	Data	no	233.000			
DRAM3_D2	DRAM3_D2	Data	no	233.000			
DRAM3_D3	DRAM3_D3	Data	no	233.000			
DRAM3_D4	DRAM3_D4	Data	no	233.000			
DRAM3_D5	DRAM3_D5	Data	no	233.000			





#### A short overview of PIA ..





# **Key Benefits**

- > Power Integrity Advance enables analysis and exploration of the power distribution network at the 'virtual prototype' design stage, before you commit to a costly physical prototype
- > Helps you reduce project timescale and cost to bring your product to market faster and improve quality and reliability





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