

**Real-Timeness and System Integrity
on a Asymmetric Multi Processing configuration**

D&E Event – **November 2nd**
Relator: Manuele Papais
Sales & Marketing Manager

DAVE Embedded Systems



DAVE Embedded Systems' HEADQUARTER
Via Talponedo, 29/A
33080 Porcia, Italy

DAVE Embedded Systems' BRANCH OFFICE
Maximilianstrasse, 13
80539 München, Germany



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Sales Offices:

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- Belgium / The Netherlands
 - **Telerex B.V.**
- Now opening: Japan

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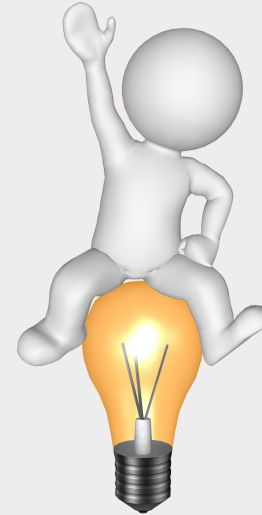
Concept and Design
of Embedded Systems

DAVE Embedded Systems



Concept and Design
of Embedded Systems

Solutions Provider



Supporting and Promoting
Customer Ideas and
Concepts
from Scratch to Business



Products Portfolio

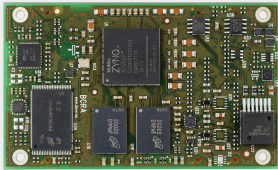
Products Portfolio

System On Modules

Texas Instruments
SITARA, DA VINCI

NXP i.MX6...

XILINX Zynq



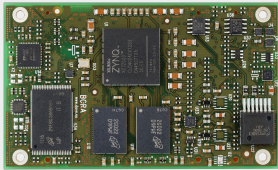
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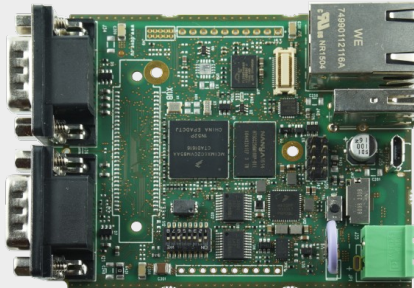
XILINX Zynq



Single Board Computers

Wall mount

DIN Bar mount



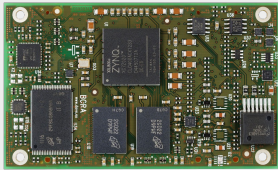
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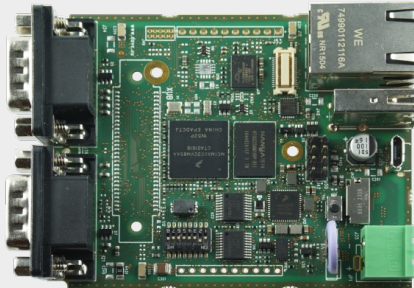
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Customized Solutions

Based on customer
requirements

Based on existing
proven solutions



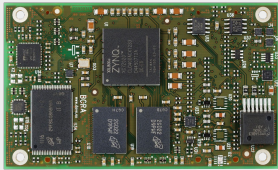
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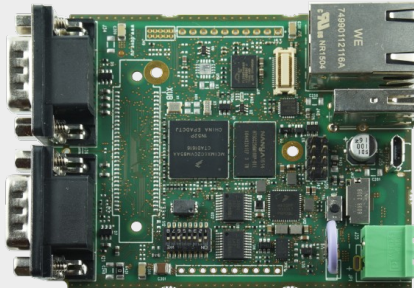
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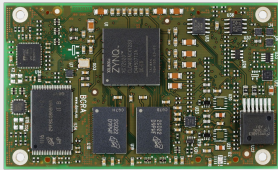
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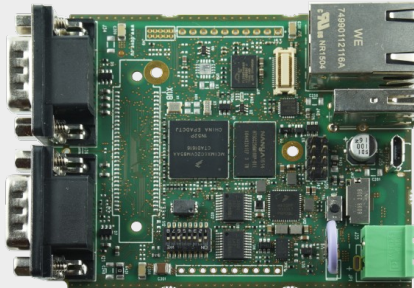
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Linux Kernel & Drivers

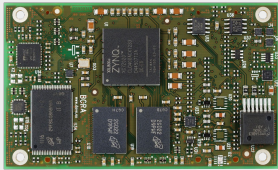
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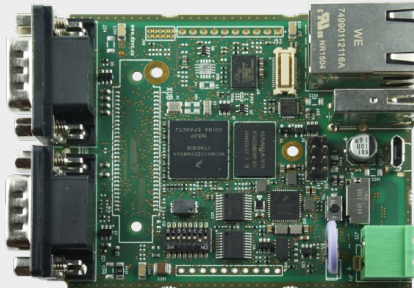
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Android BSP

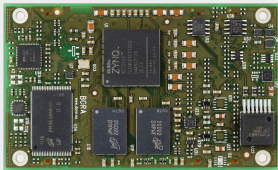
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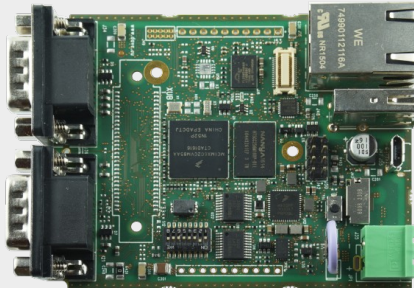
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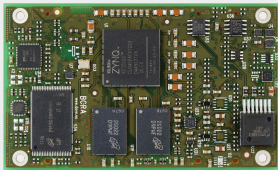
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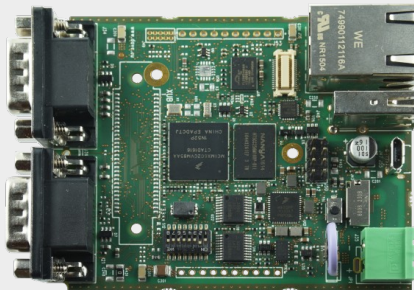
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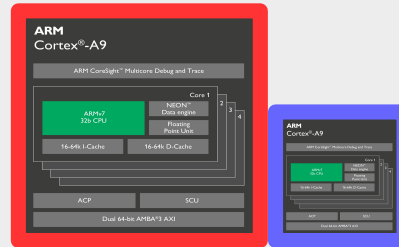
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FPGA Vivado Project
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RTOS
Integration/examples

AMP Asymmetric Multi Processing

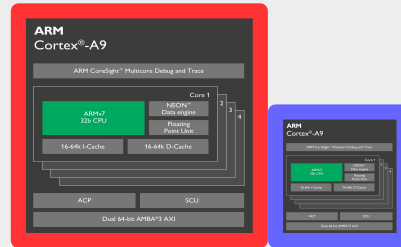
BIG - LITTLE



- NXP Vybrid
- TI AM335
- ...

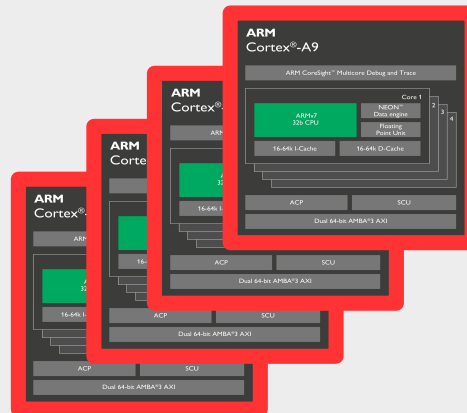
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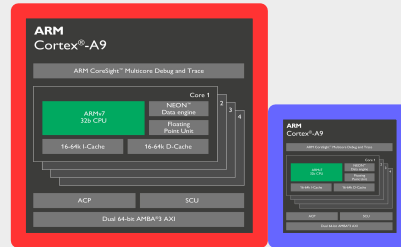
SIMMETRIC



- NXP i.MX6 DUAL Lite
- NXP i.MX6 DUAL
- NXP i.MX6 QUAD
- ...

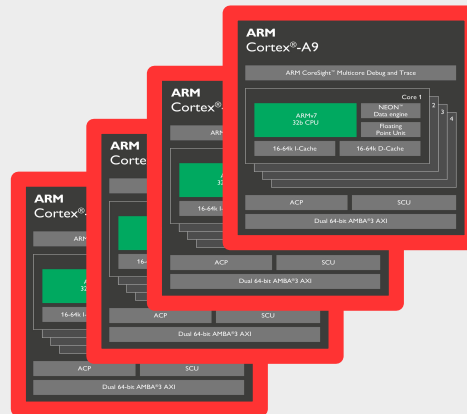
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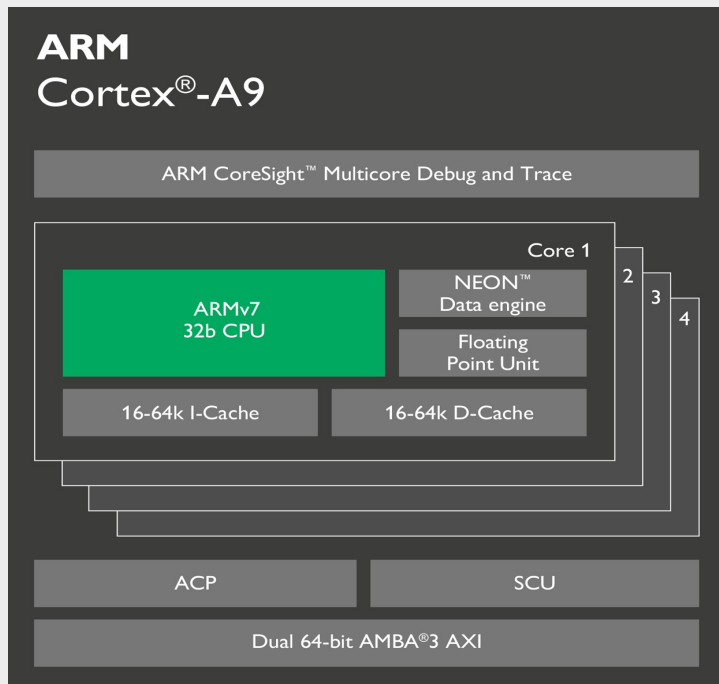
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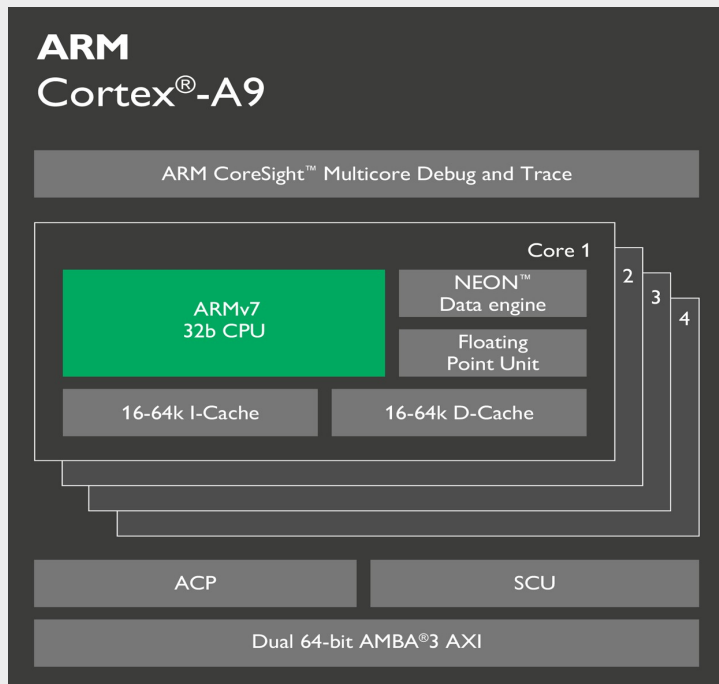
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Cortex-A9 architecture

- Multicore platform approach
- Low power architecture
- Industrial grade proof

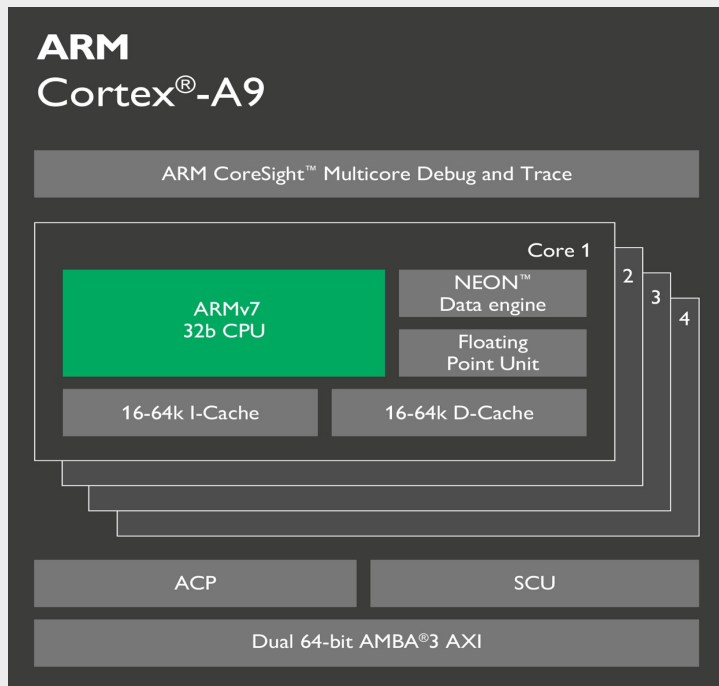


Cortex-A9 architecture



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- **TrustZone IP integrated**

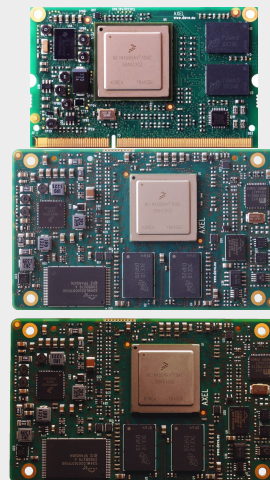
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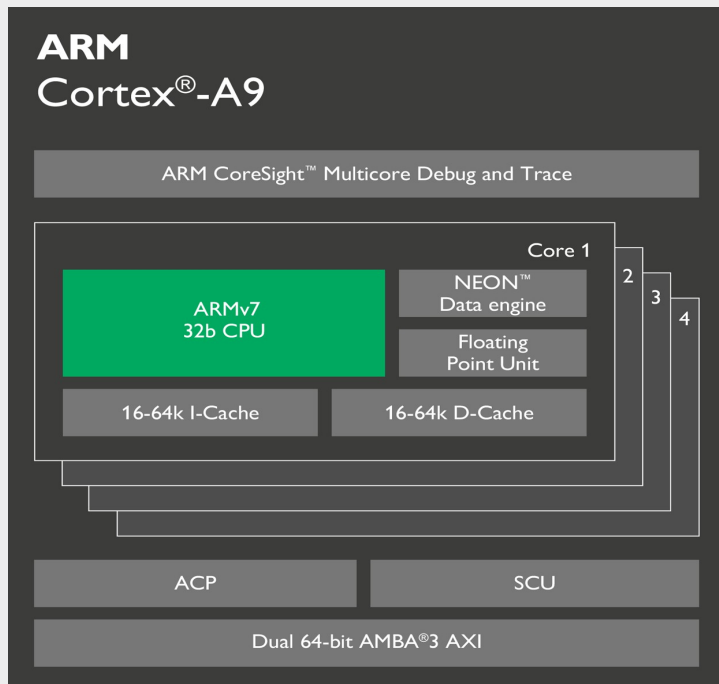
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NXP i.MX6



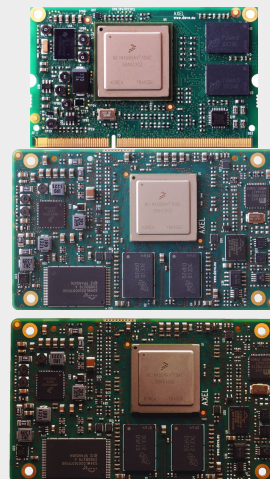
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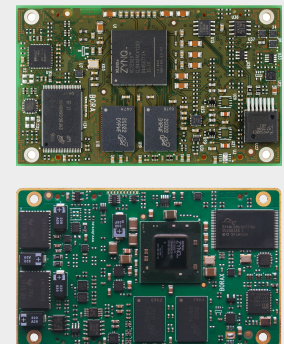
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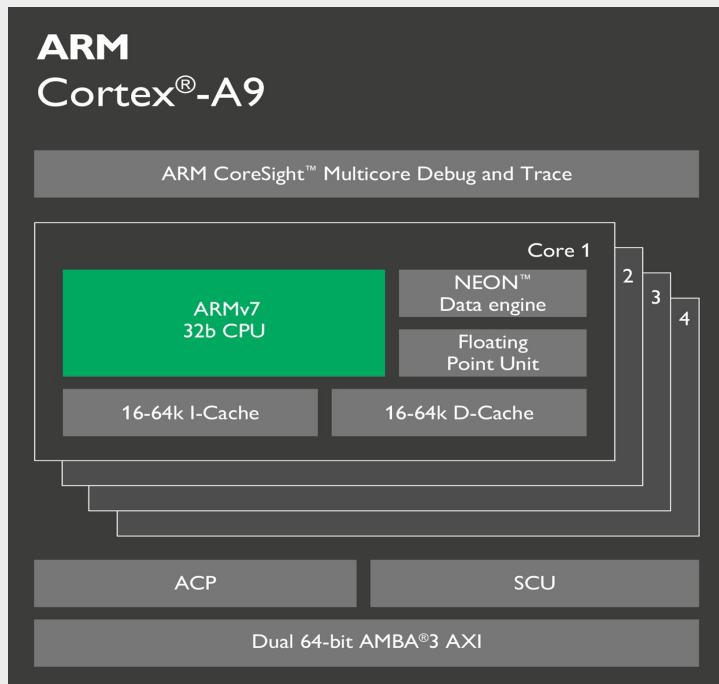
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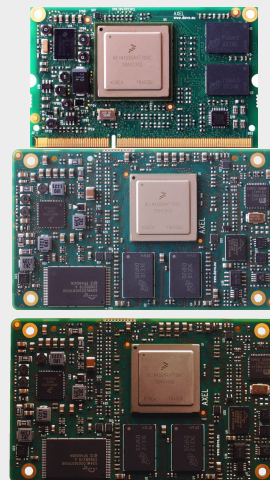
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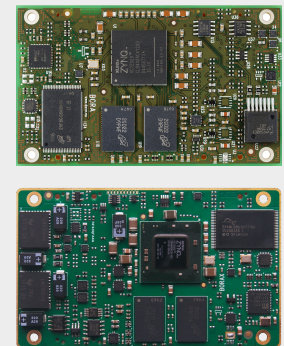
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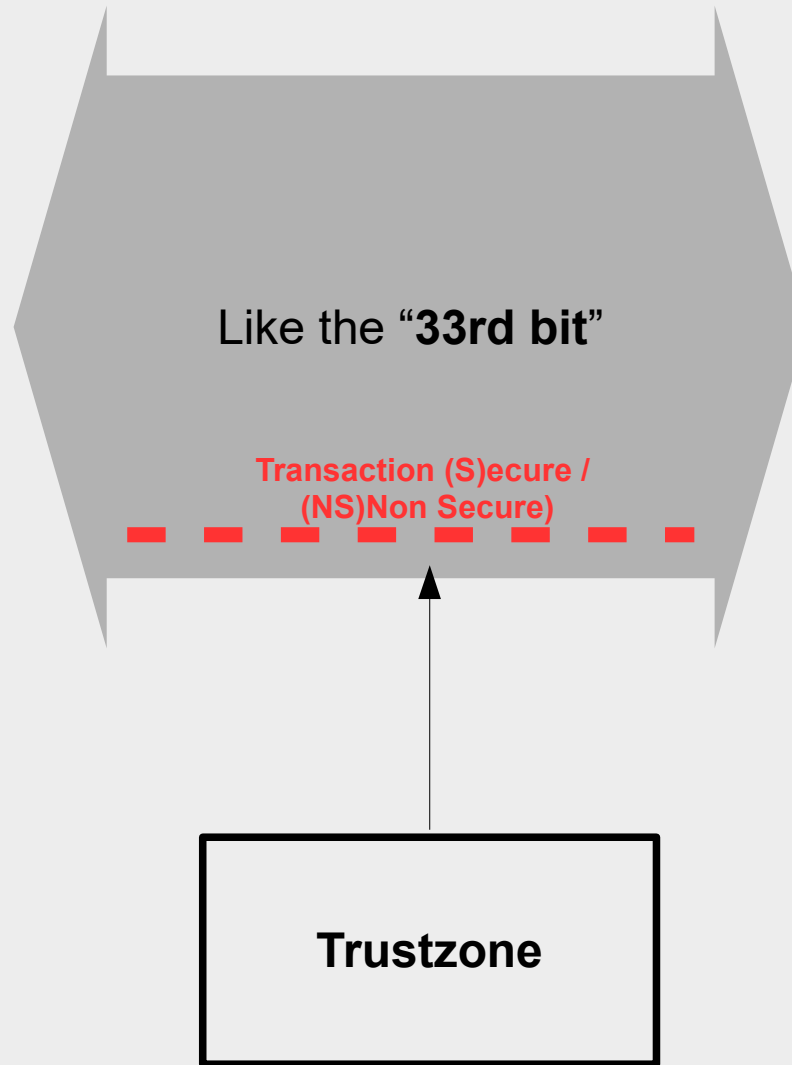
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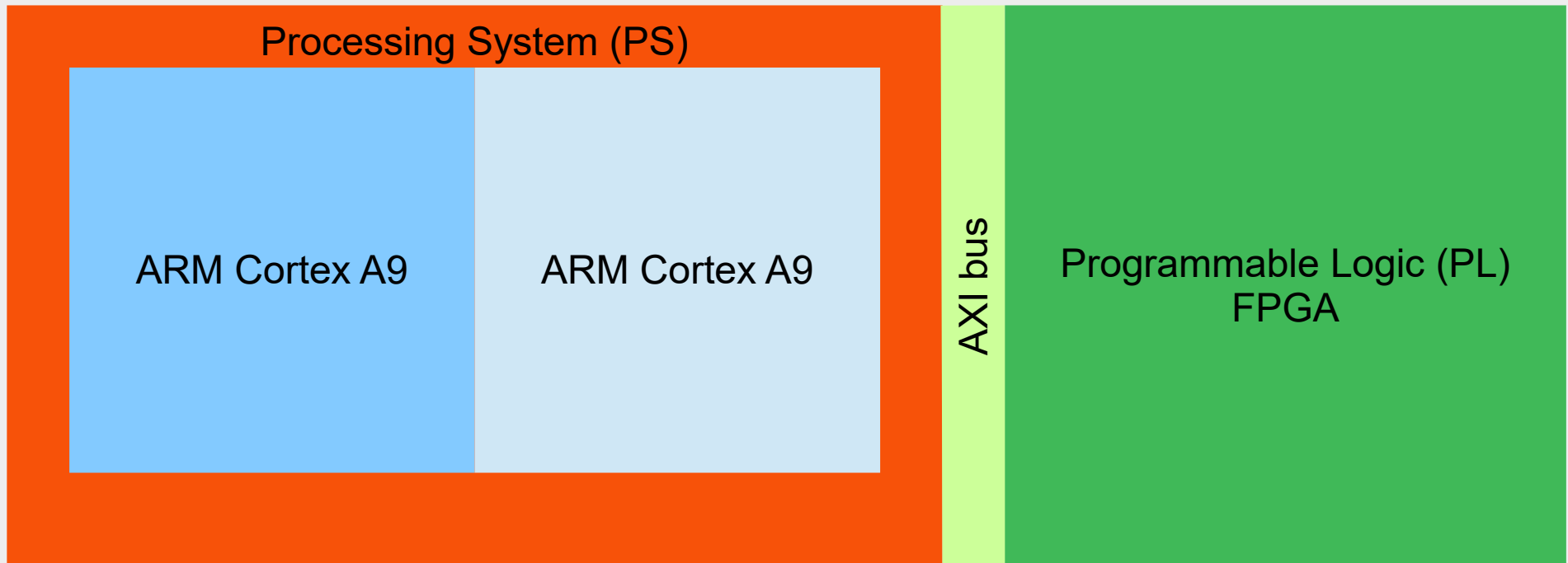
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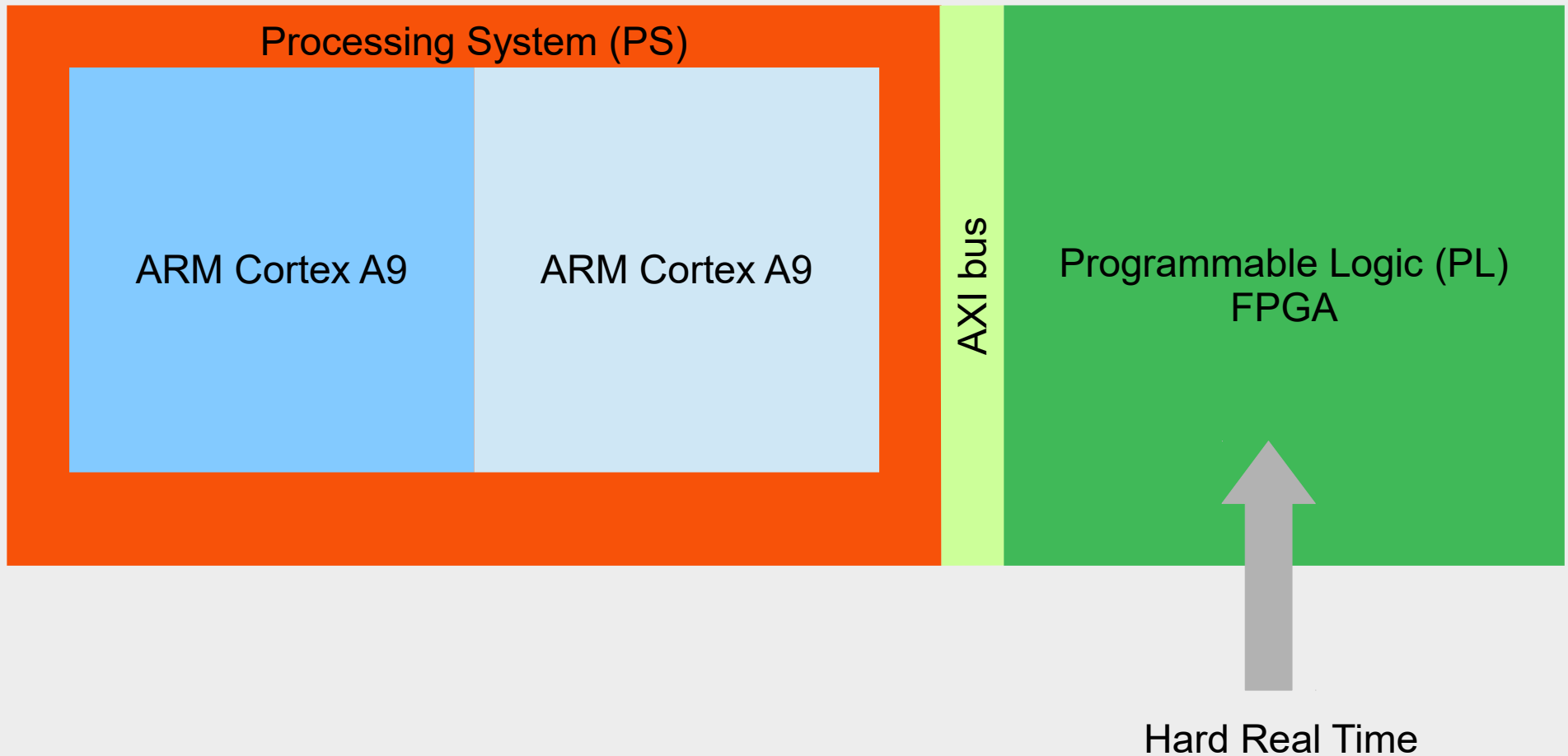
The TrustZone IP



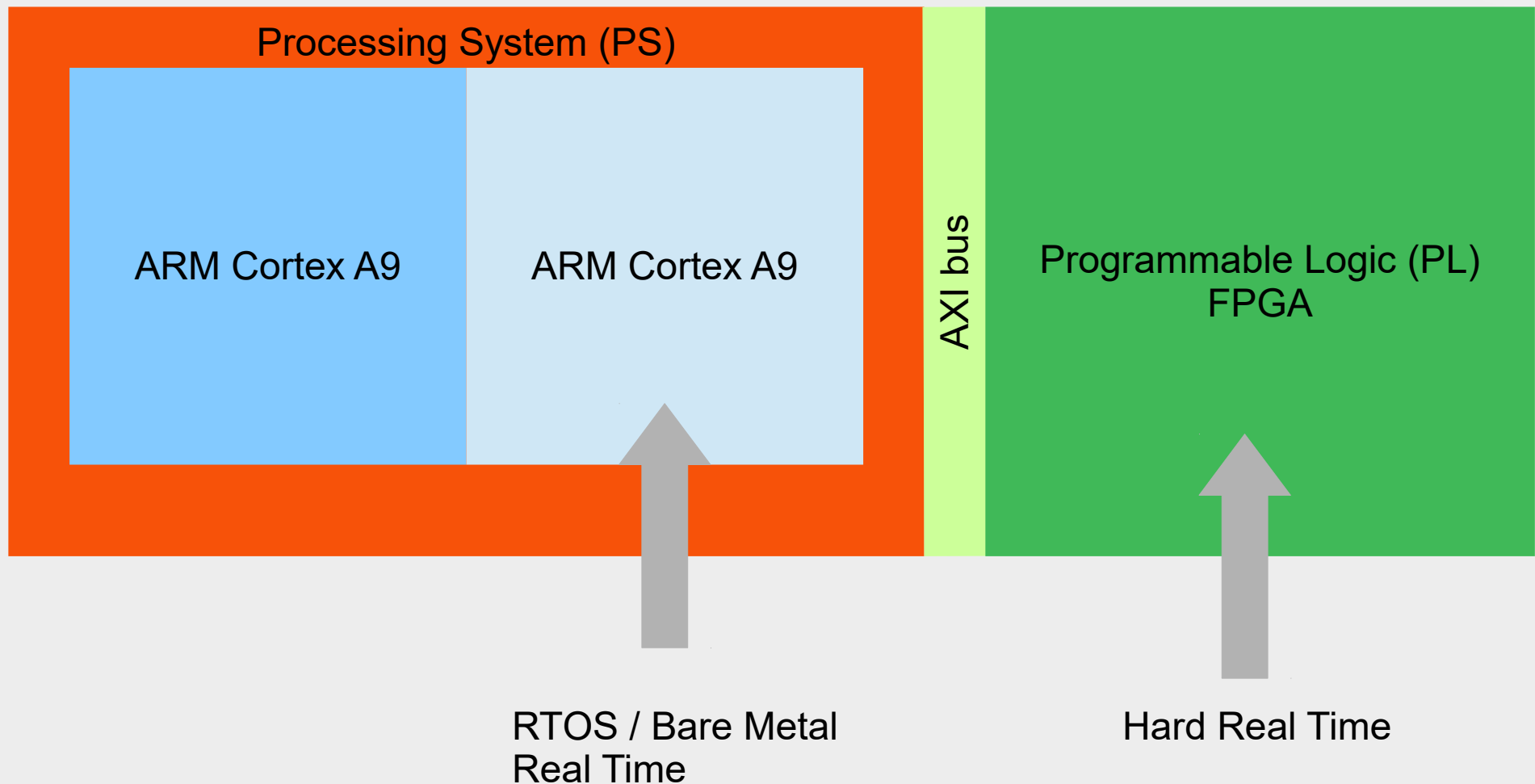
The Asymmetric Multi Processing on Zynq Architecture



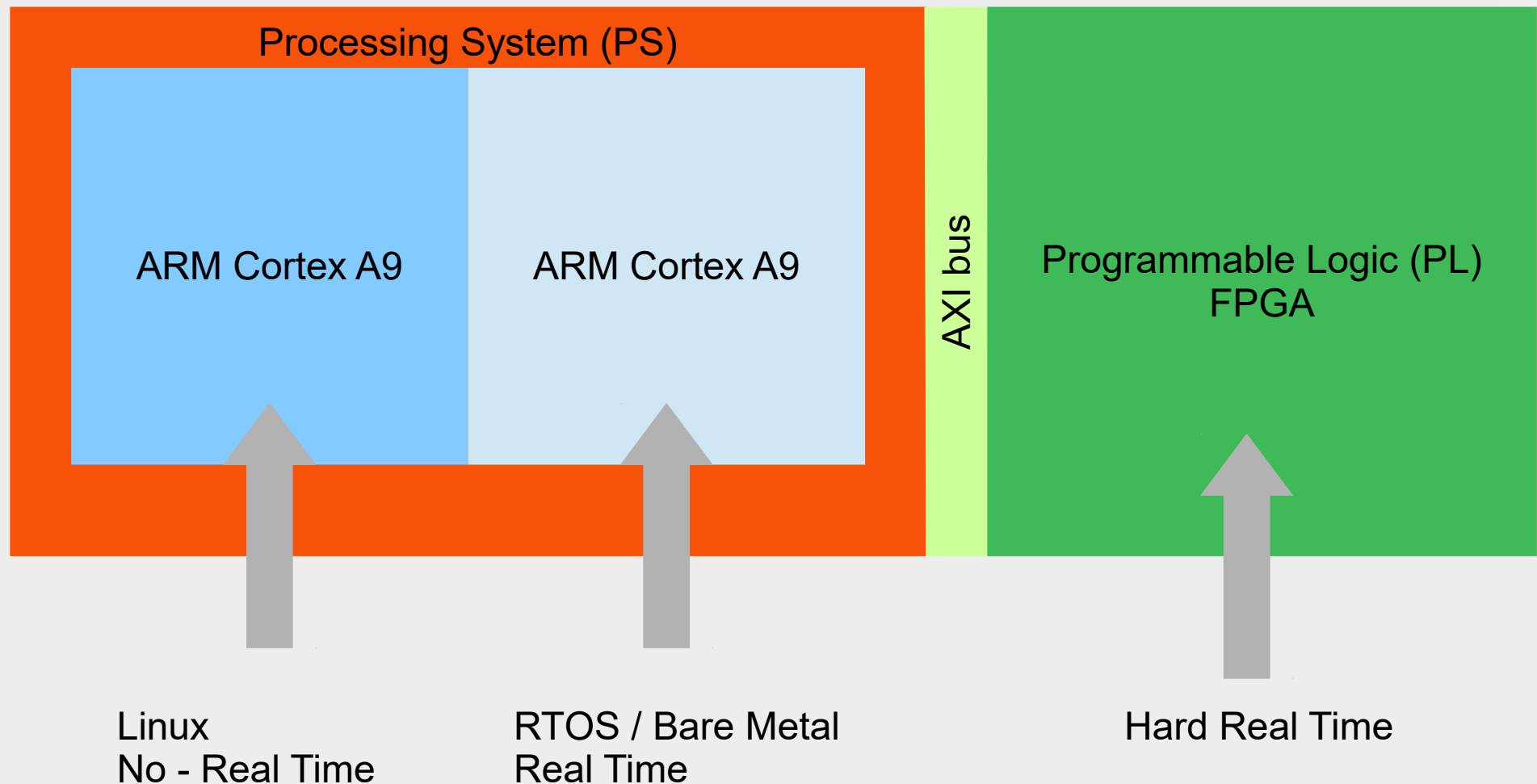
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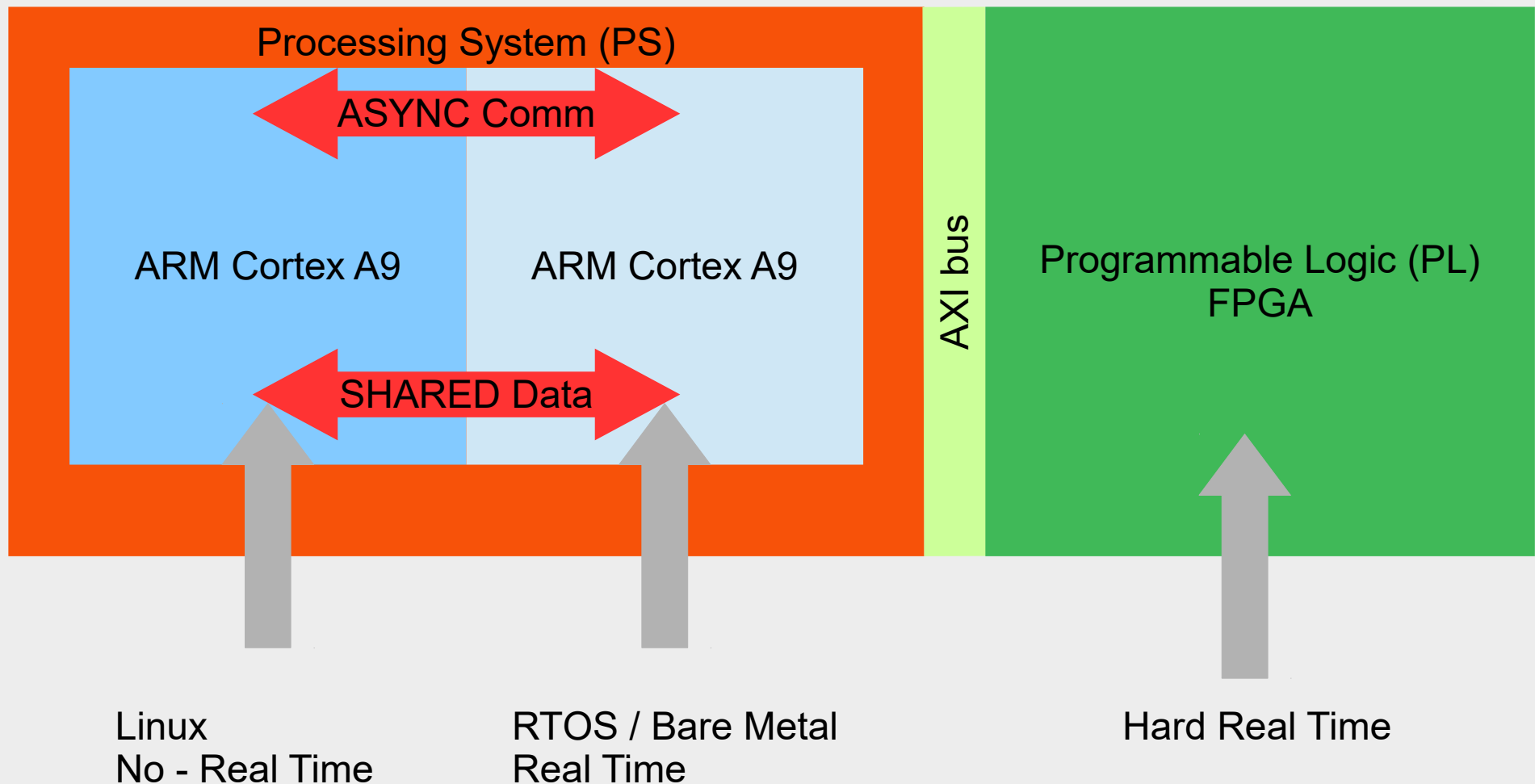
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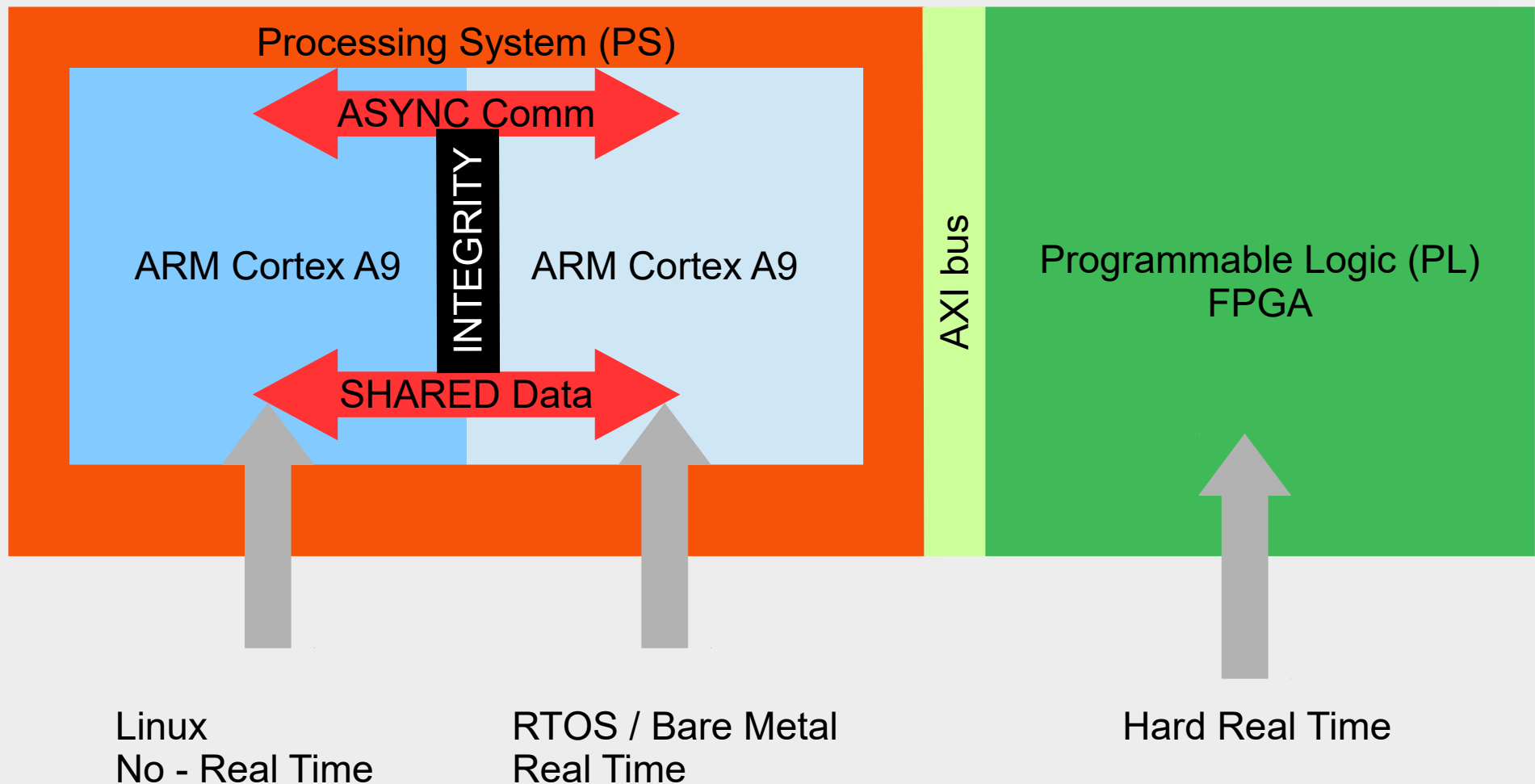
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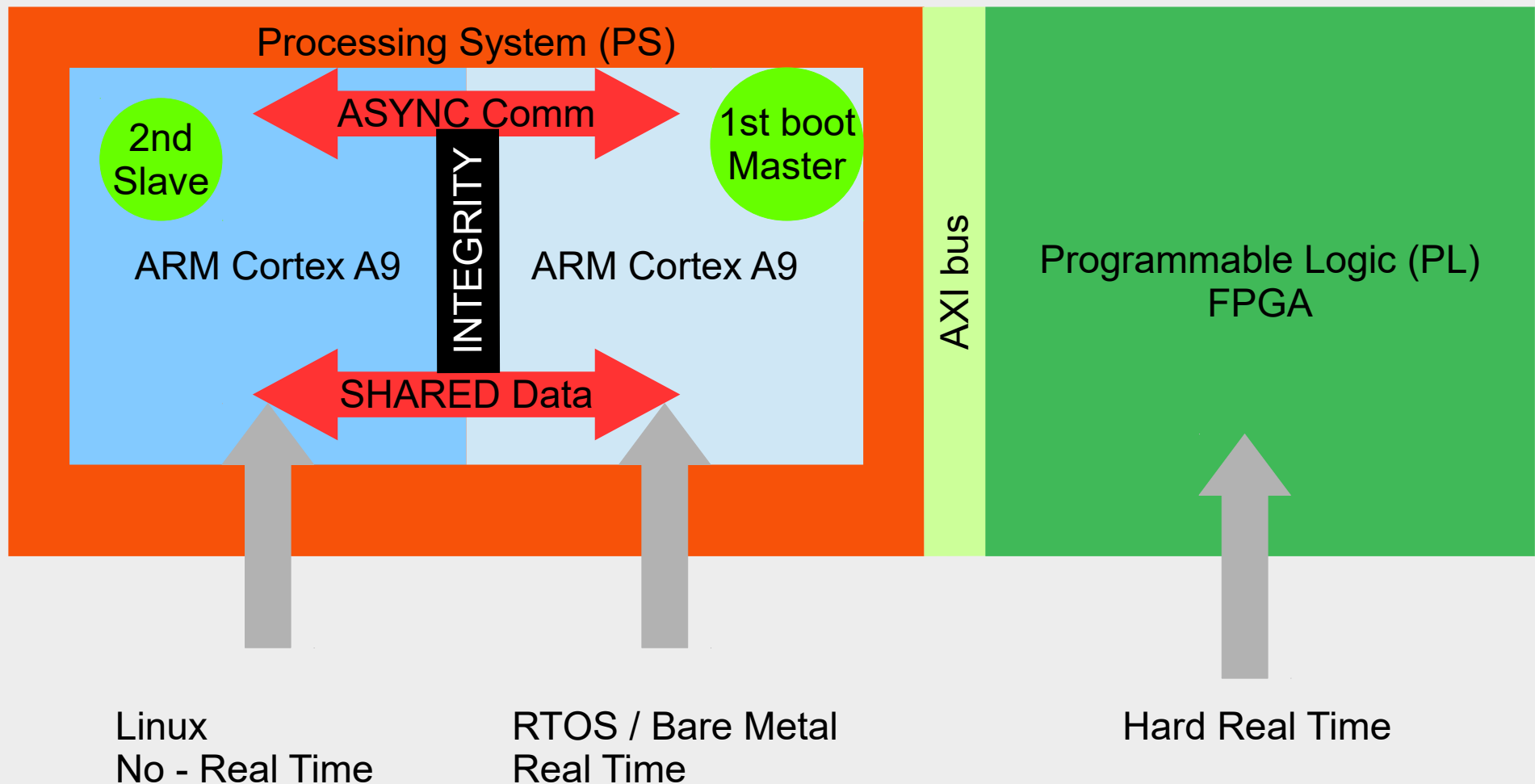
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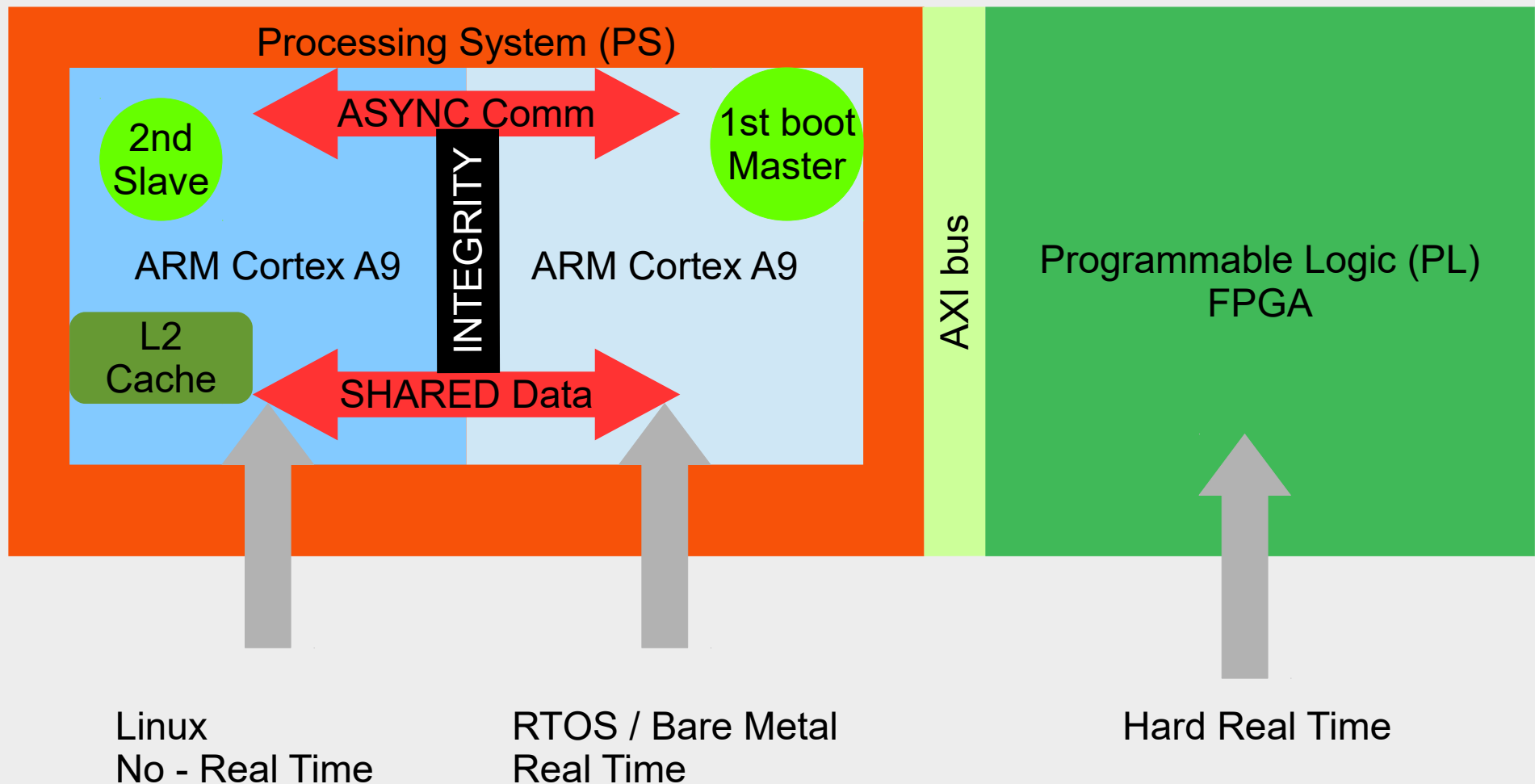
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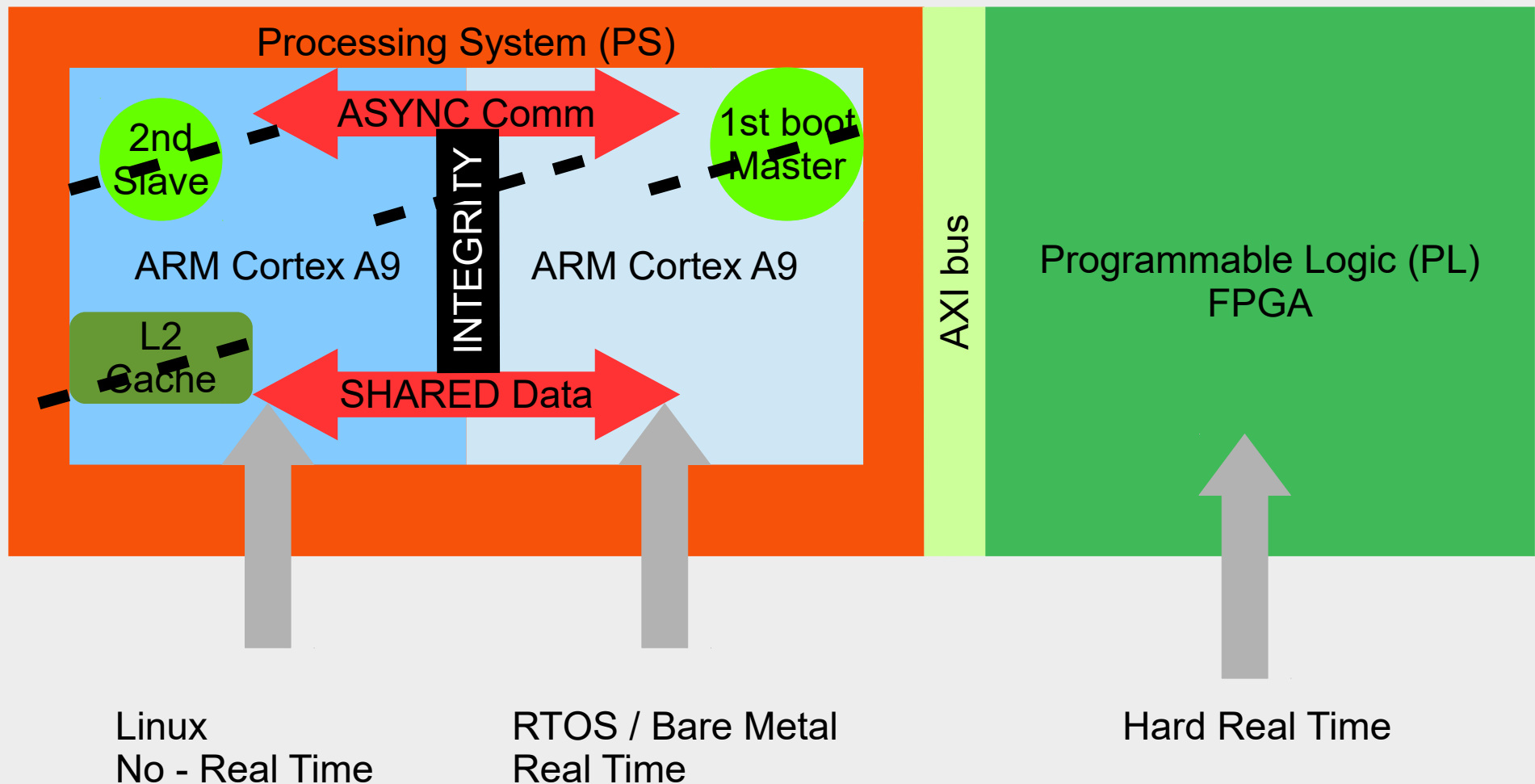
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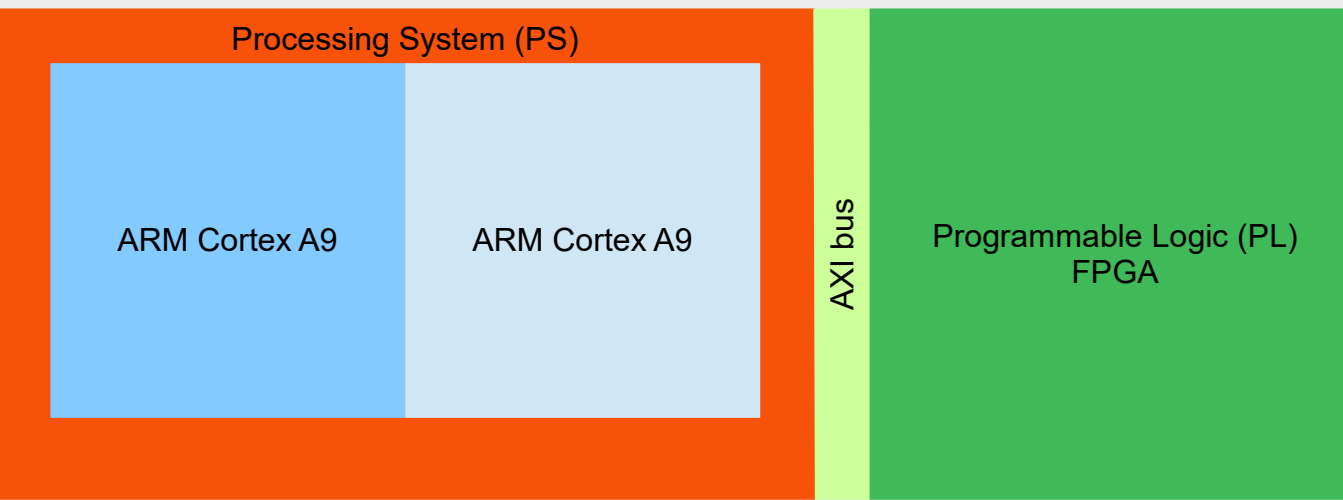


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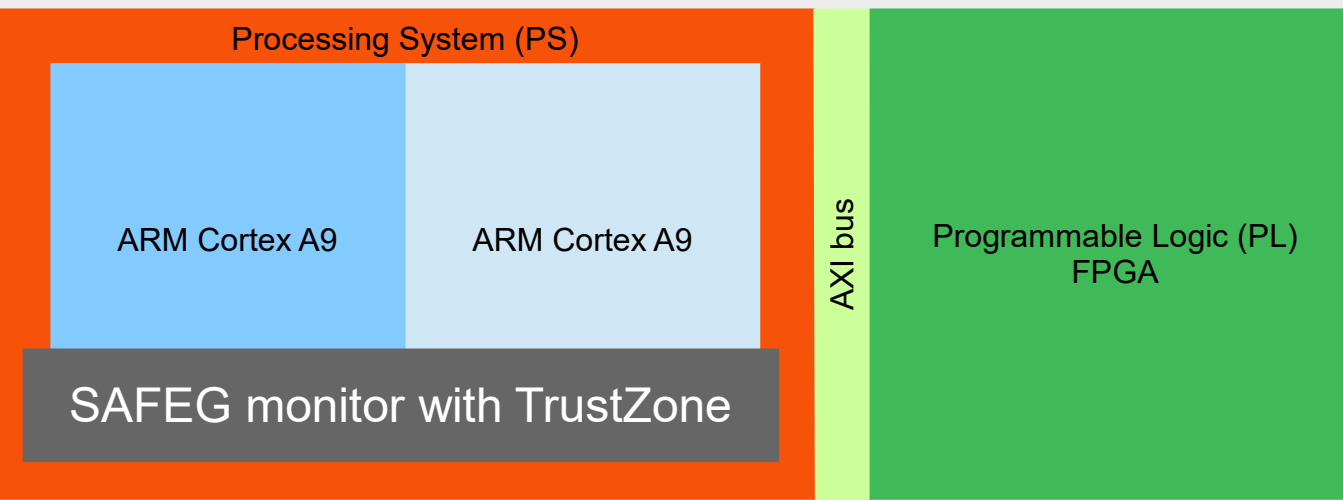
Traditional AMP has not ALL these feature so,
integrate all new feature listed?

The TrustZone-based Approach



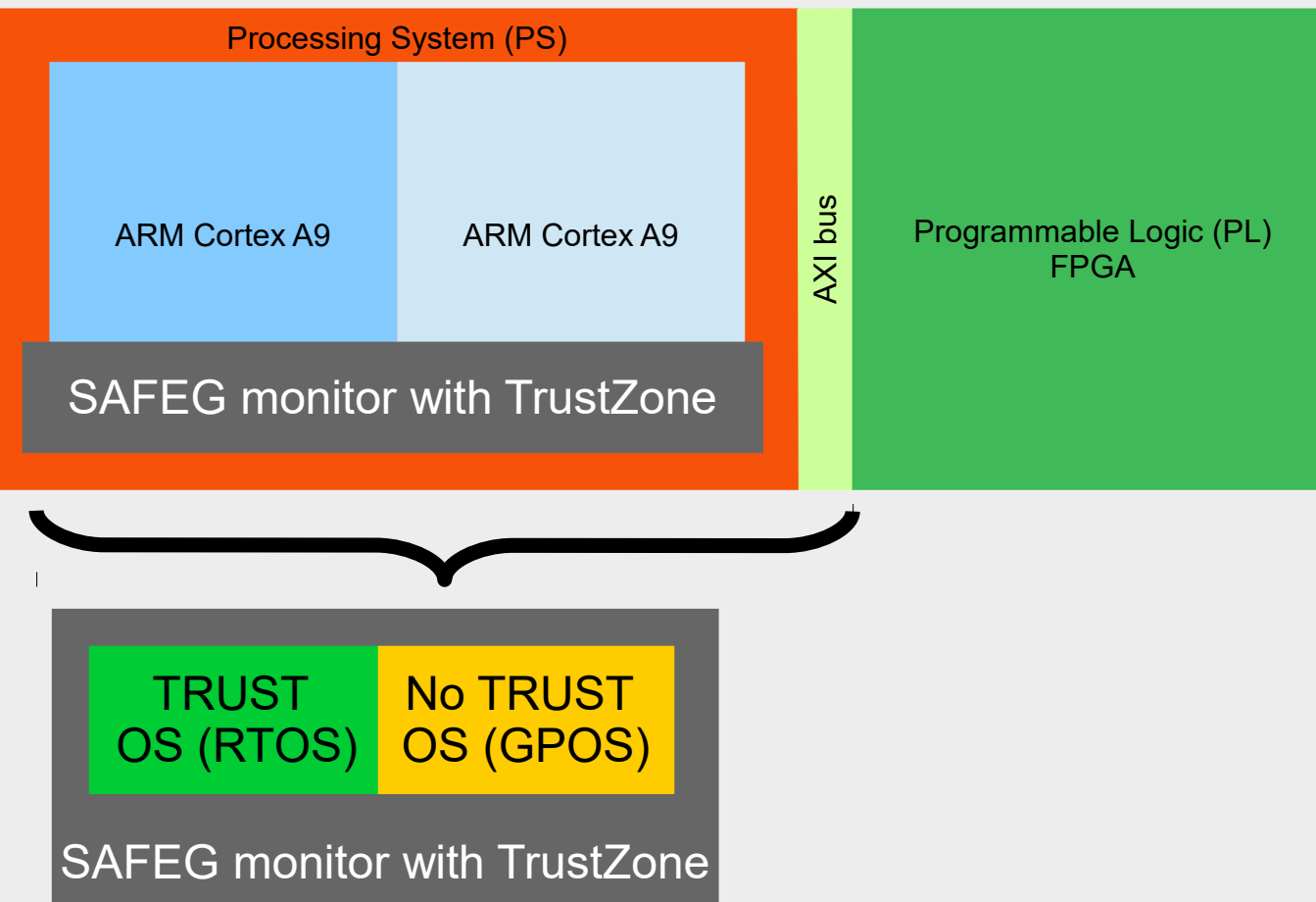
- It is required a Software Monitor

The TrustZone-based Approach



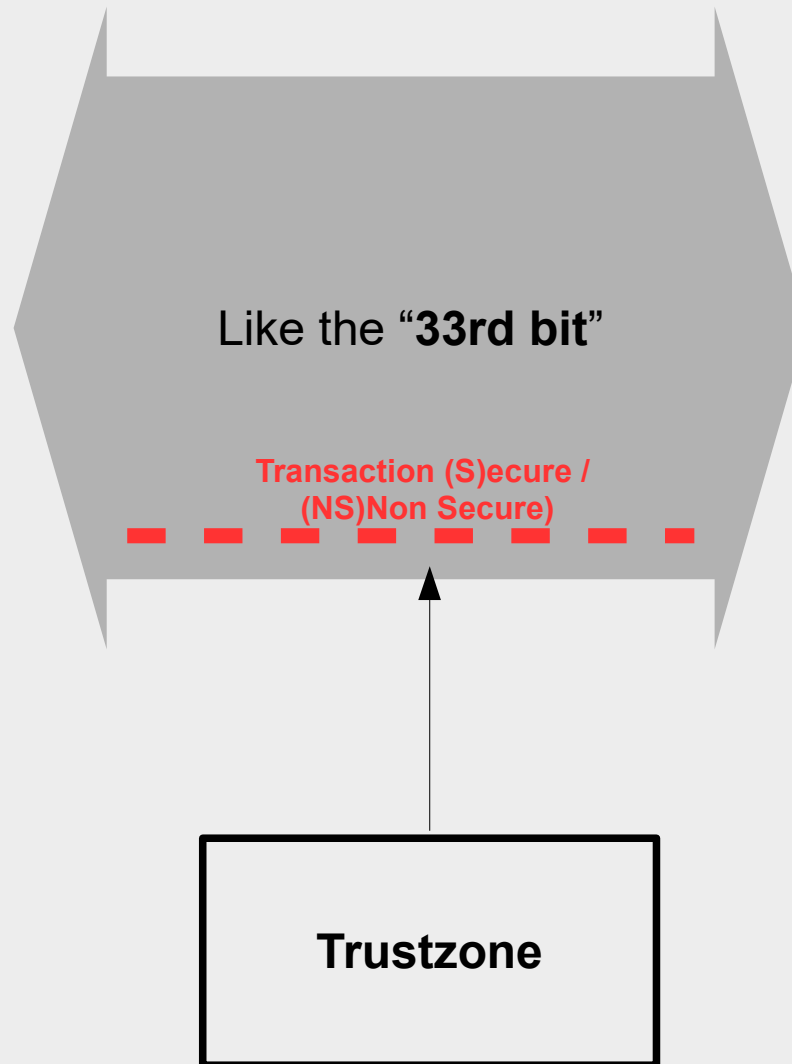
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The TrustZone-based Approach

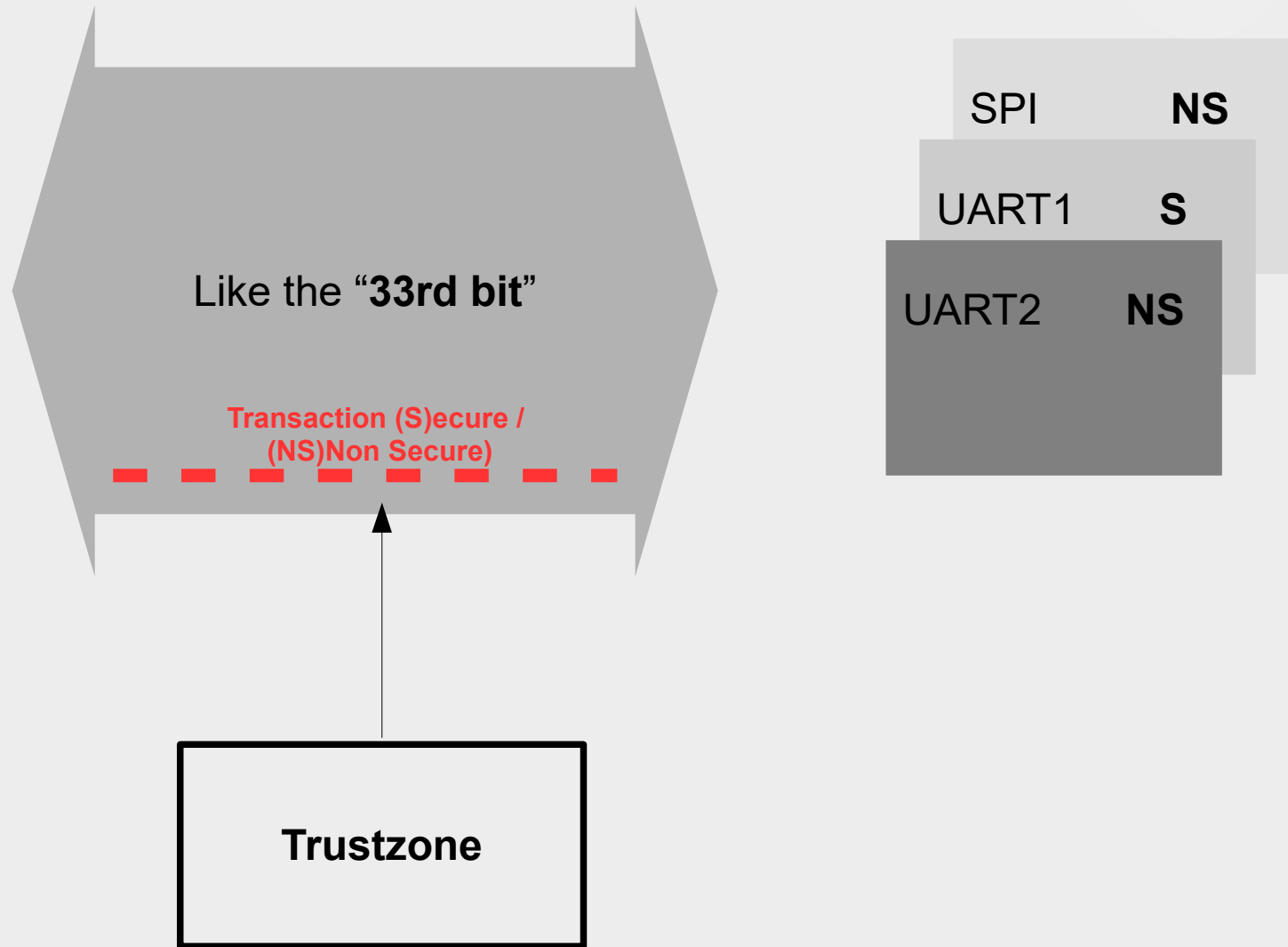


- It is required a Software Monitor
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- The monitor is responsible for:
 - Enable TrustZone IP
 - Initialize Trusted /Non Trusted areas

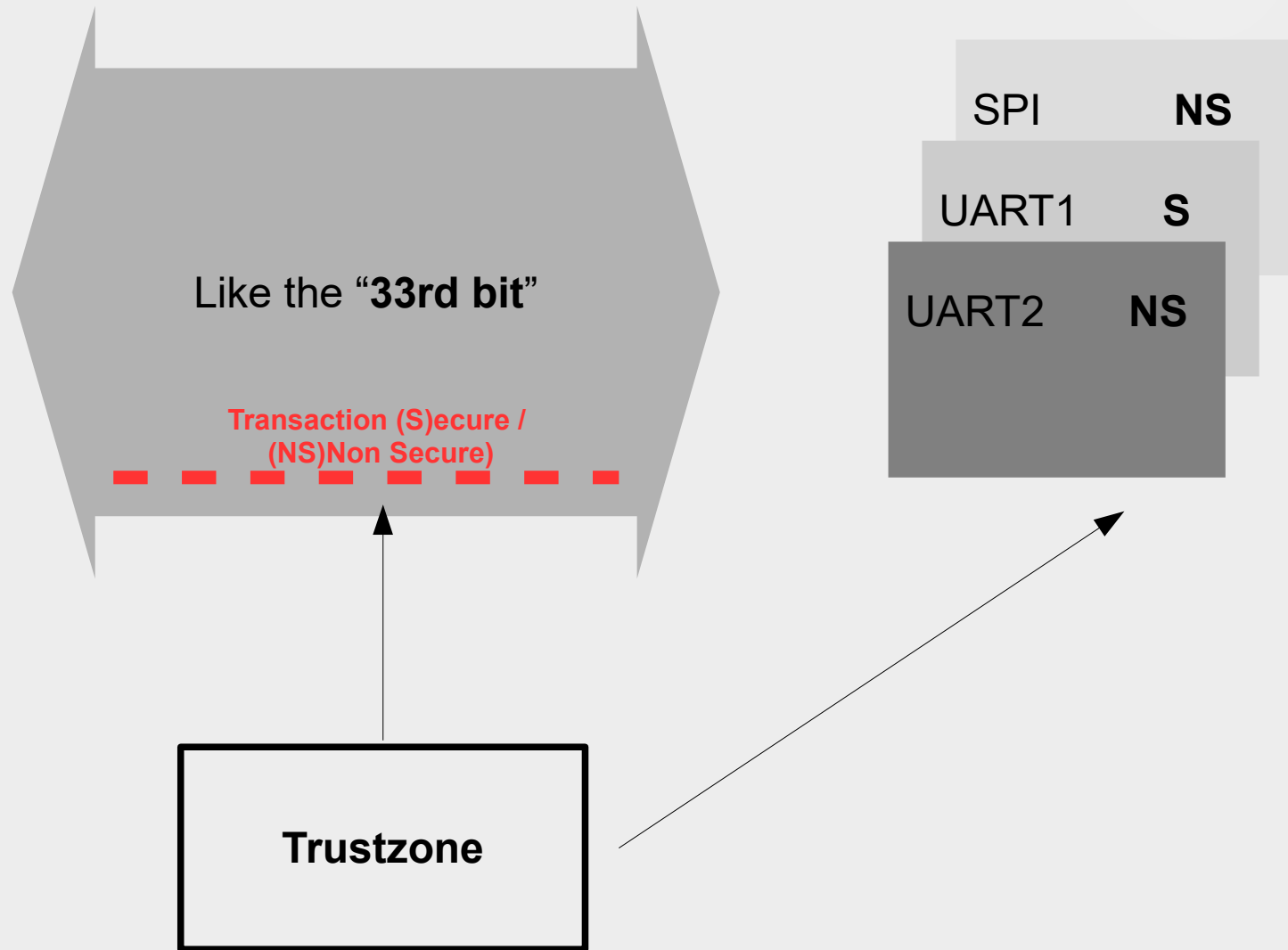
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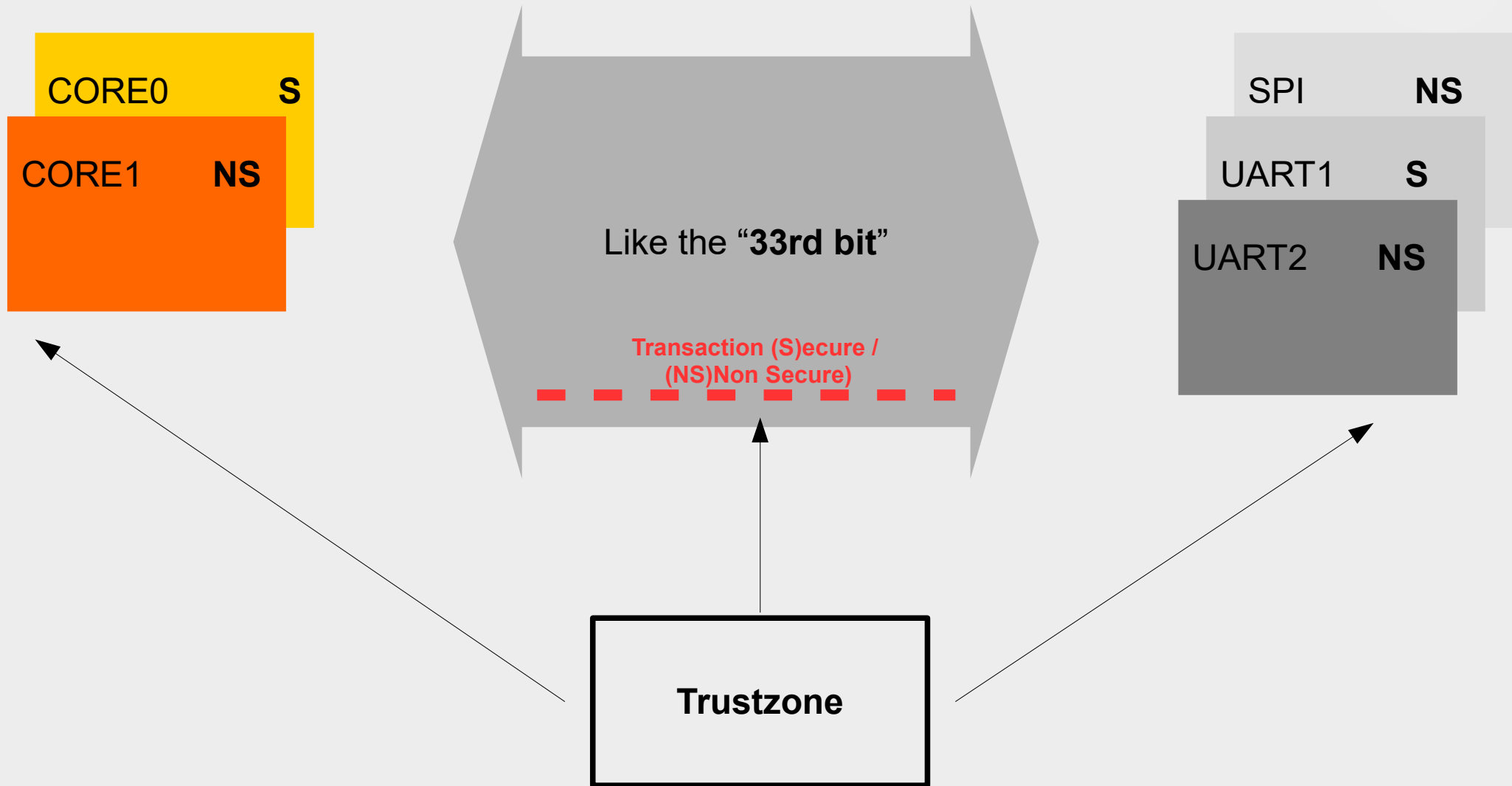
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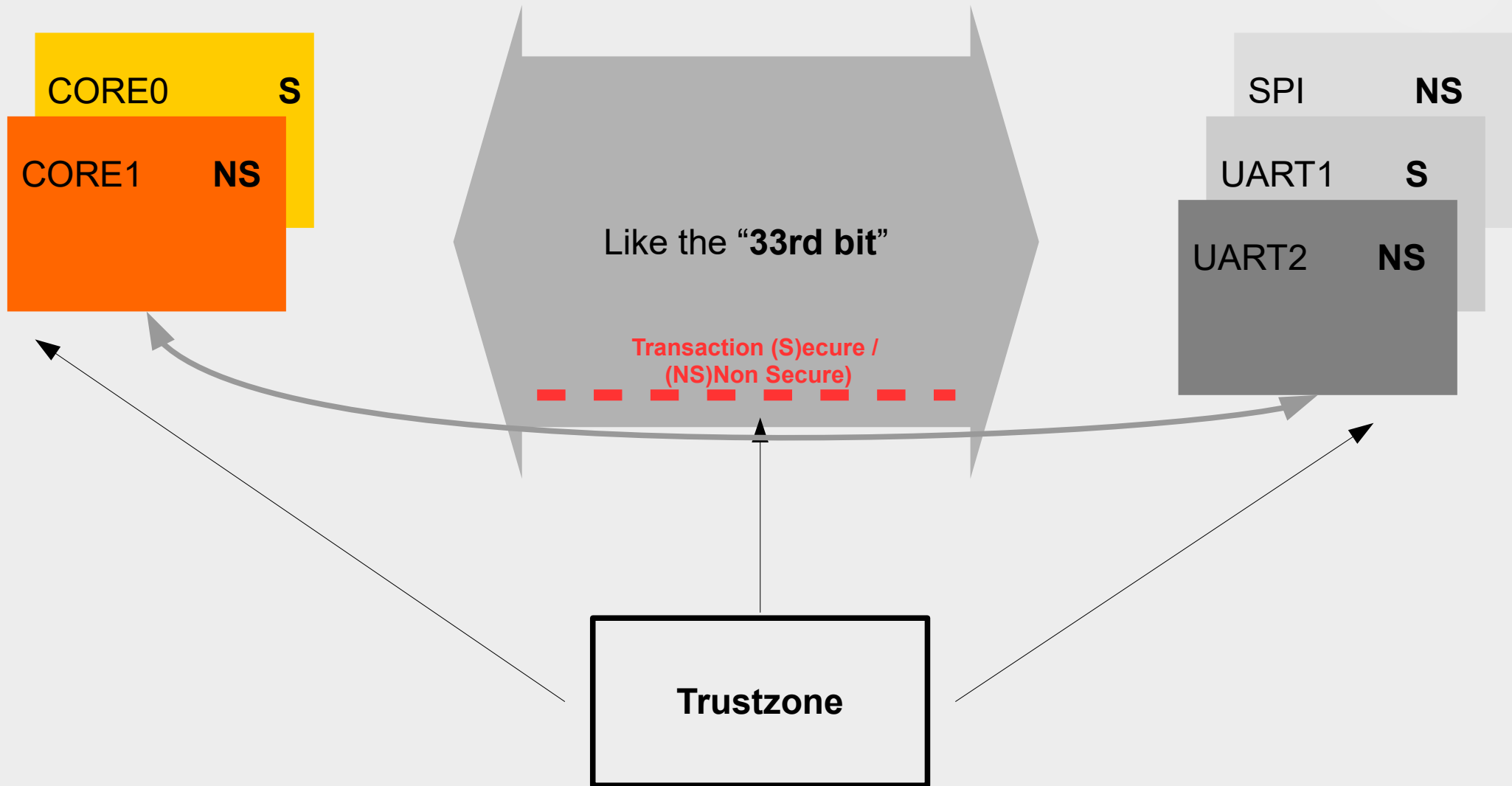
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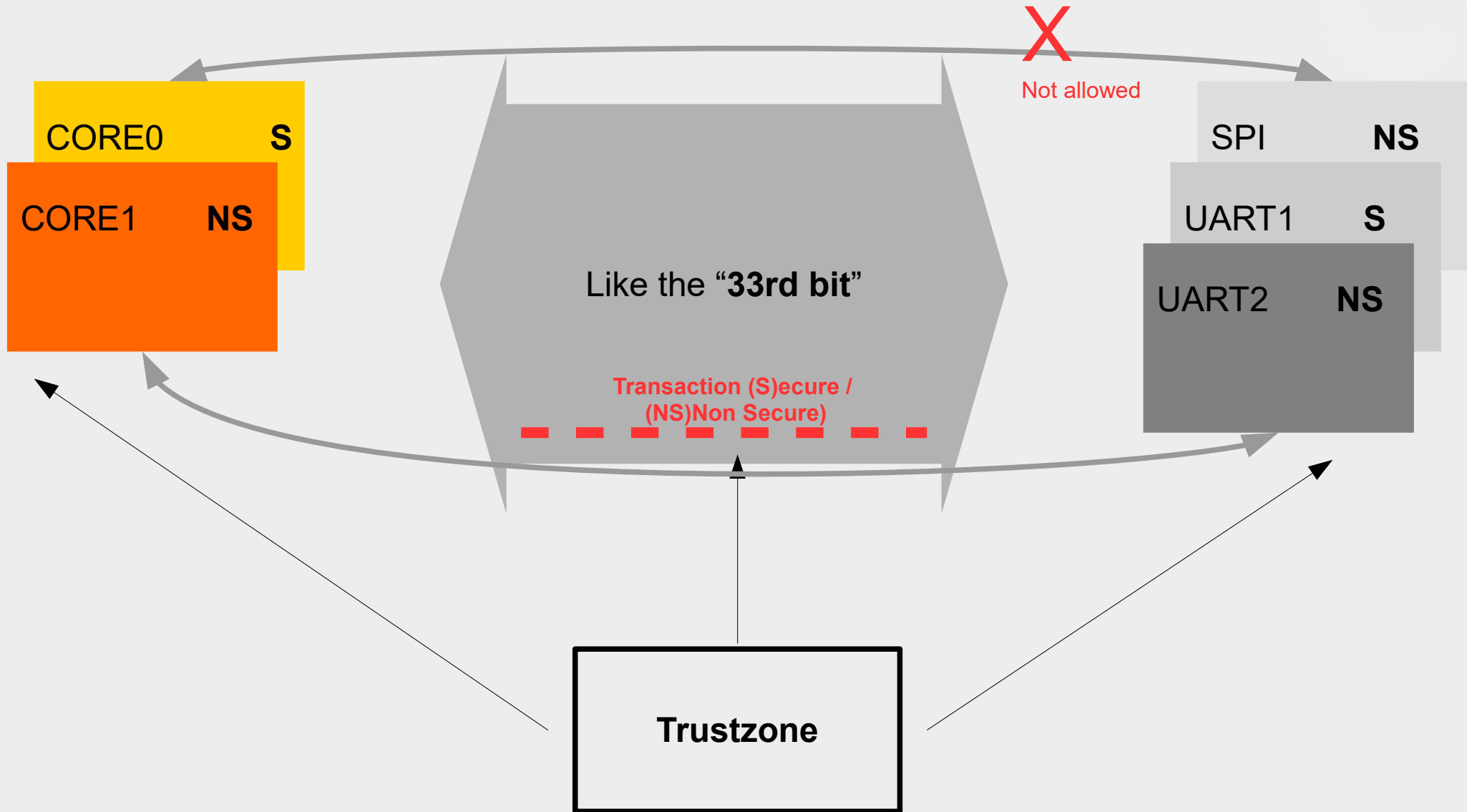
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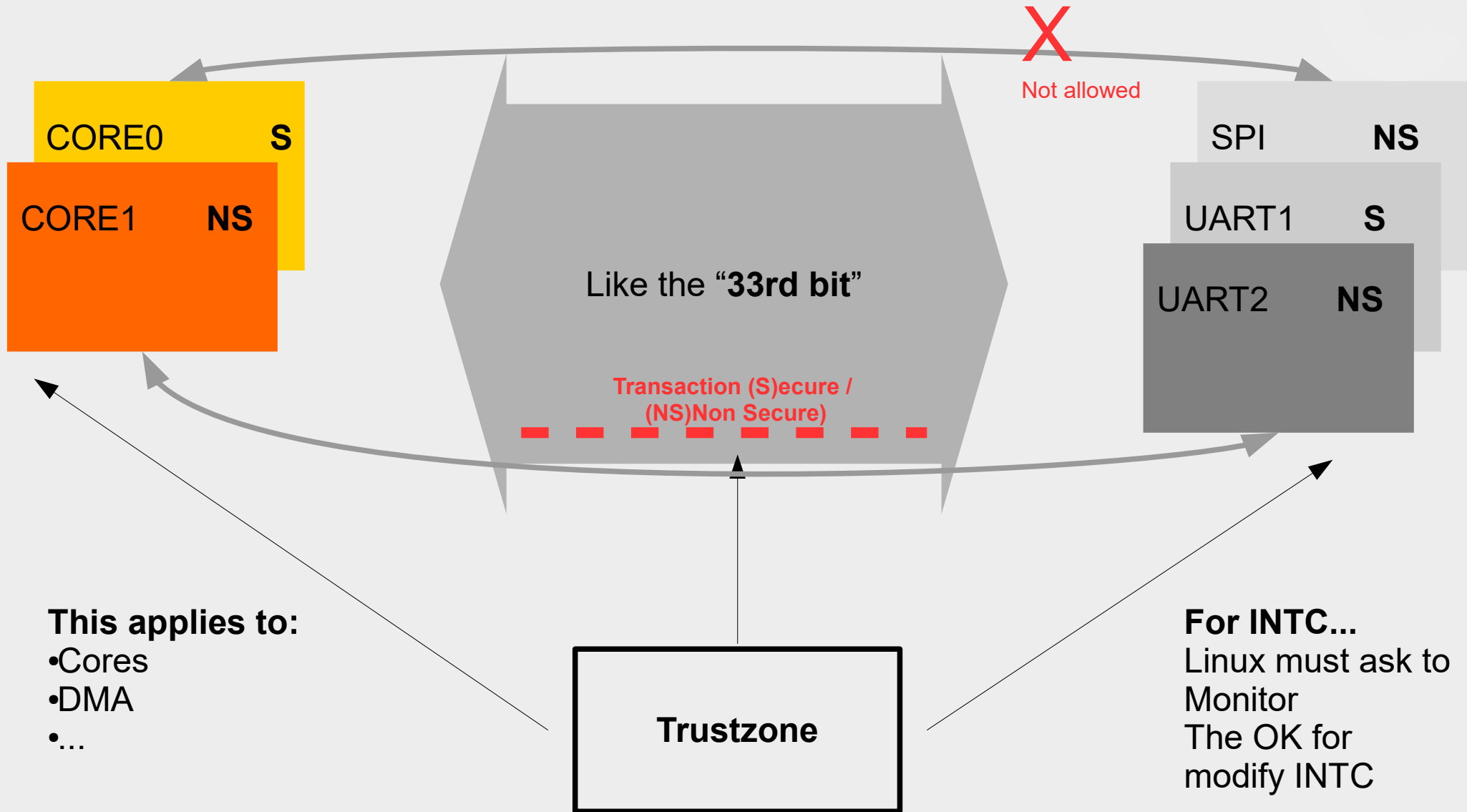
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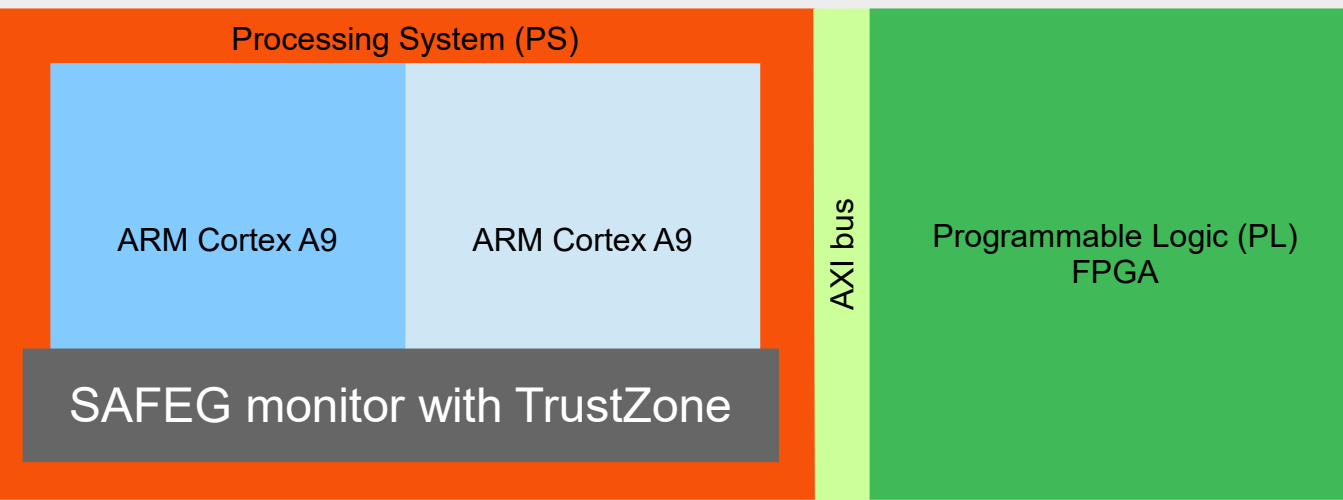
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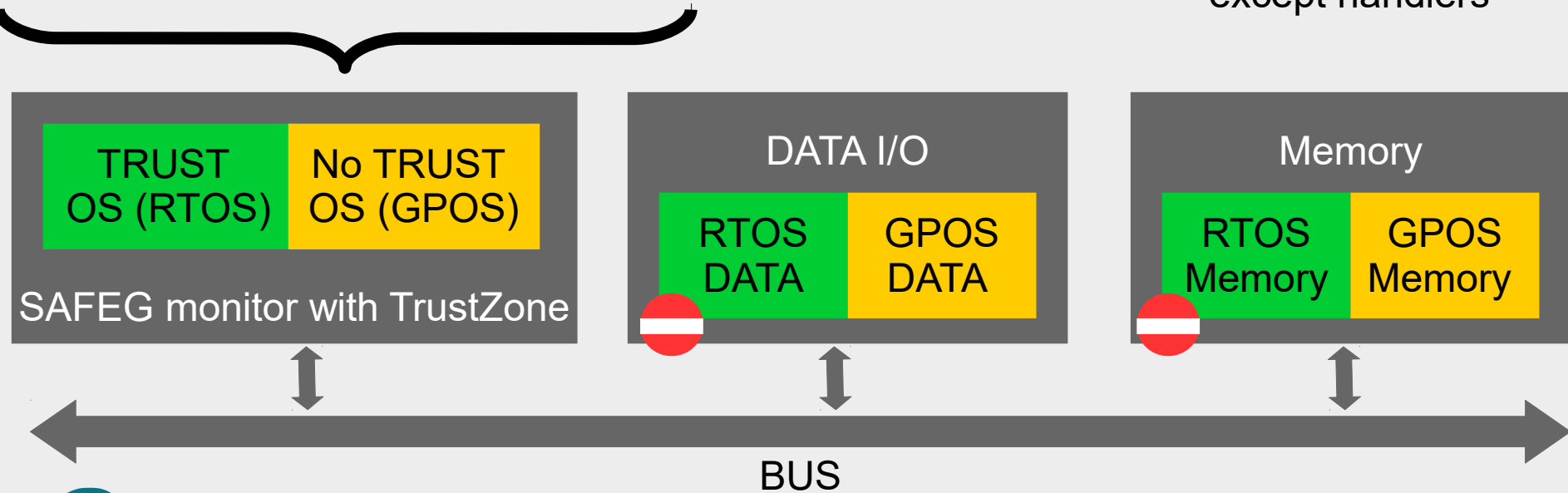
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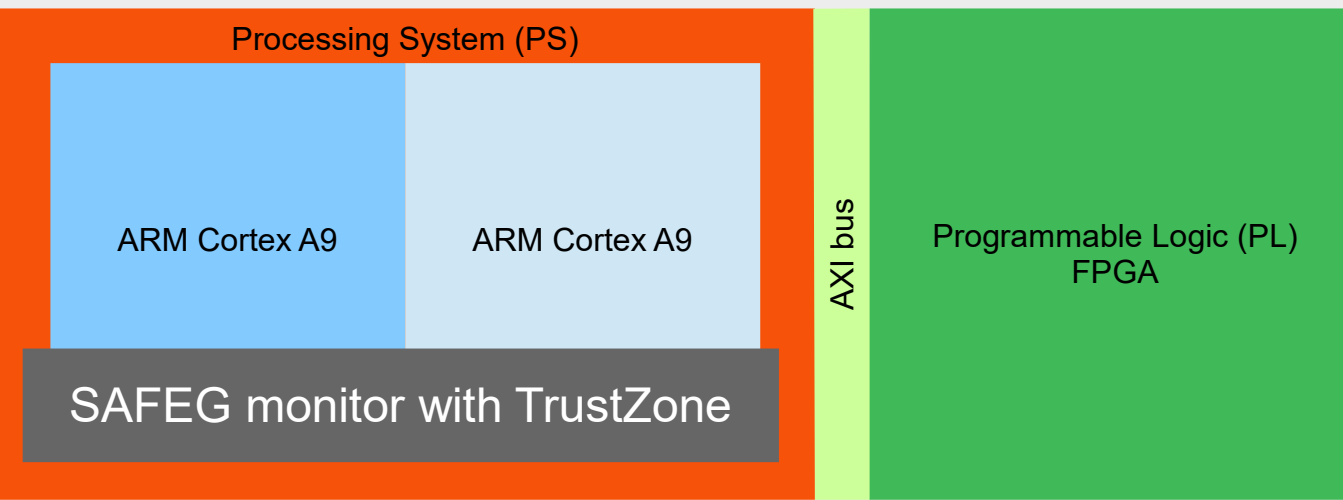
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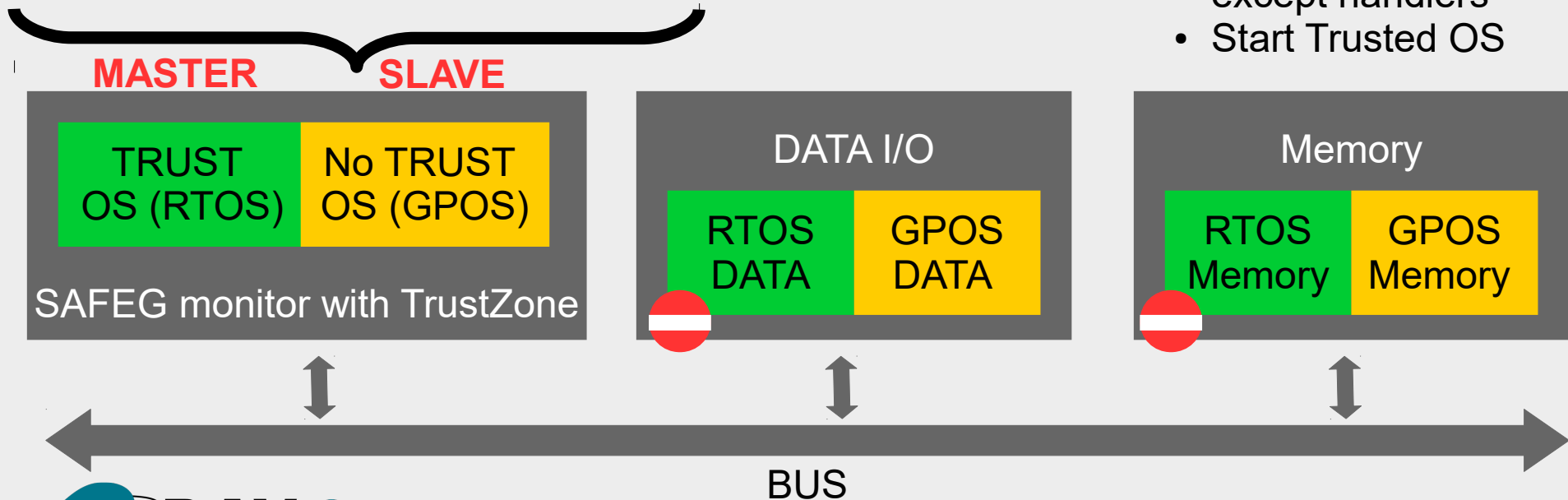
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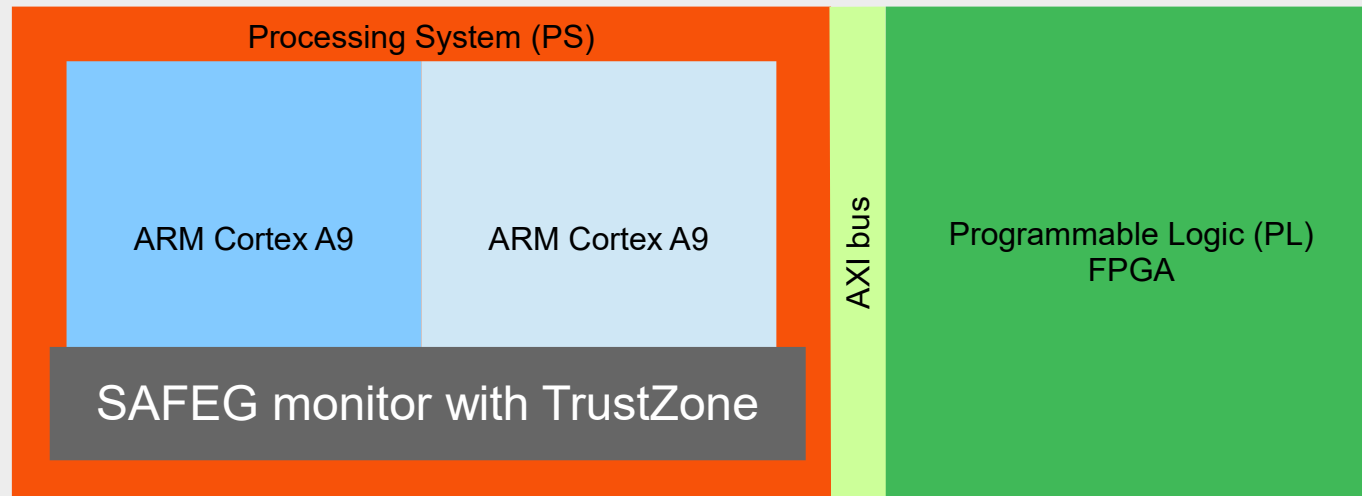
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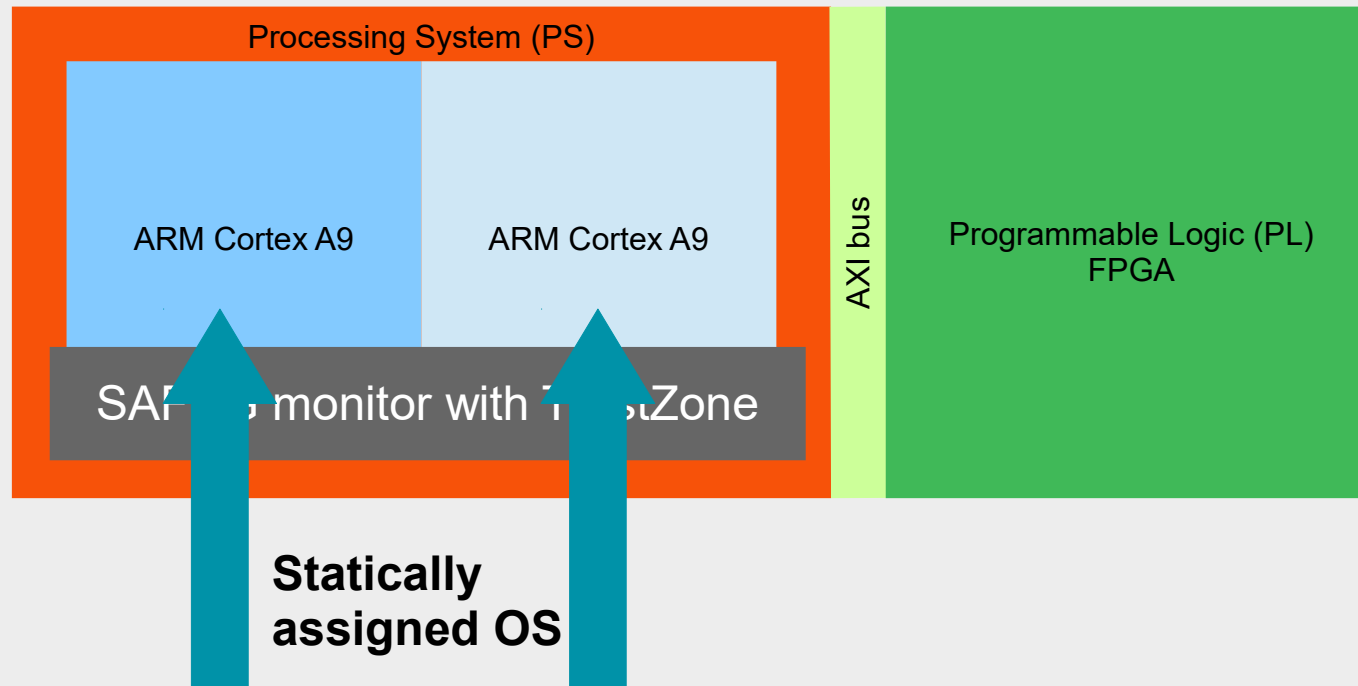
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 - Start Trusted OS



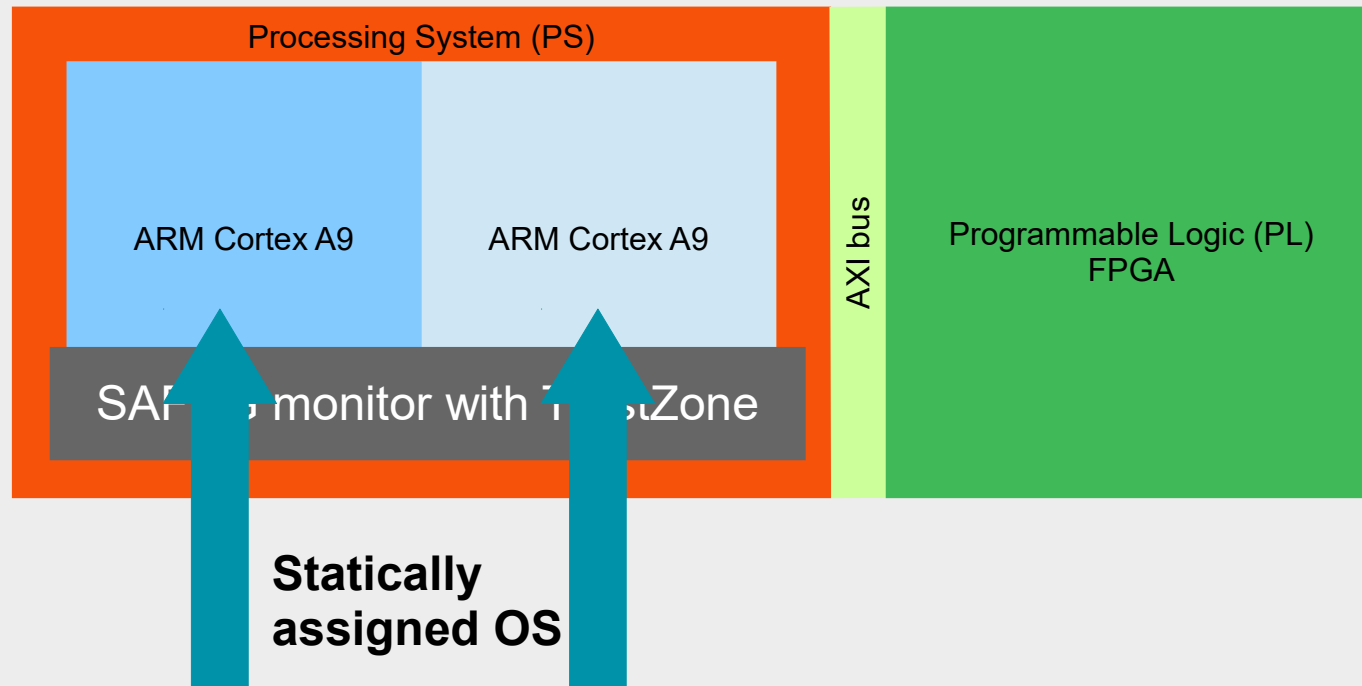
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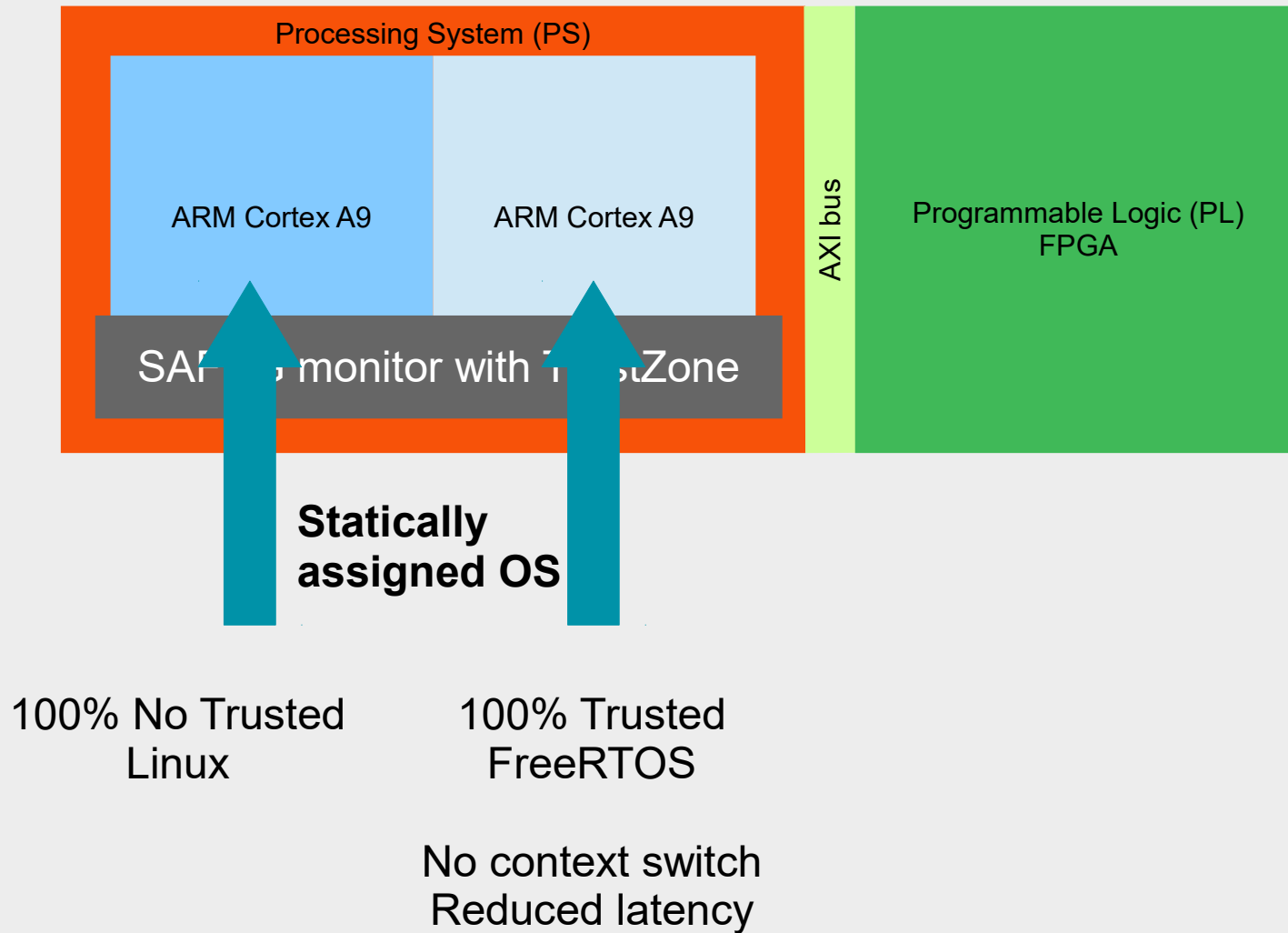


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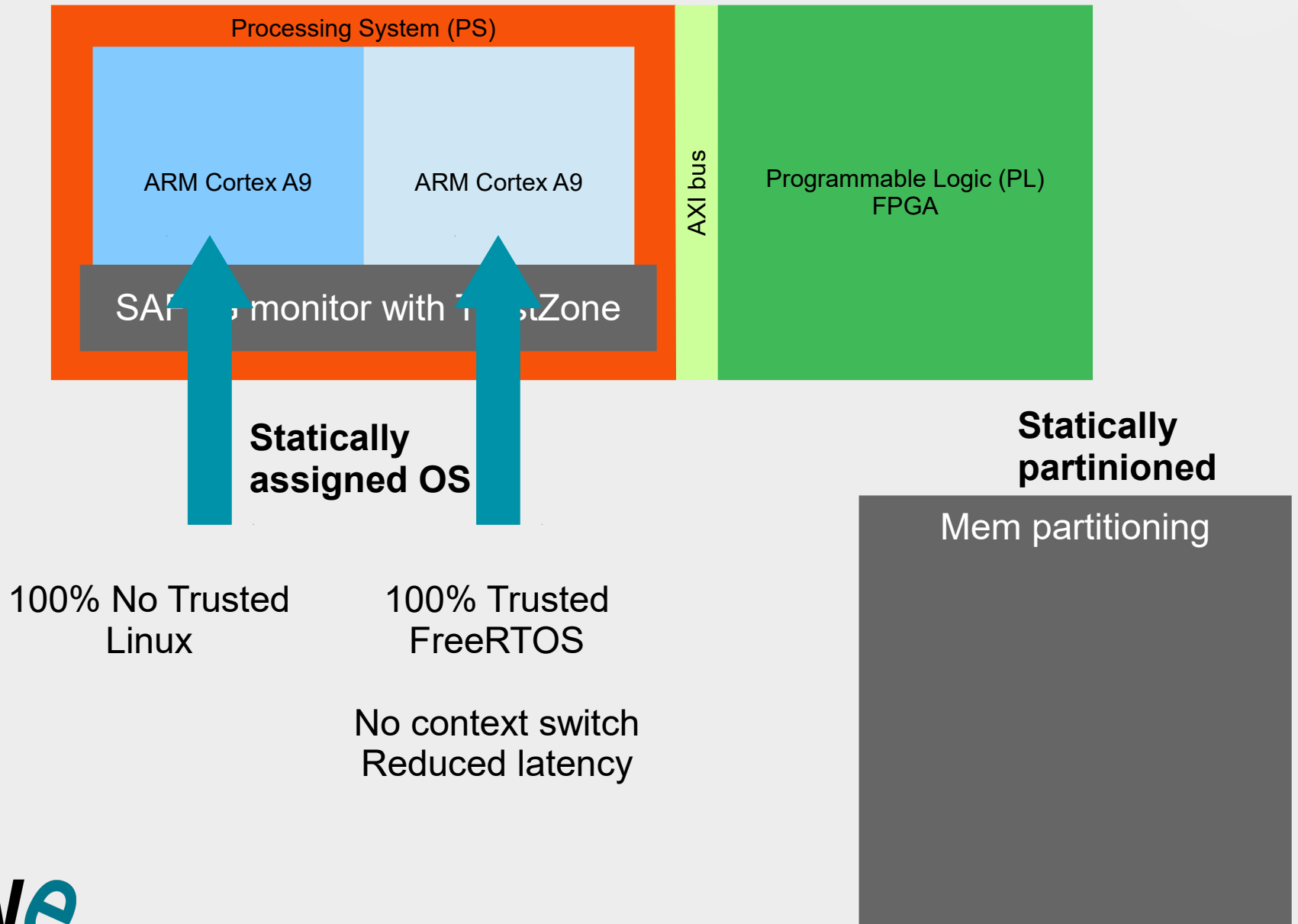


100% No Trusted
Linux

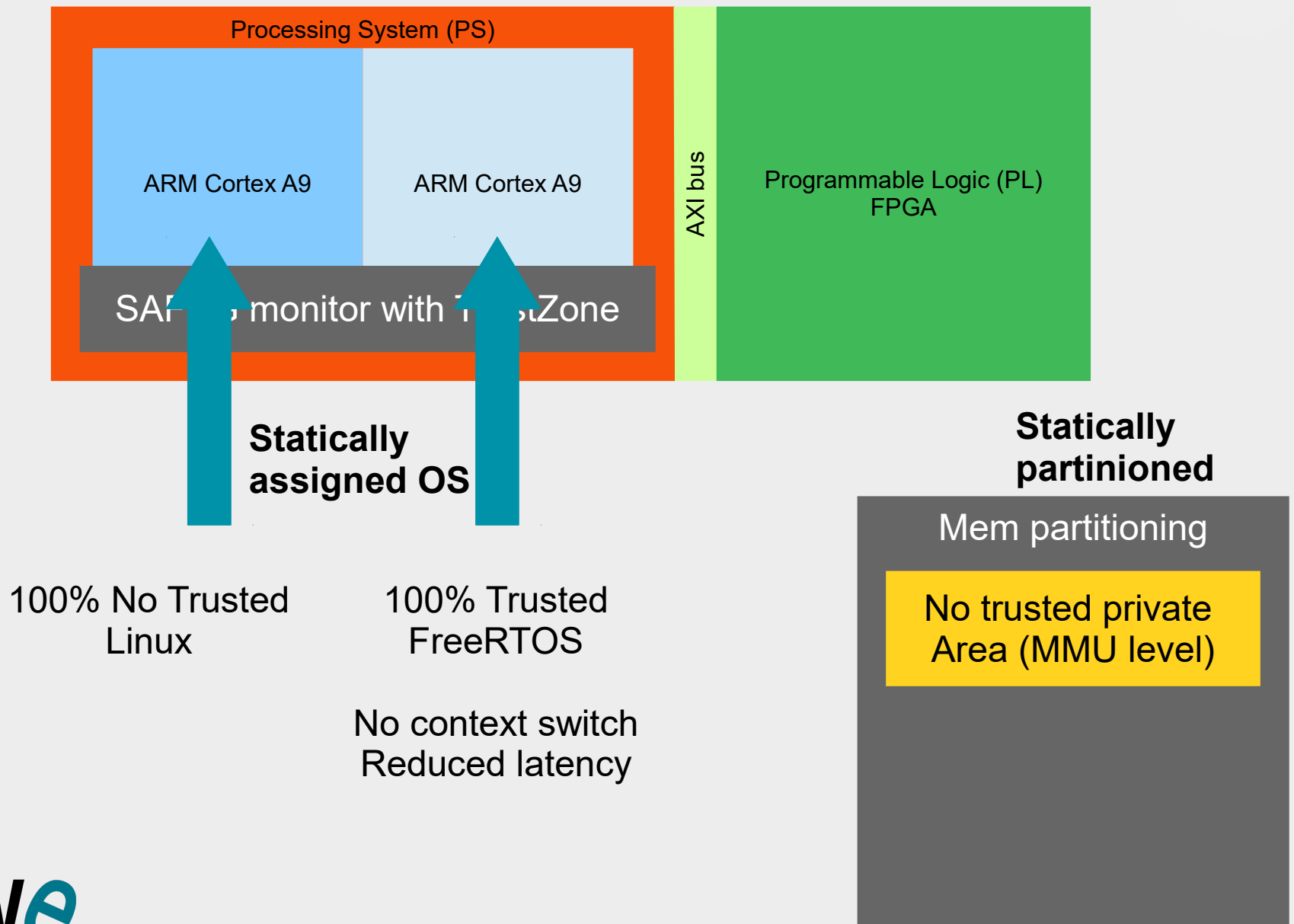
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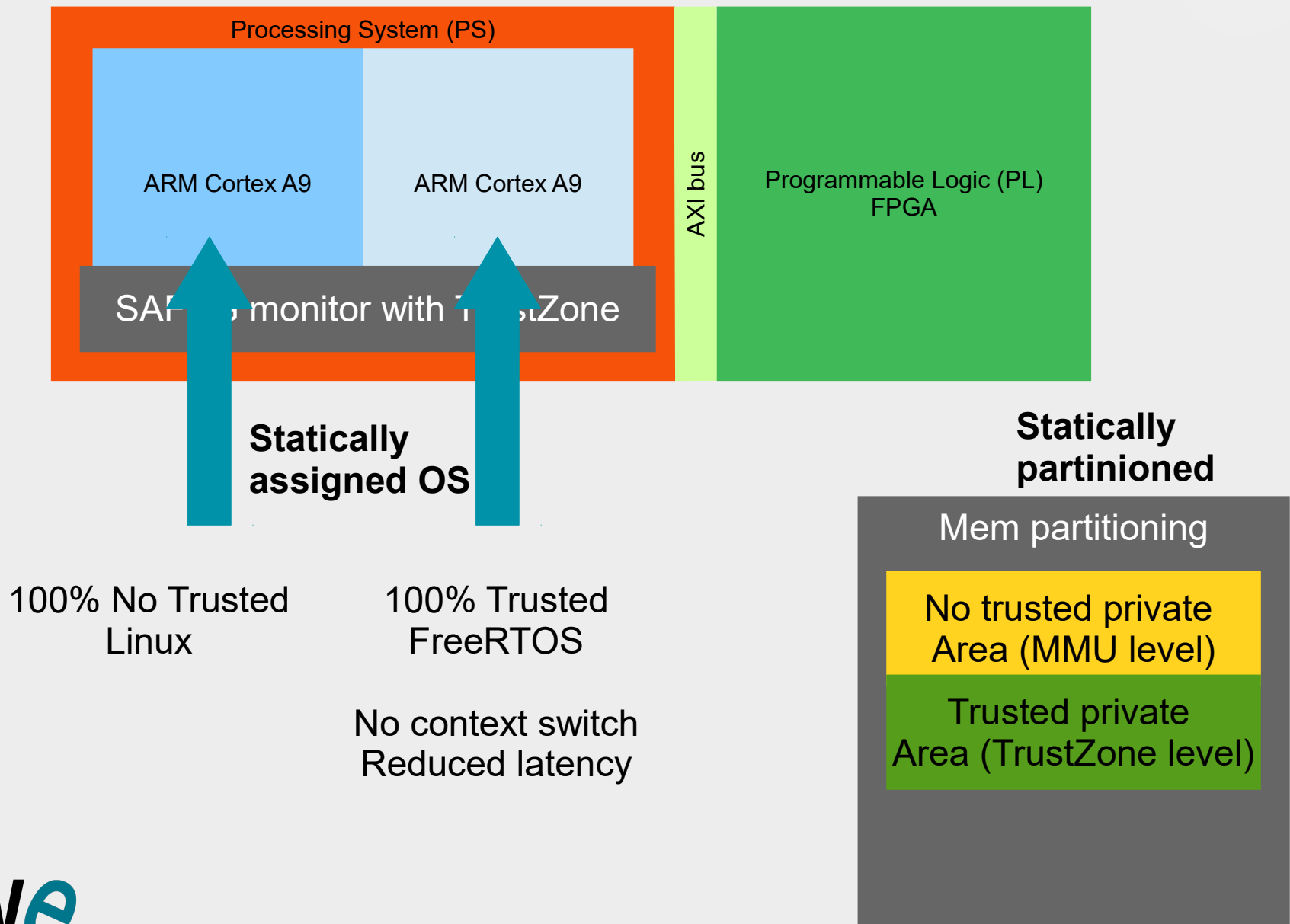
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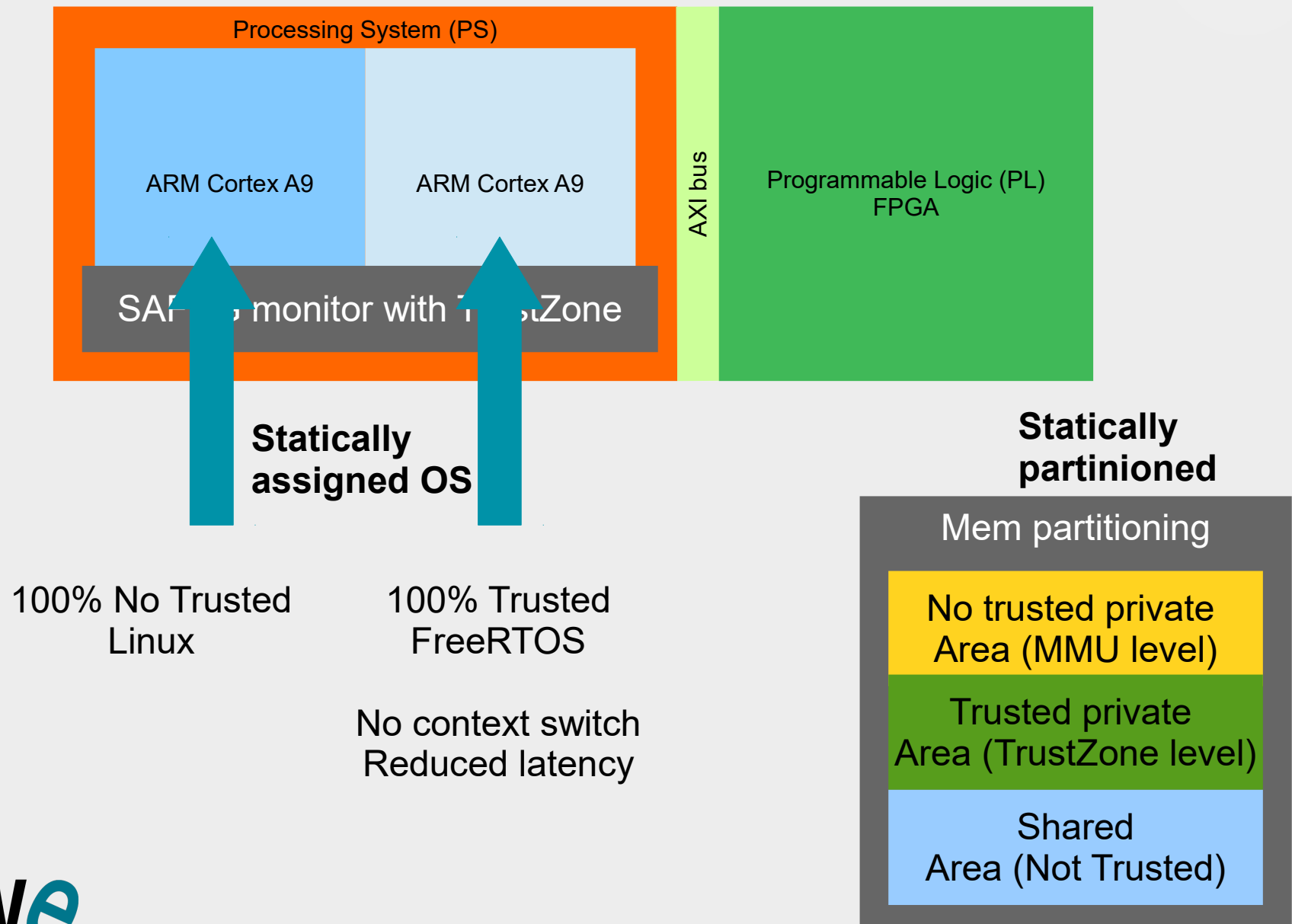
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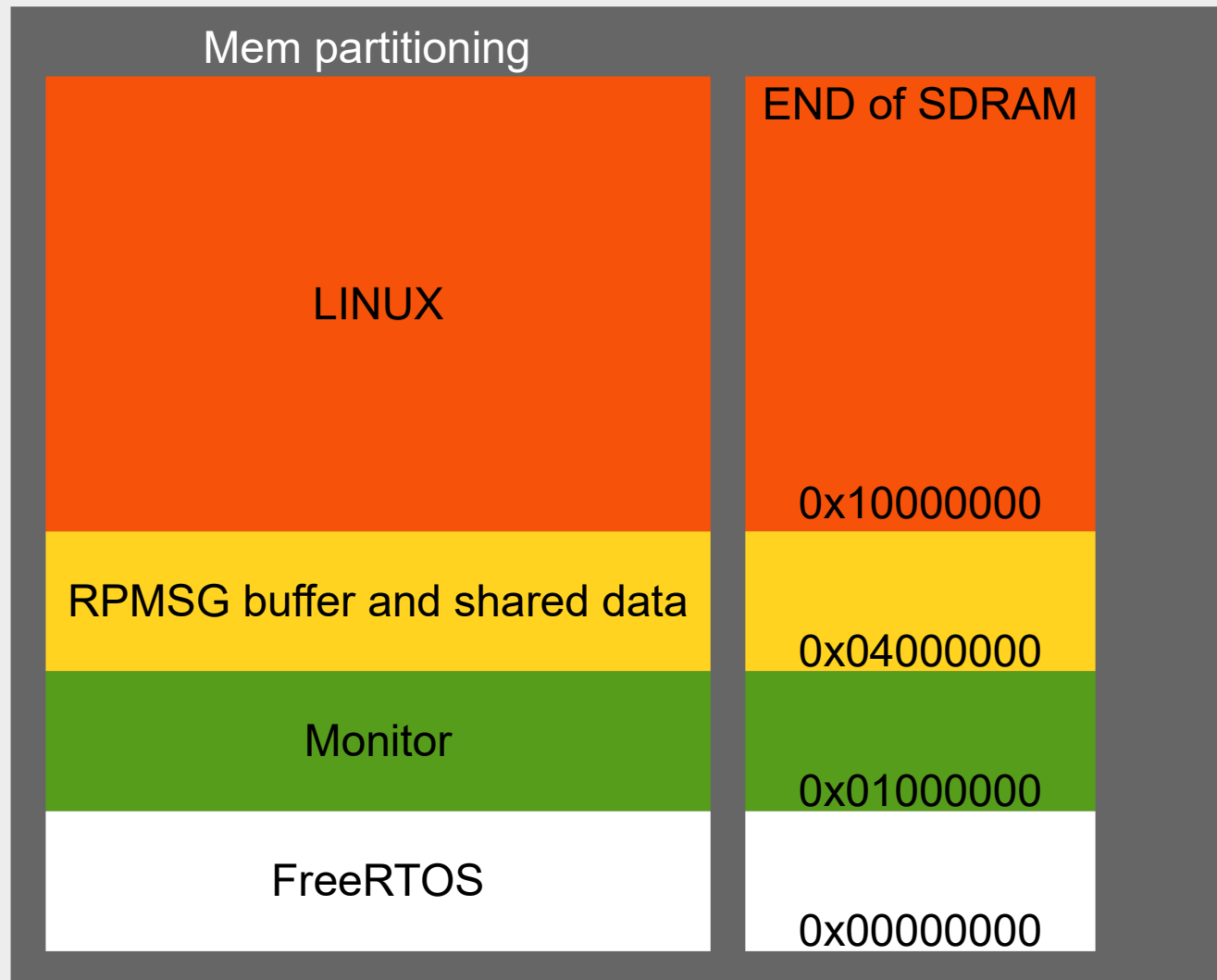
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DAVE Embedded Systems' example



Details: The MEM partitioning



Details: The B00T process

0 – RESET



Details: The B00T process

0 – RESET

1 – **BootROM**: FSBL taken from NV-memory and loaded on On Chip Memory

Details: The B00T process

0 – **RESET**

1 – **BootROM**: FSBL taken from NV-memory and loaded on On Chip Memory

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Details: The BOOT process

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- Monitor
- Trusted code FREERTOS
- No Trusted code LINUX

Details: The BOOT process

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Details: The BOOT process

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5 – **Monitor**:

- Init TrustZone
- Enable data structures and Handlers for both cores
- Gives to Trust code the control of machine FREERTOS

MASTER

Details: The BOOT process

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- Enable data structures and Handlers for both cores
- Gives to Trust code the control of machine FREERTOS

MASTER

6 – **RTOS** FreeRTOS:

- Under his control decides to start No Trusted OS (LINUX)

SLAVE

Details: Inter-World comm

Several methods available

OP - TEE

dualoscom

RPMsg

OpenAMP

**Based on
TOPPERS
Very specific
Too SW layers**

**Based on TI DSP
accepted on
mainline
Used by Xilinx in
AN
Very well
structured on
buffers and cache
handlings**

**Similar to RPMsg
Used on MPSoCs**

Details: Inter-World comm

Several methods available

OP - TEE

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RPMsg

OpenAMP

Selection Criterias

Details: The B00T process

Several methods available

OP - TEE

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RPMsg

OpenAMP

Selection Criterias

Acceptance into
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Details: The B00T process

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OP - TEE

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RPMsg

OpenAMP

Selection Criterias

Acceptance into
Mainline Linux Kernel

Control over the
isolation level between
the two worlds

Details: The B00T process

Several methods available

OP - TEE

dualoscom

RPMsg

OpenAMP

Selection Criterias

Acceptance into
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Maintenance – future
developments

Control over the
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RPMsg

OpenAMP

Selection Criterias

Acceptance into
Mainline Linux Kernel



Maintenance – future
developments

Control over the
isolation level between
the two worlds



The level of isolation is
application dependent

Details: The BOOT process

Several methods available

OP - TEE

dualoscom

RPMsg

OpenAMP

Selection Criterias

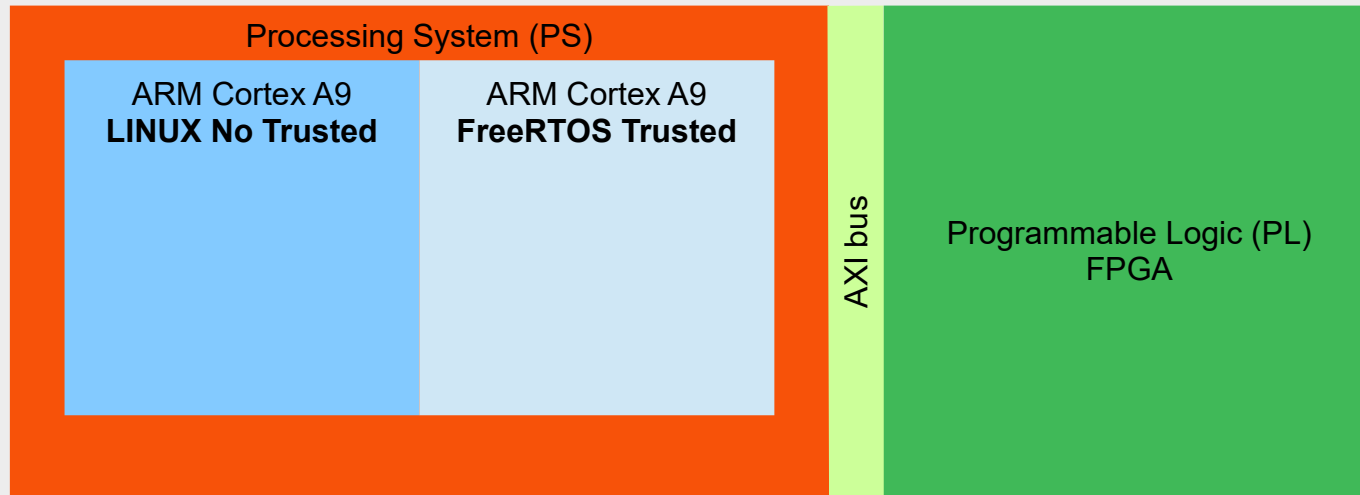
Acceptance into
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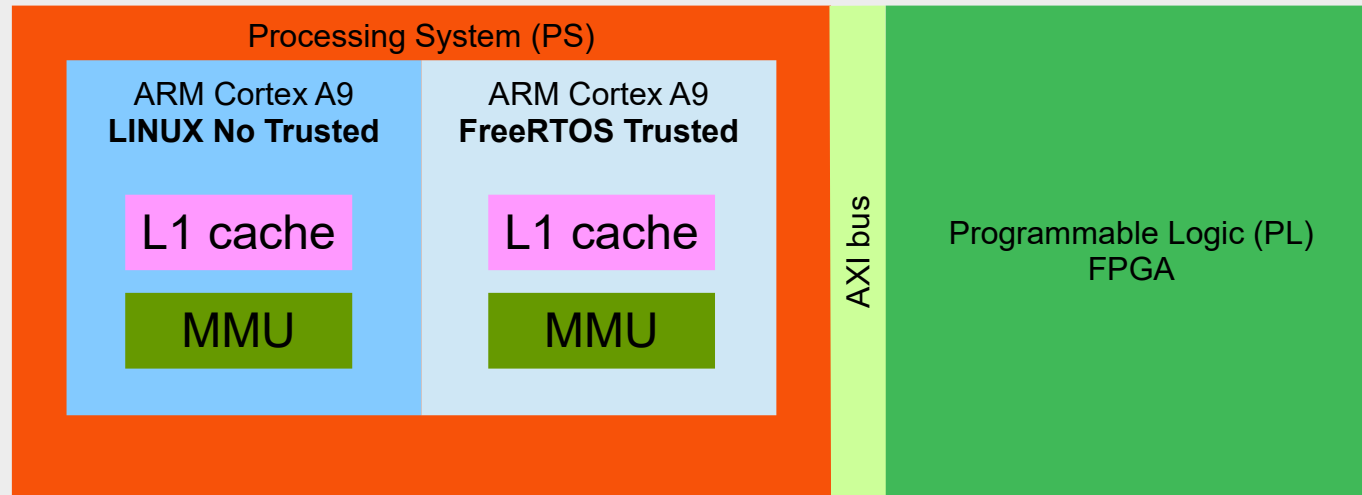
Control over the
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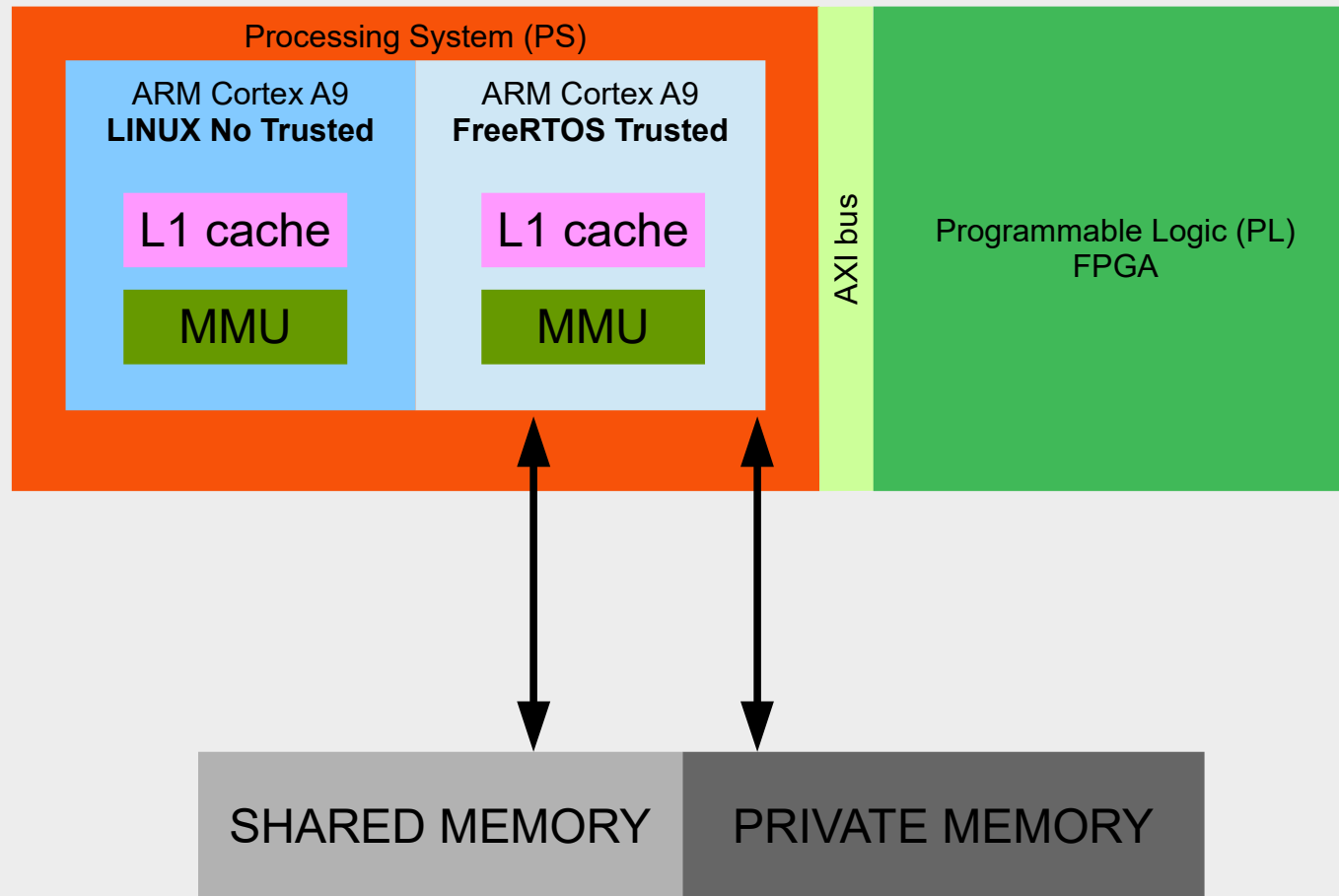
Details: L2 cache management



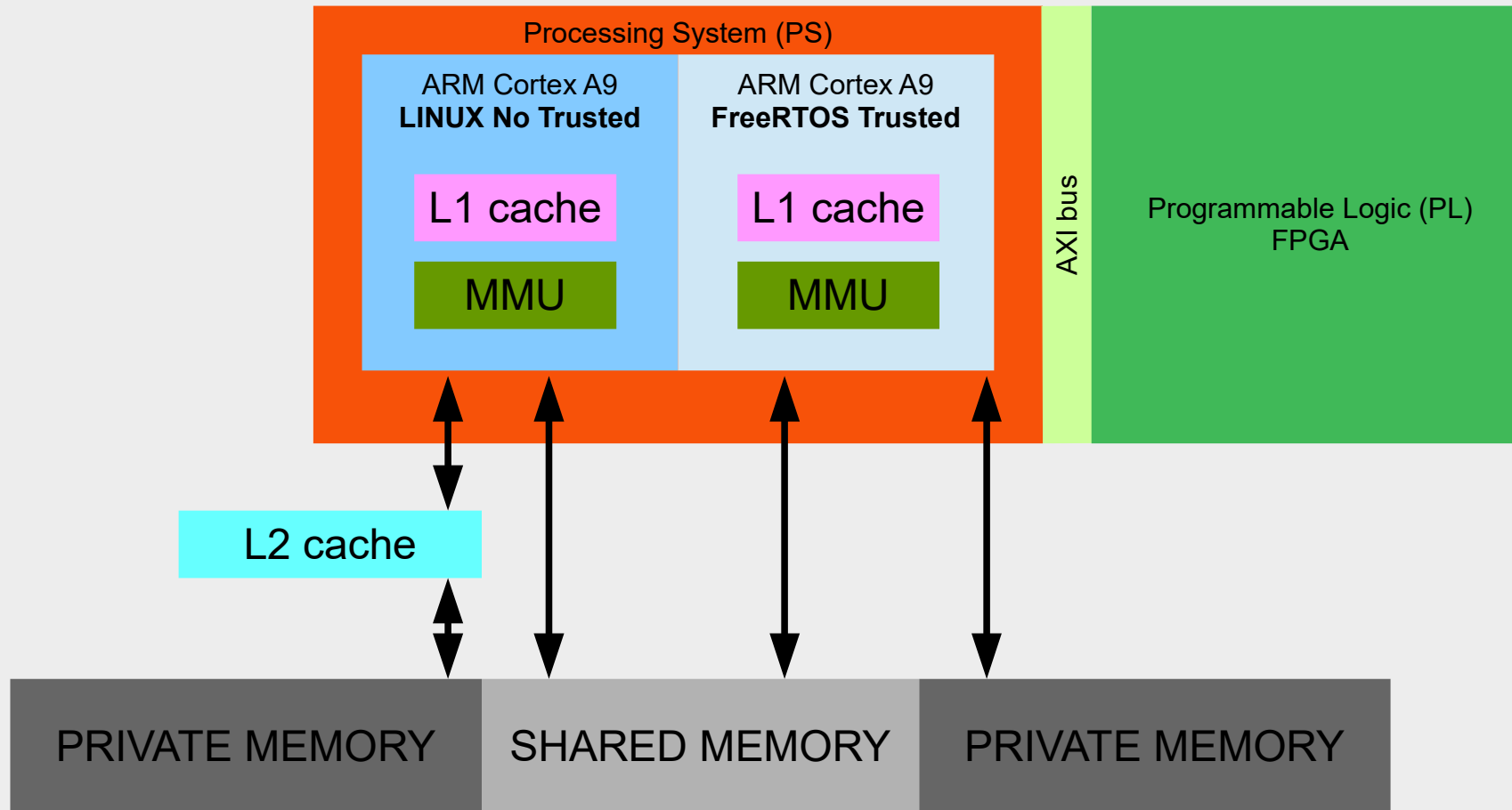
Details: L2 cache management



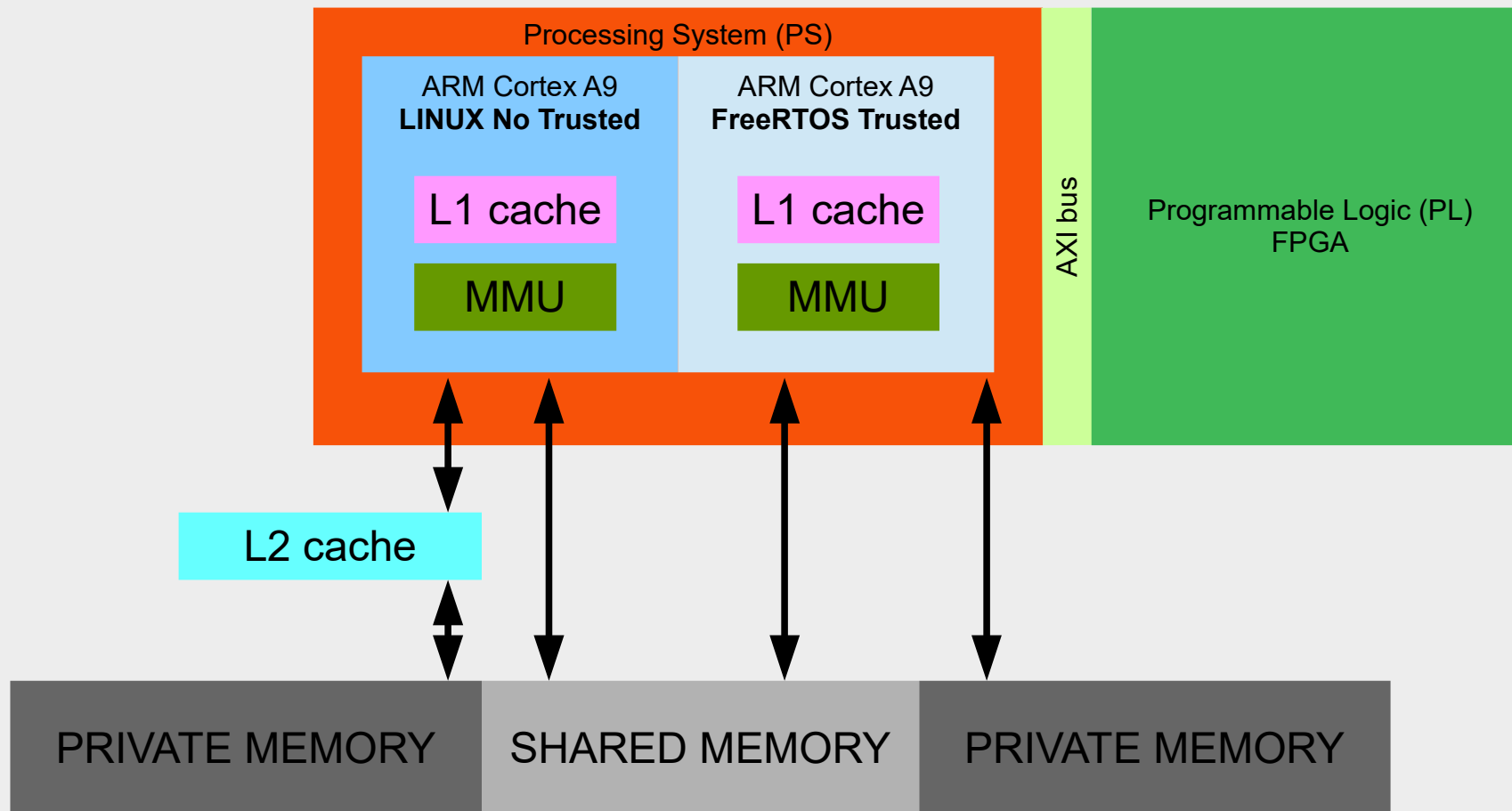
Details: L2 cache management



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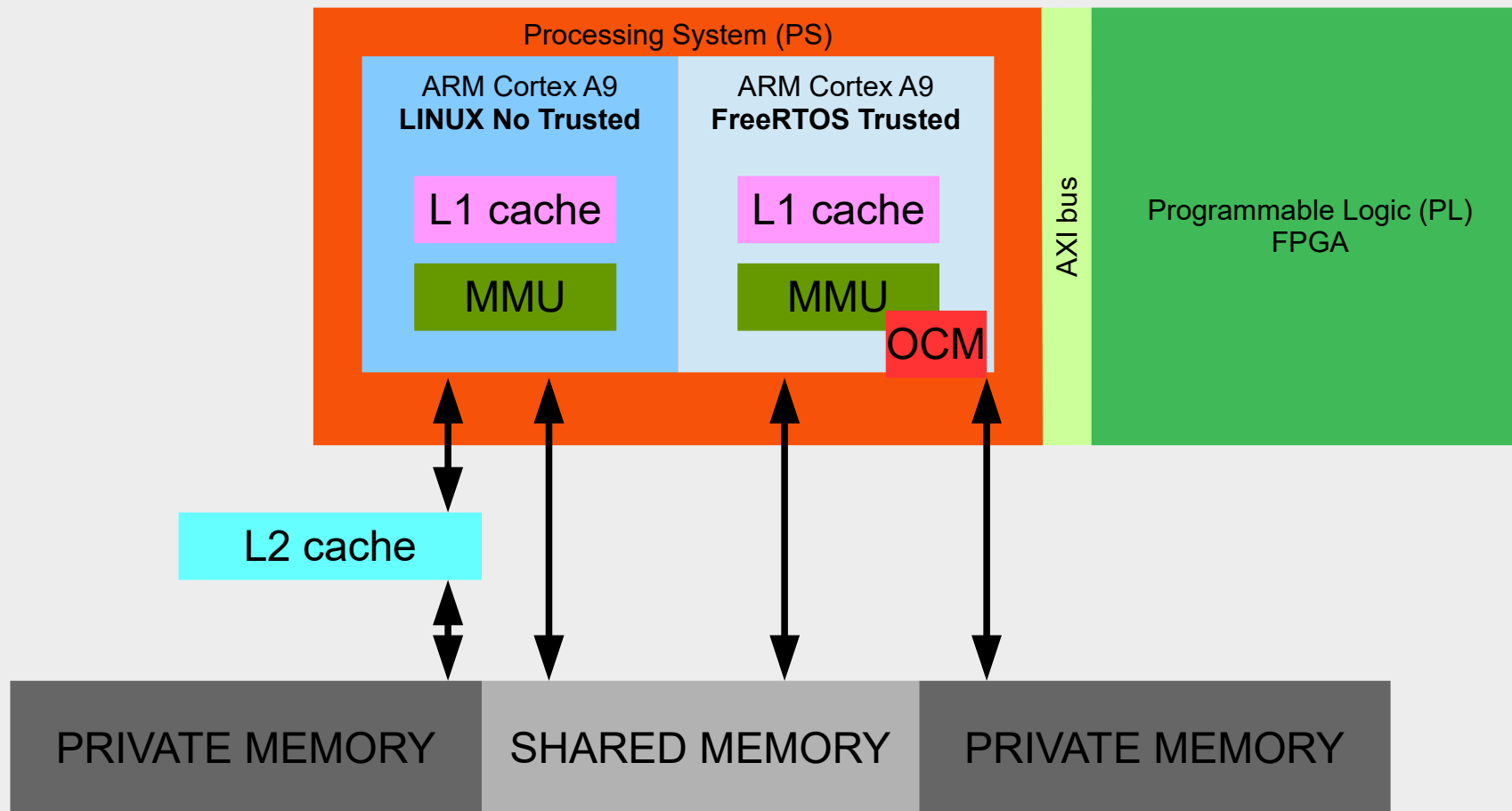


Details: L2 cache management



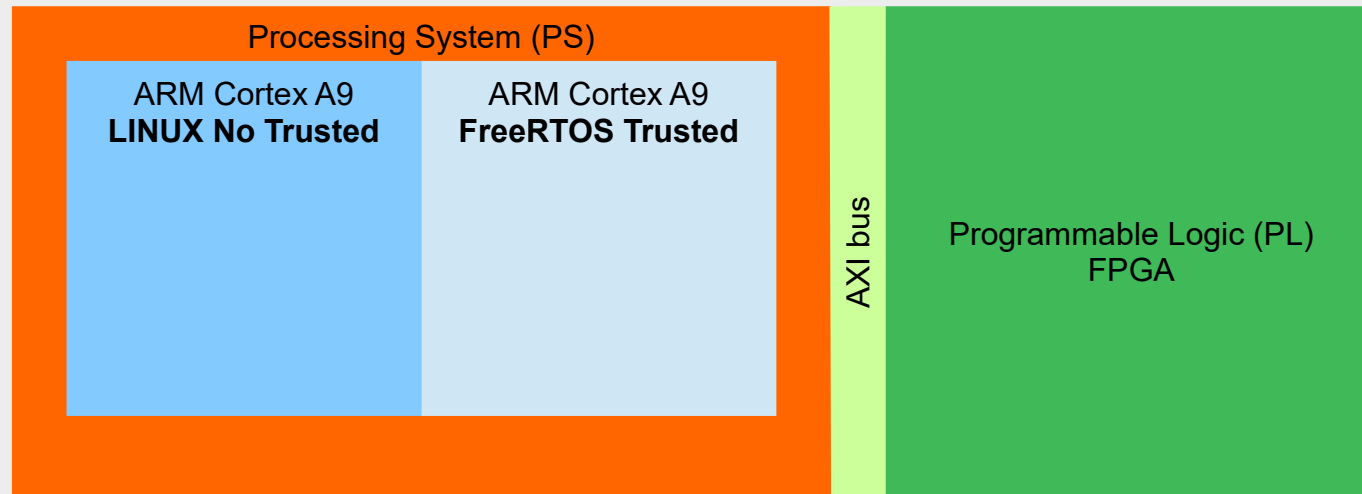
- Linux performances are not affected by dual OS solutions
- FreeRTOS determinism is granted
- Shared mem is not cached

Details: L2 cache management



- Linux performances are not affected by dual OS solutions
- FreeRTOS determinism is granted
- Shared mem is not cached
- Internal OCM can be granted only to Trust OS

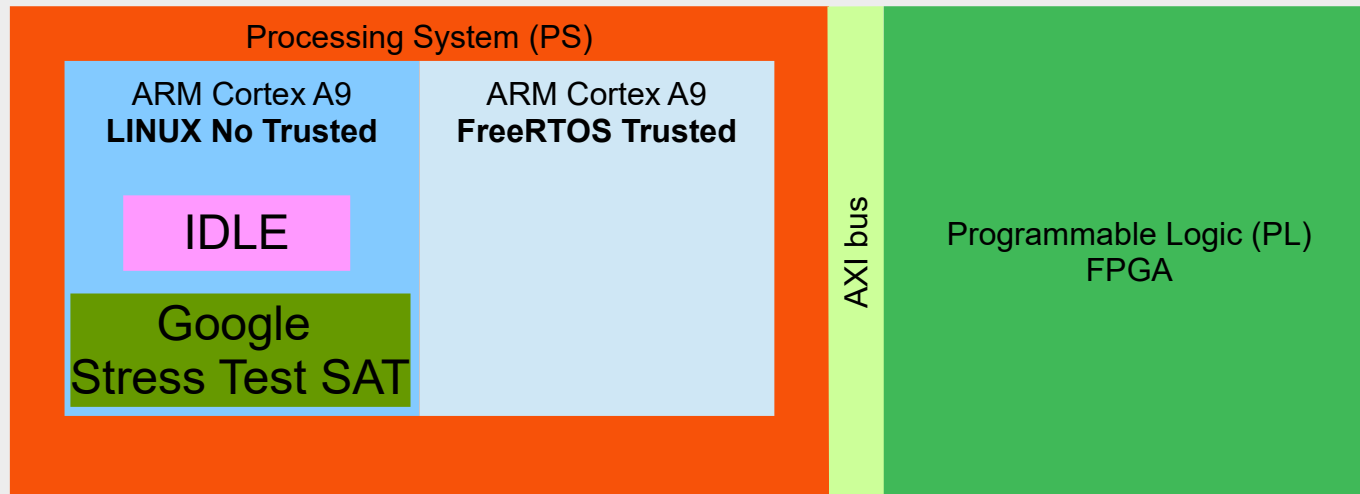
Details: Performances achieved



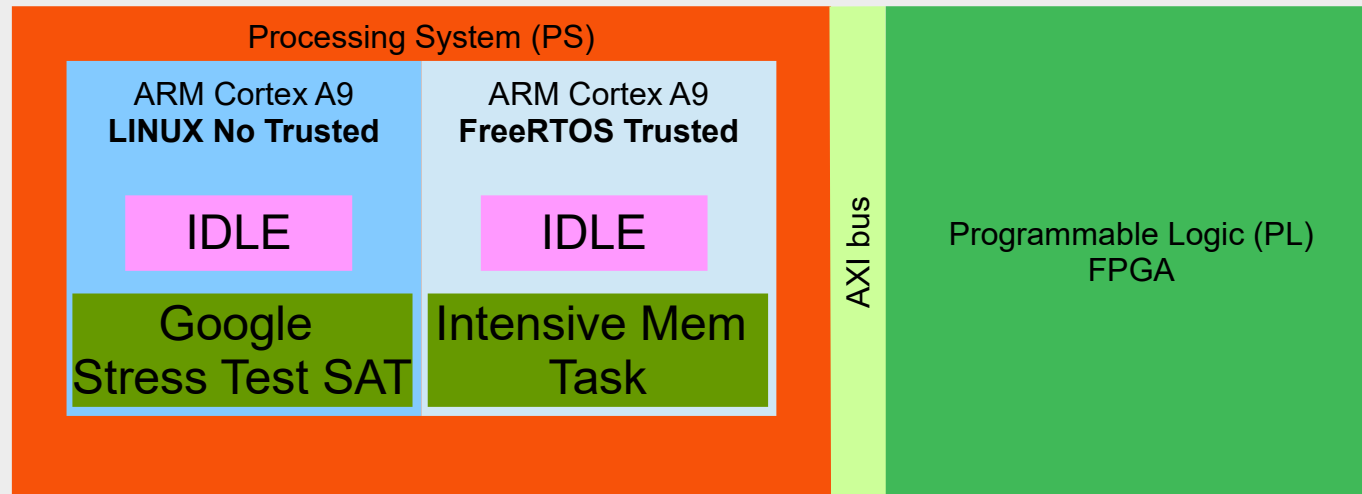
TEST BENCH: used the internal timer to measure the latency between:

- INT handling
- INT service

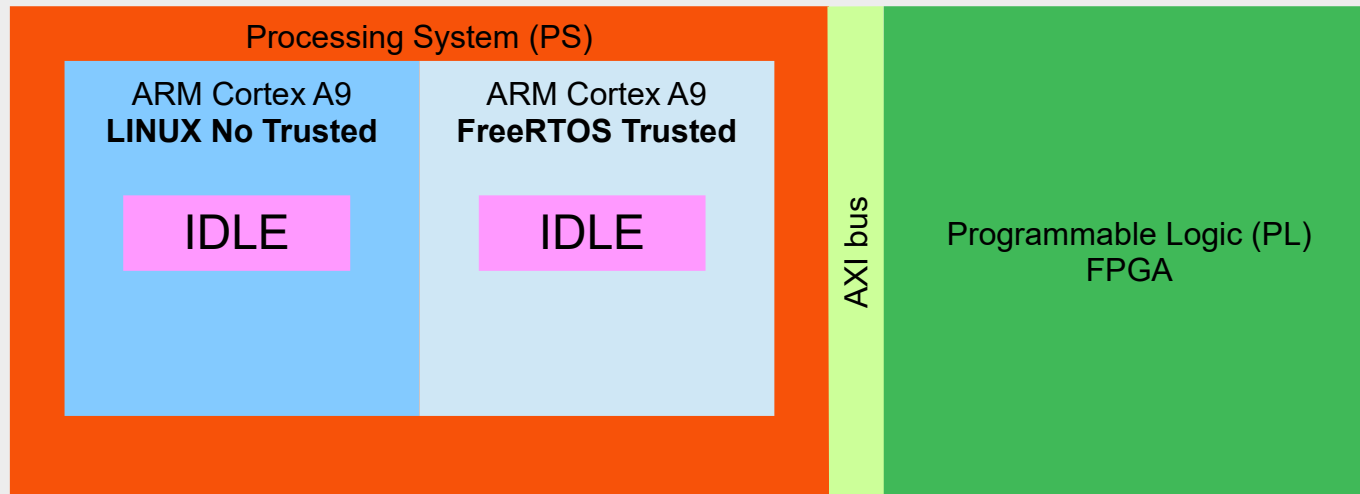
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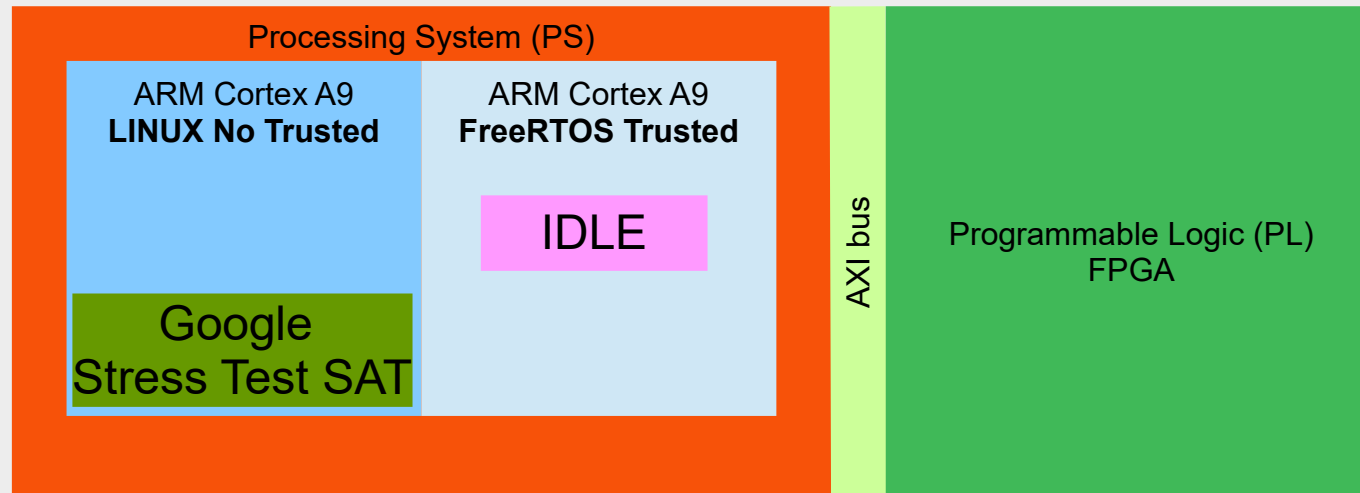


Details: Performances achieved



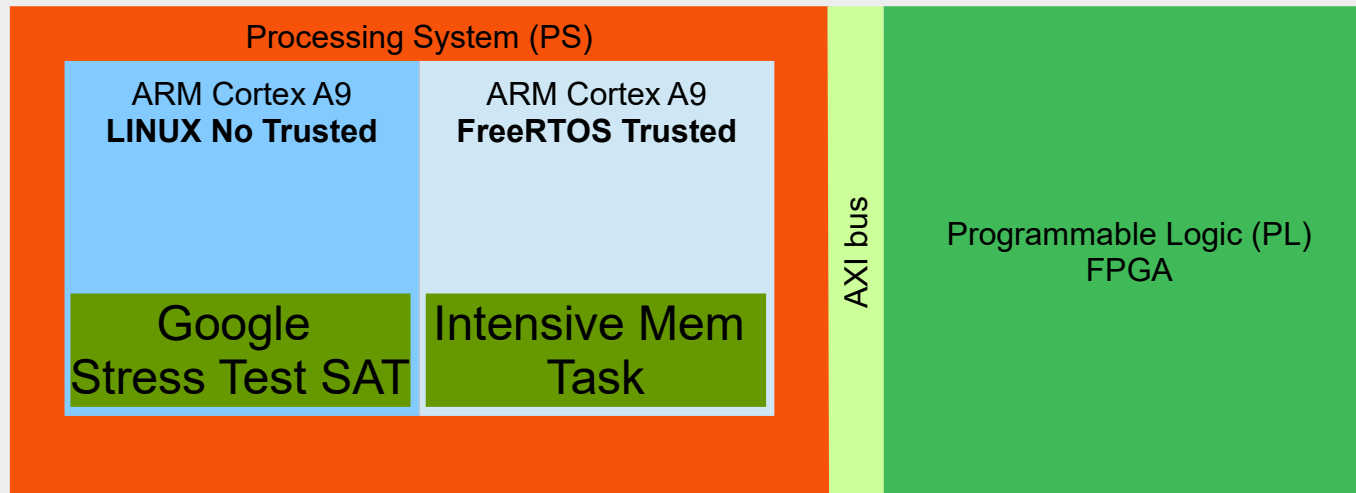
Latency	Linux IDLE RTOS IDLE	
min	287ns	
avg	287ns	
max	548ns	

Details: Performances achieved



Latency	Linux IDLE RTOS IDLE	LINUX SAT RTOS IDLE
min	287ns	287ns
avg	287ns	296ns
max	548ns	539ns

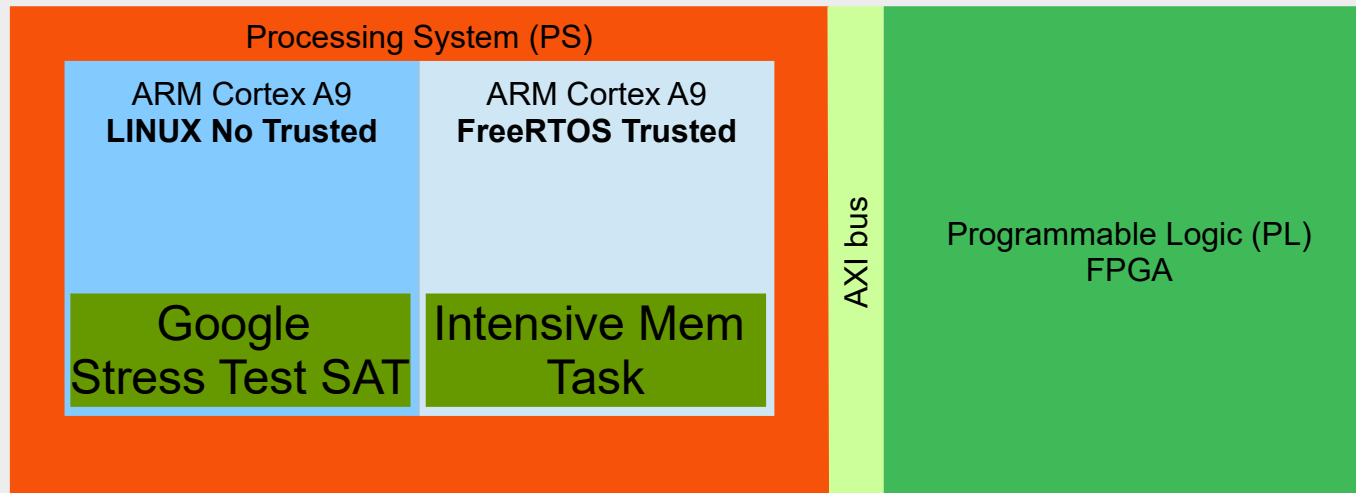
Details: Performances achieved



Latency	Linux IDLE RTOS IDLE	LINUX SAT RTOS IDLE	LINUX SAT RTOS 16k task load
min	287ns	287ns	287ns
avg	287ns	296ns	205ns
max	548ns	539ns	575ns

- Linux performances not affect RTOS in any condition
- FreeRTOS latency is granted with not heavy load tasks

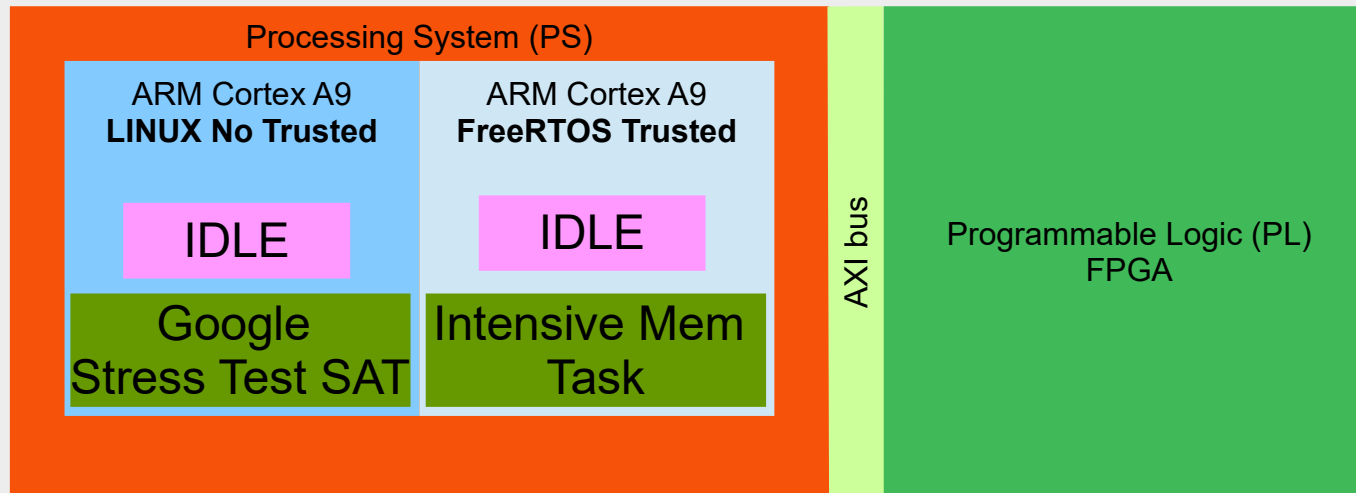
Details: Performances achieved



Latency	Linux IDLE RTOS IDLE	LINUX SAT RTOS IDLE	LINUX SAT RTOS 16k task load	LINUX SAT RTOS 128k task load
min	287ns	287ns	287ns	1268ns
avg	287ns	296ns	205ns	2024ns
max	548ns	539ns	575ns	3050ns

- Linux performances not affect RTOS in any condition
- FreeRTOS latency is granted with not heavy load tasks
- FreeRTos is affected by high mem loads due to it is not cached

Details: Performances achieved



Latency	Linux IDLE RTOS IDLE	LINUX SAT RTOS IDLE	LINUX SAT RTOS 16k task load	LINUX SAT RTOS 128k task load
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- Linux performances not affect RTOS in any condition
- FreeRTOS latency is granted with not heavy load tasks
- FreeRTos is affected by high mem loads due to it is not cached

The L2 cache can be also used only on Trust OS – there are pro and cons (typically a determinism reduction is noted)

Future works and references

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- Complete Reboot of Slave core from Master Core

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- Deep understanding and optimization of INTerrupt handling and communication data interchange between two worlds related to determinism and latency aspects

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- Deep understanding and optimization of INTerrupt handling and communication data interchange between two worlds related to determinism and latency aspects

- Refers to:

<http://www.dave.eu/sites/default/files/BRX-WP001.pdf>

Yashu Gosain and Prushothaman Palanichamy, Xilinx
WP429 - TrustZone Technology Support in Zynq-7000 All
Programmable SoCs (v1.0), May 20, 2014

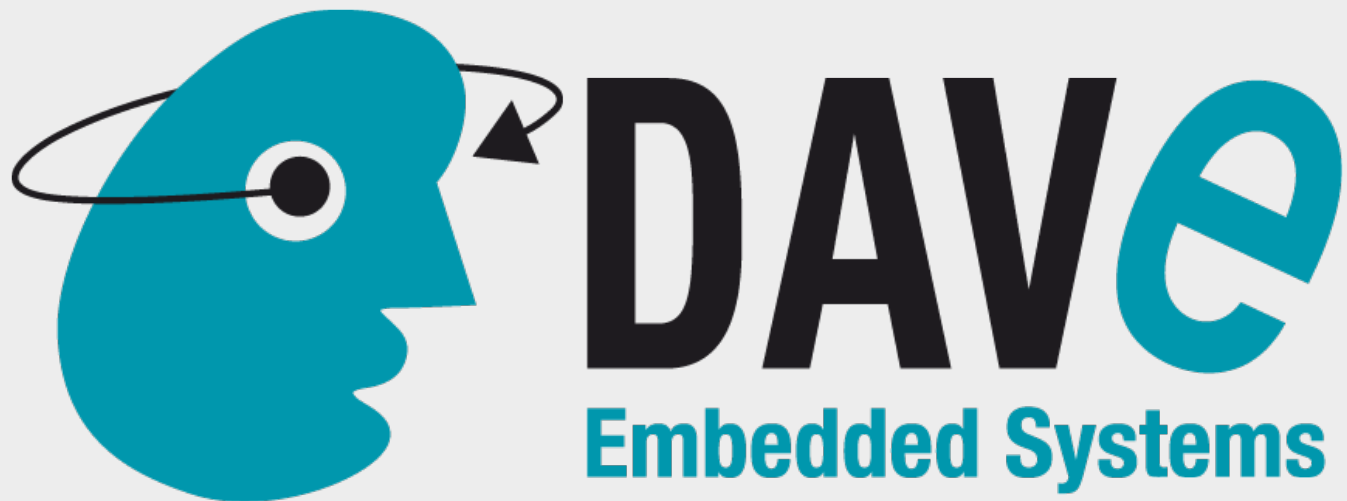
DAVE Embedded Systems, AN-BELK-001: Asymmetric
Multiprocessing (AMP) on Bora – Linux FreeRTOS, -
TOPPERS SafeG home page (English), -

<https://www.toppers.jp/en/safeg.html>

and many others

Question and answers





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