CORE | Vision
NEXT LEVEL EMBEDDED DEVELOPMENT

Designing a Multi-Processor based system with FPGAs

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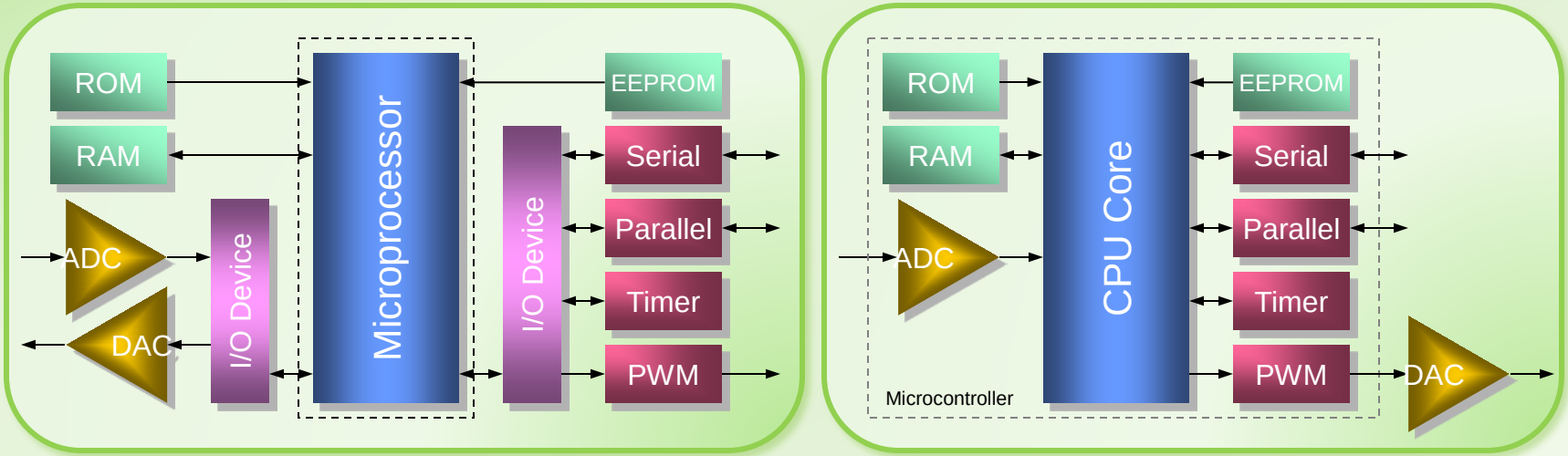
Why Use Processors ?

- Microcontrollers (µC) and microprocessors (µP) provide a higher level of design abstraction
  - Most µC functions can be implemented using VHDL or Verilog
    - Downsides are parallelism & complexity
  - Using C/C++ abstraction & serial execution make certain functions much easier to implement in a µC
- Discrete µCs are inexpensive and widely used
  - µCs have years of momentum and software designers have vast experience using them

µP versus µC

- A microprocessor (µP) is just one component of many in a ***complex system*** of digital & analog I/O



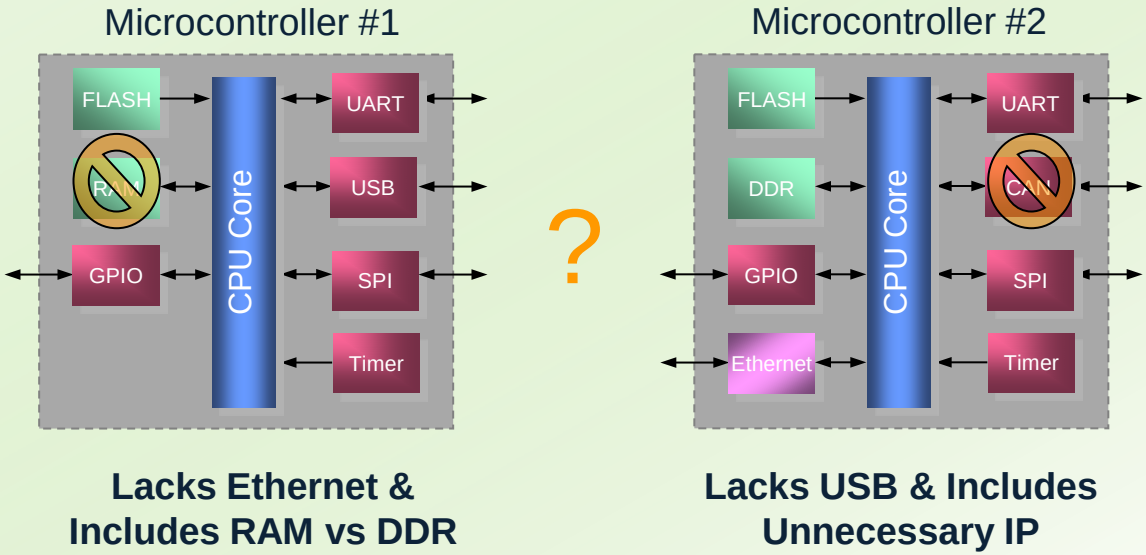
- Most ***simple system*** components are contained completely within a microcontroller (µC)

Rarely the Ideal Mix

- **Difficult to find the required mix of peripherals in Off the Shelf (OTS) microcontroller solutions**

Today System Requirements

- UART
- USB
- TIMER
- Ethernet
- SPI
- GPIO
- FLASH
- DDR



Lacks Ethernet & Includes RAM vs DDR

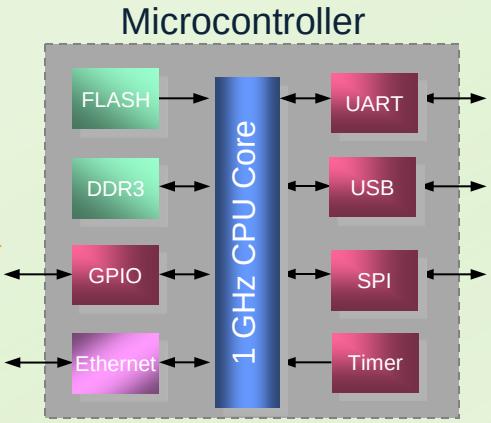
Lacks USB & Includes Unnecessary IP

Changing Requirements

- **Difficult to find the required mix of peripherals in Off the Shelf (OTS) microcontroller solutions**
- **Selecting a single processor core with long term solution viability is difficult at best**

Todays System Requirements

- 1 GHz
- UART
- USB
- TIMER
- 10/100 Ethernet
- SPI
- GPIO
- FLASH
- DDR3



Meets current system requirements

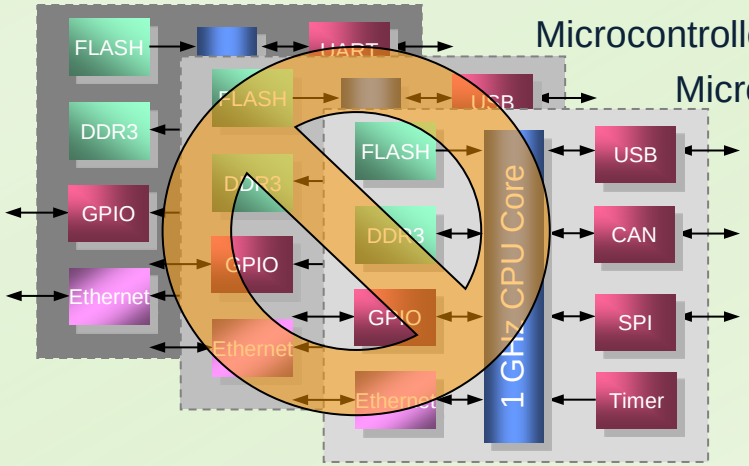
Future System Requirements

- 2.4 GHz
- UART
- USB
- TIMER
- 10/ 100/1000 Ethernet
- SPI
- GPIO
- FLASH
- DDR4

?

Here Today, Gone Tomorrow

- **Difficult to find the required mix of peripherals in Off the Shelf (OTS) microcontroller solutions**
- **Selecting a single processor core with long term solution viability is difficult at best**
- **Without direct ownership of the processing solution, obsolescence is always a concern**



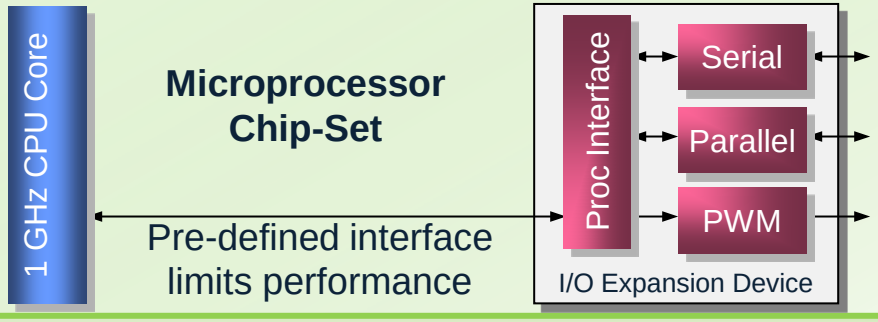
Microcontroller #1 - Low Volume Niche

Microcontroller #2 – Moderate Volume

Microcontroller #3 – High Volume Automotive

Chipset Solutions

- Difficult to find the required mix of peripherals in Off the Shelf (OTS) microcontroller solutions
- Selecting a single processor core with long term solution viability is difficult at best
- Without direct ownership of the processing solution, obsolescence is always a concern
- Many microprocessor based solutions provide limited On-Chip peripheral support



Embedded Design with FPGAs

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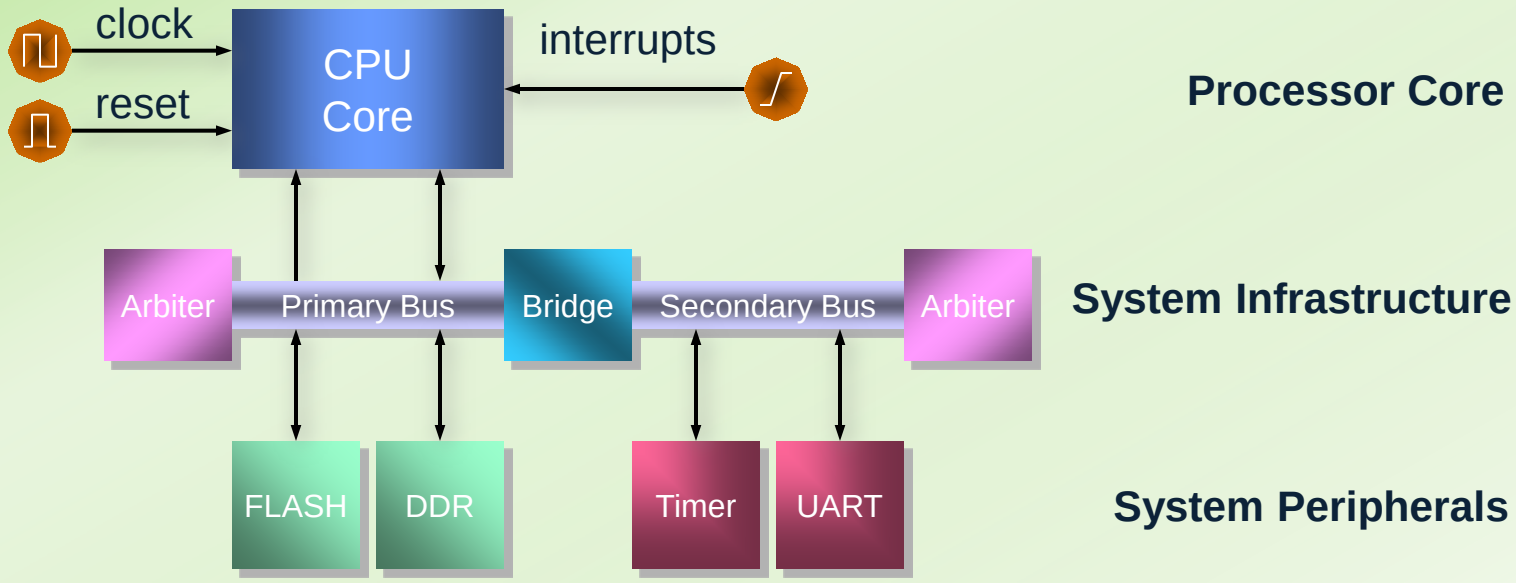
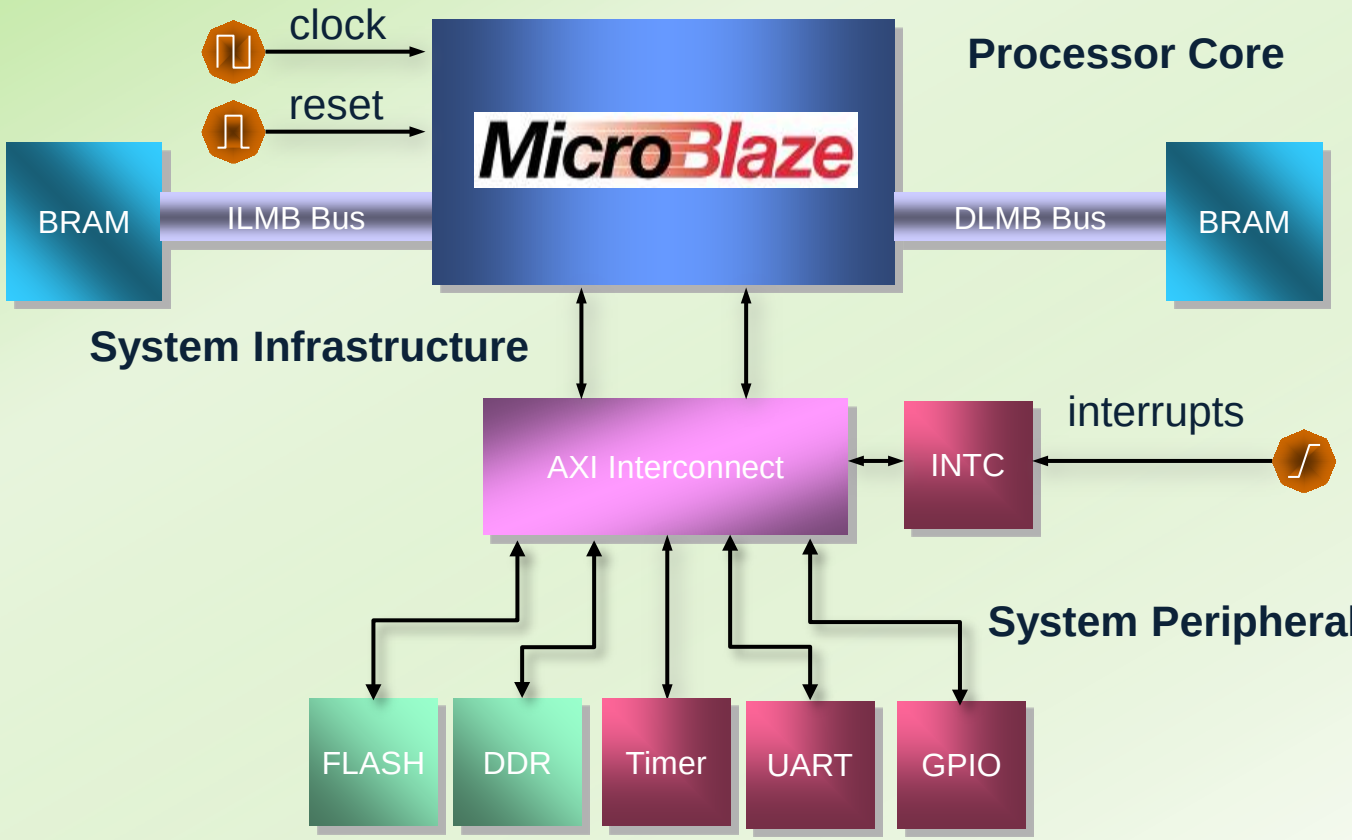
- FPGA allow for the implementation of an ideal mix of peripherals and system infrastructure
- New system requirements can be supported without changing the processor core
- Longevity of FPGAs approaches the longest available microcontrollers in the market
- FPGAs are used to augment µP functionality absorbing the core is the next natural step

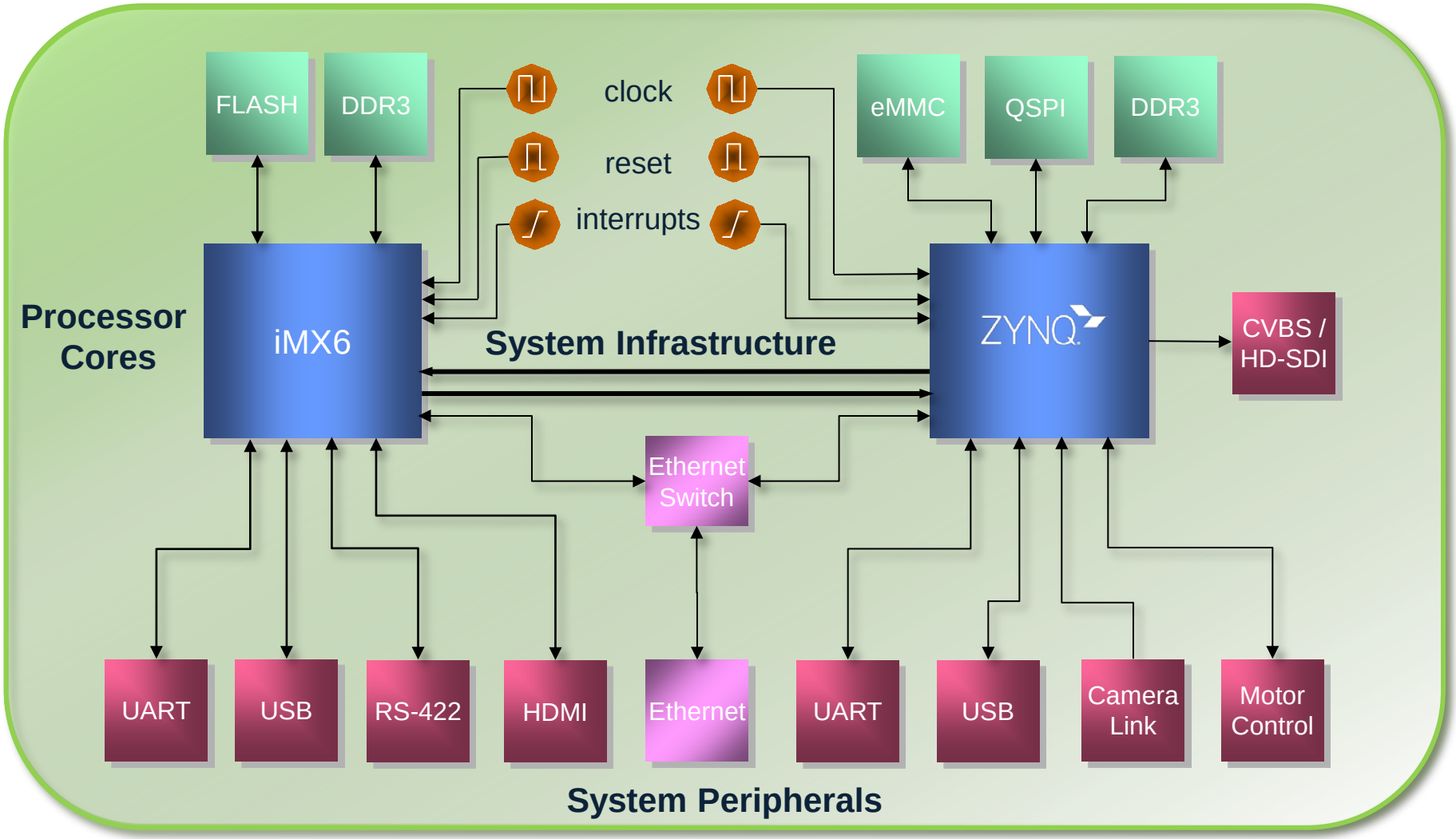
Simple Processor System



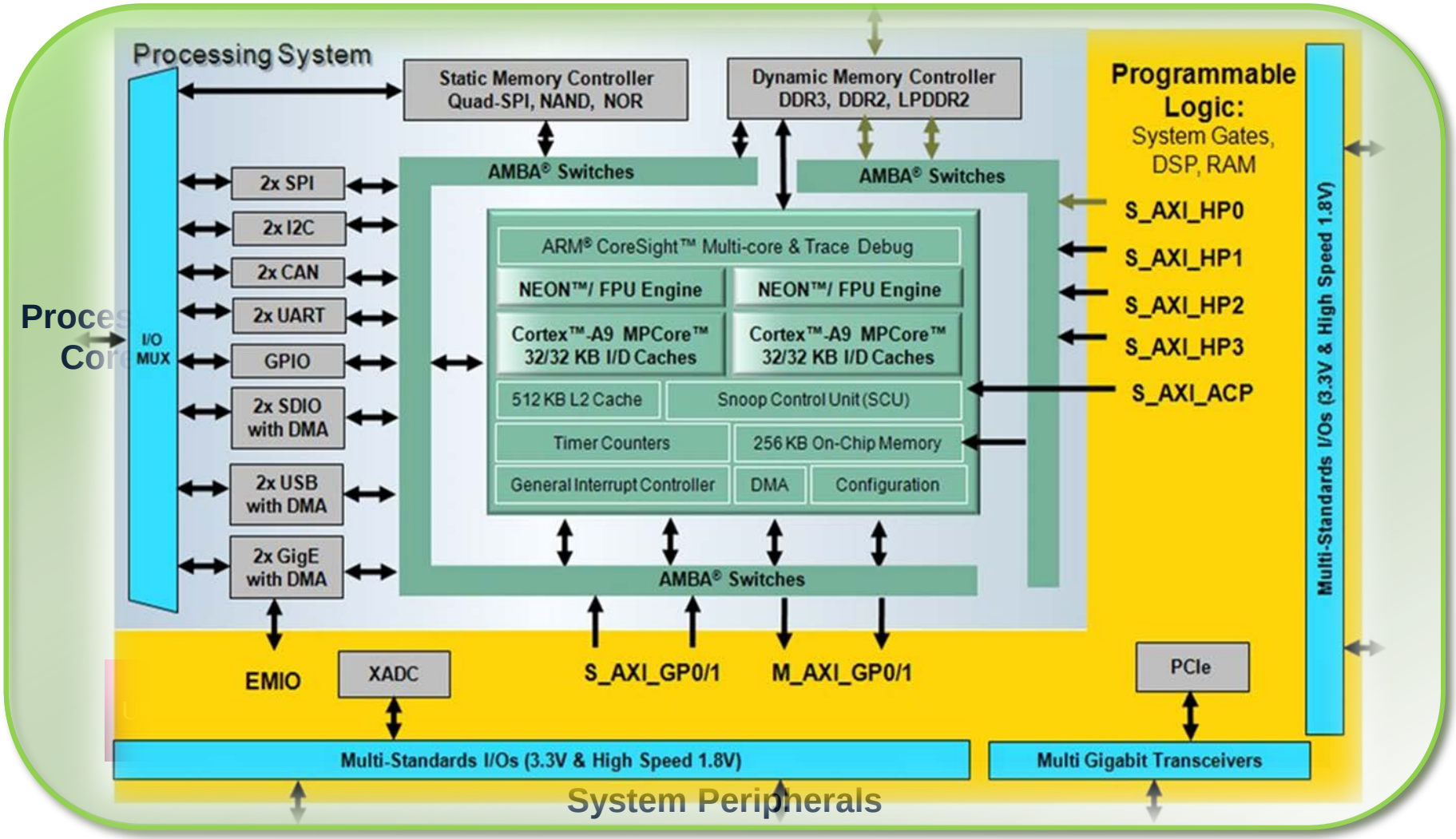
Softcore Processor System



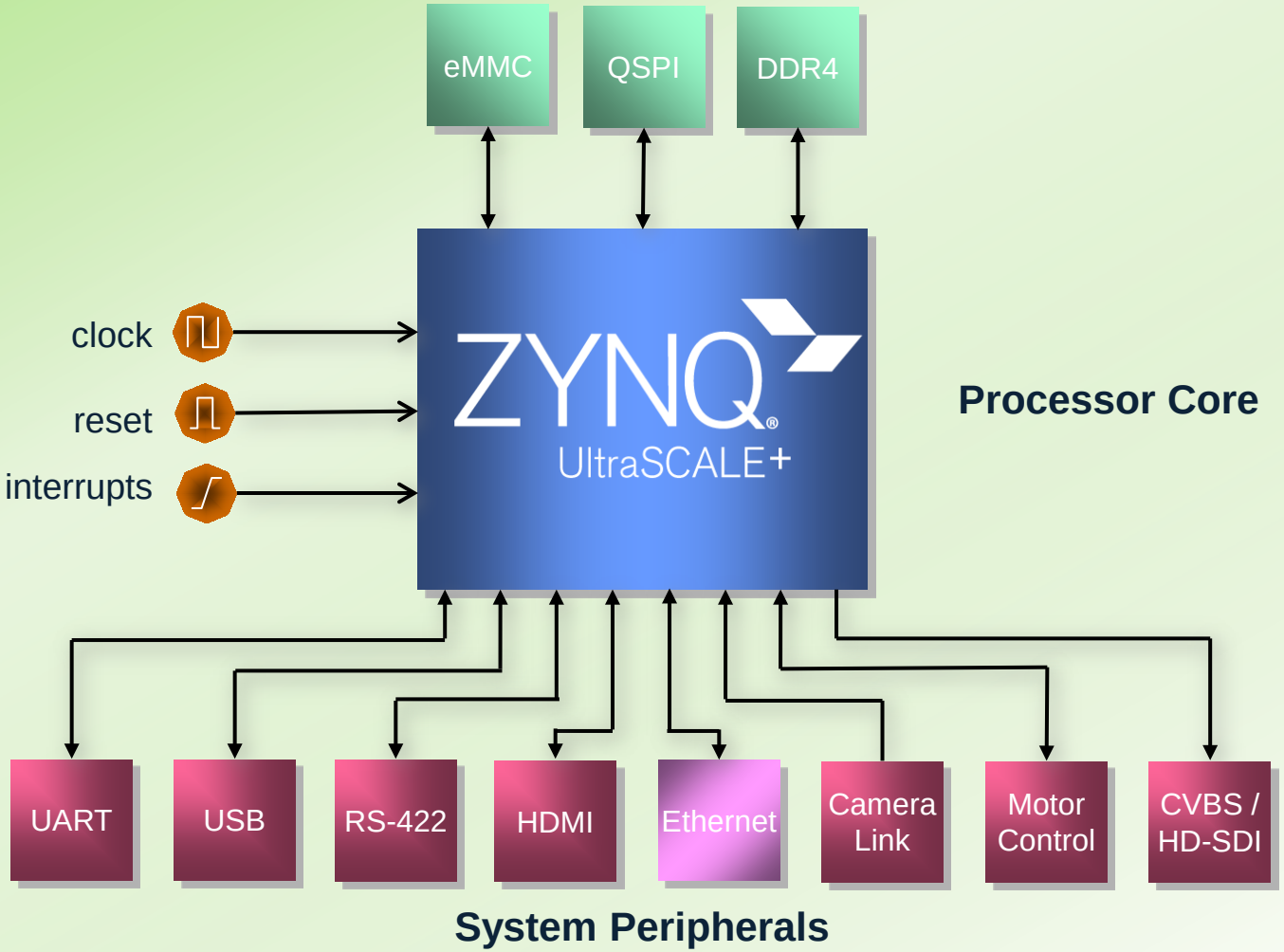
Hybrid Processor System



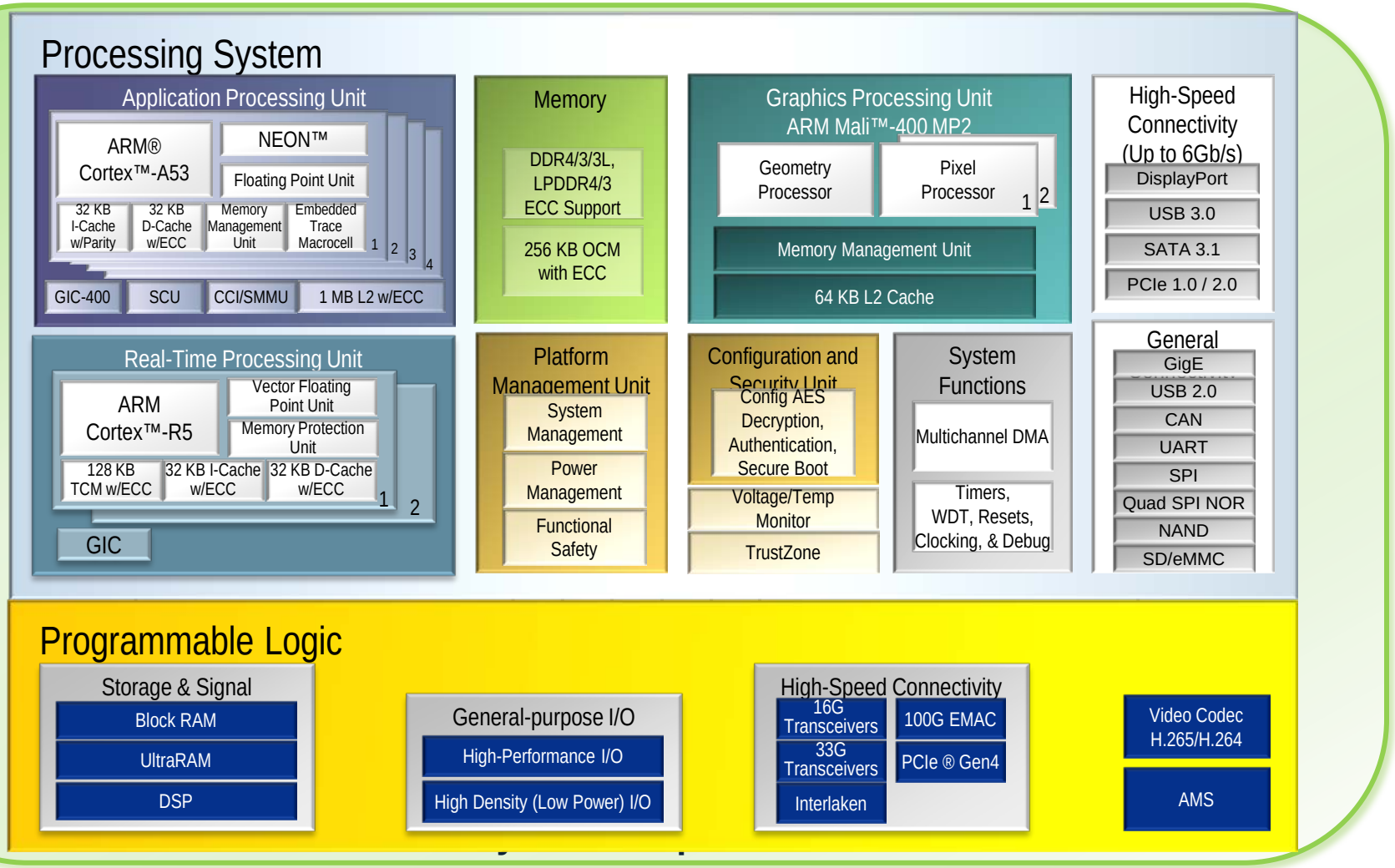
Hybrid Processor System



FPGA based Processor System

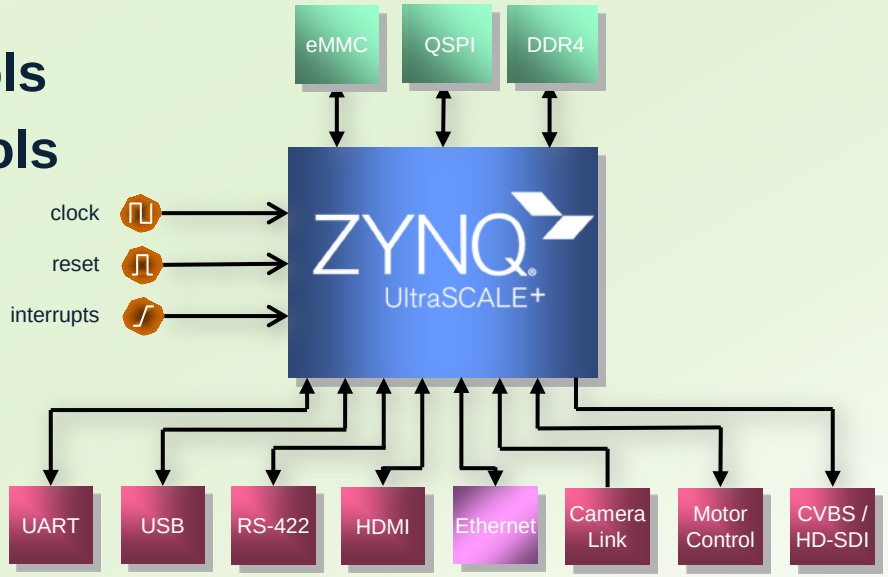


FPGA based Processor System



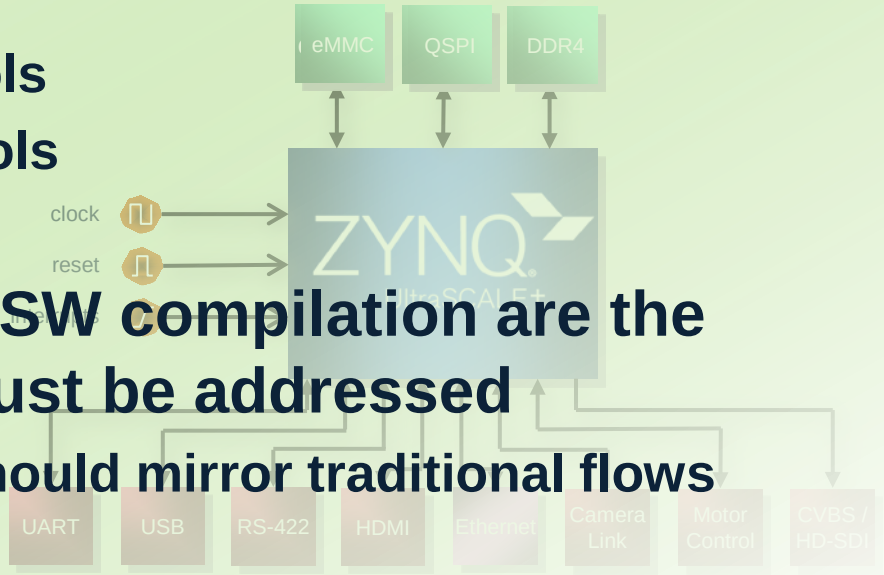
Necessary Tools

- A full complement of tools are required to design an embedded processor system
  - Processor system generation
  - Hardware implementation tools
  - Software compilers
  - Hardware debugger tools
  - Software debugging tools

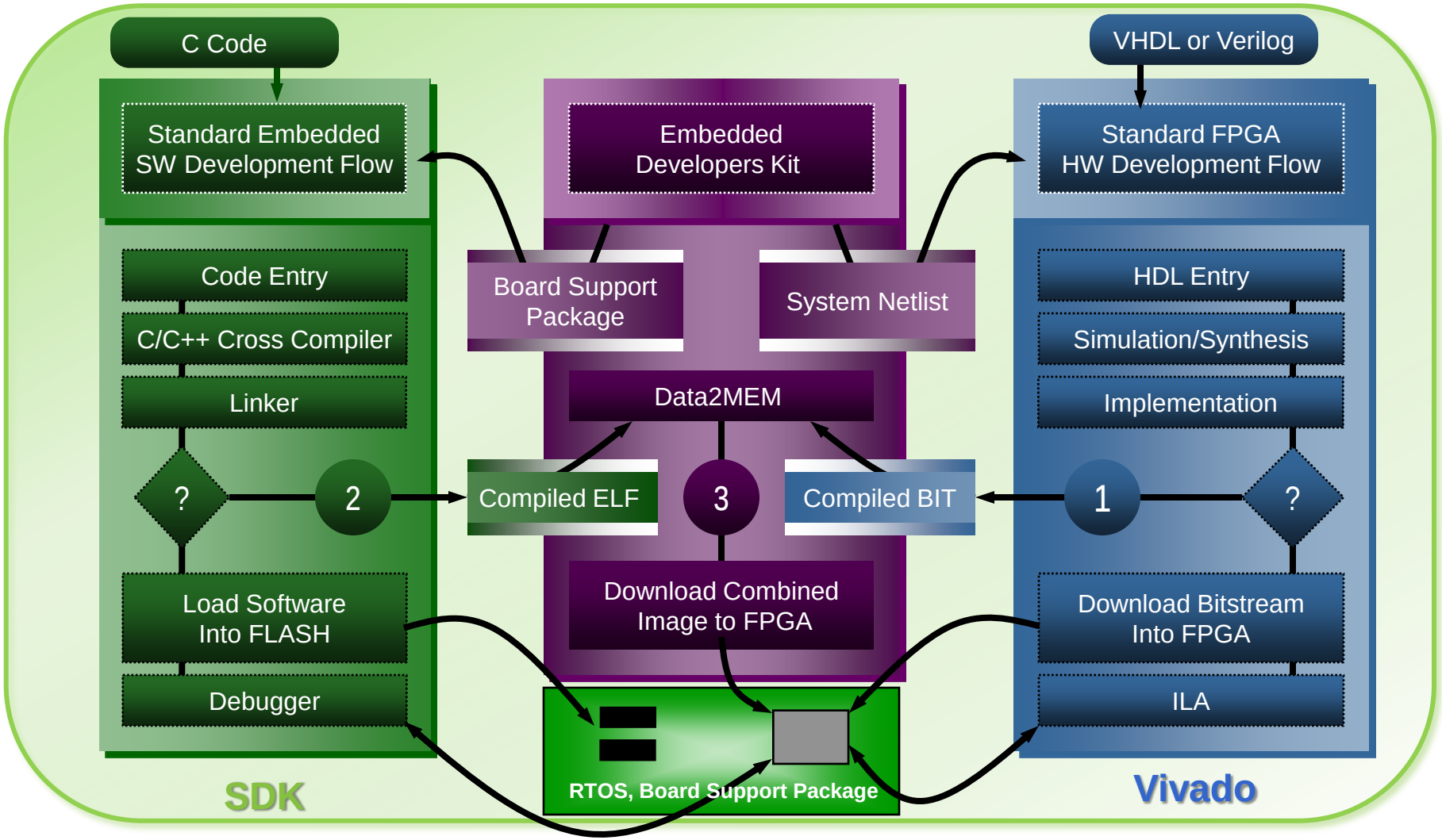


Necessary Tools

- A full complement of tools are required to design an embedded processor system
  - Processor system generation
  - Hardware implementation tools
  - Software compilers
  - Hardware debugger tools
  - Software debugging tools
- HW implementation & SW compilation are the two main flows that must be addressed
  - The embedded flows should mirror traditional flows

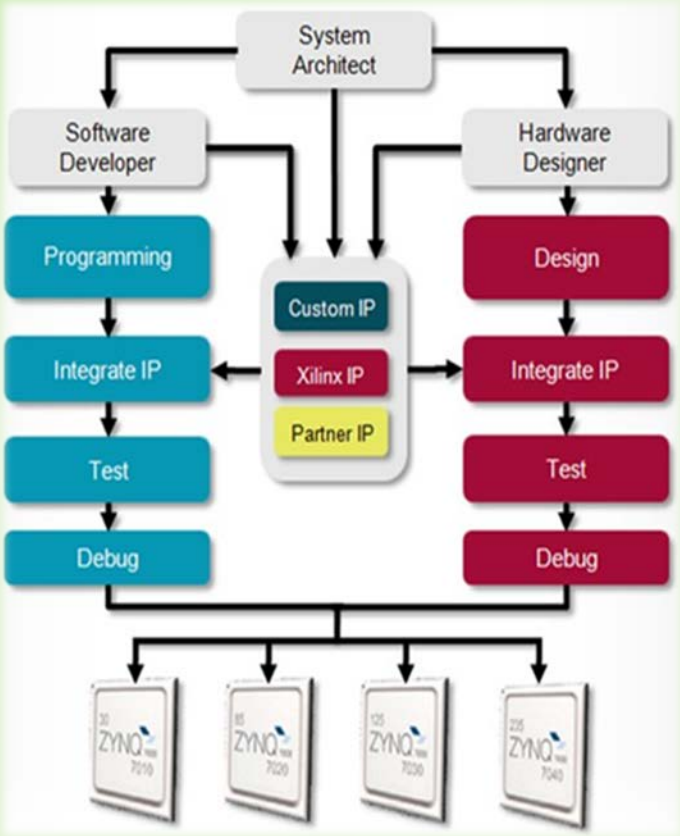


Traditional Embedded Design Flow



Design Flow and Tools

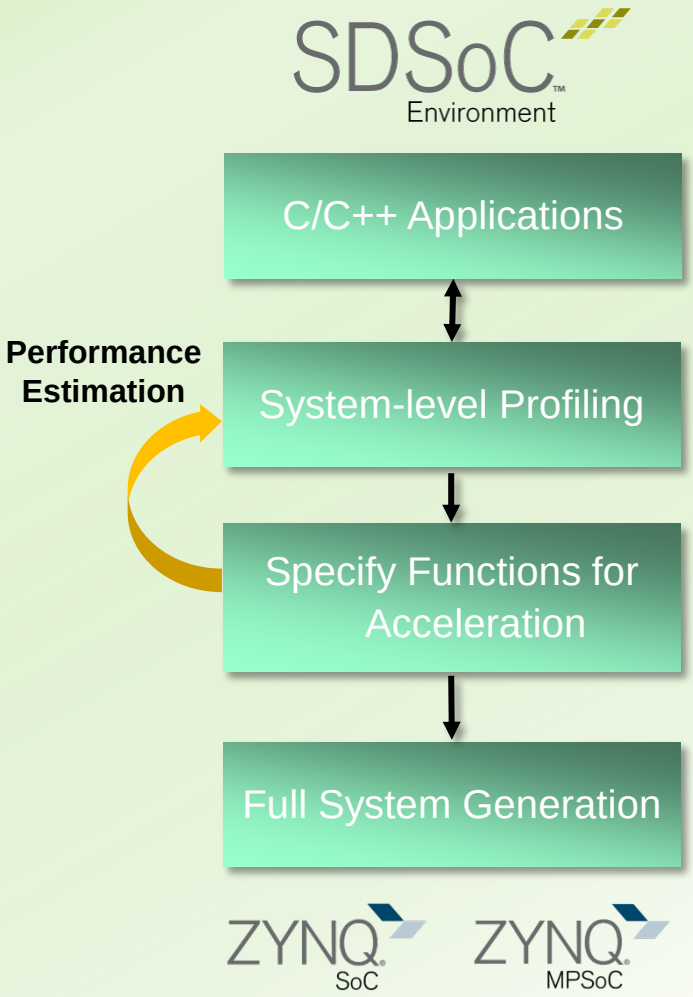
- **Software**
  - Real-time OS
  - Drivers
  - APIs
  - …
- **Tools**
  - Vivado SDK
  - Matlab
  - SDSoC
  - …



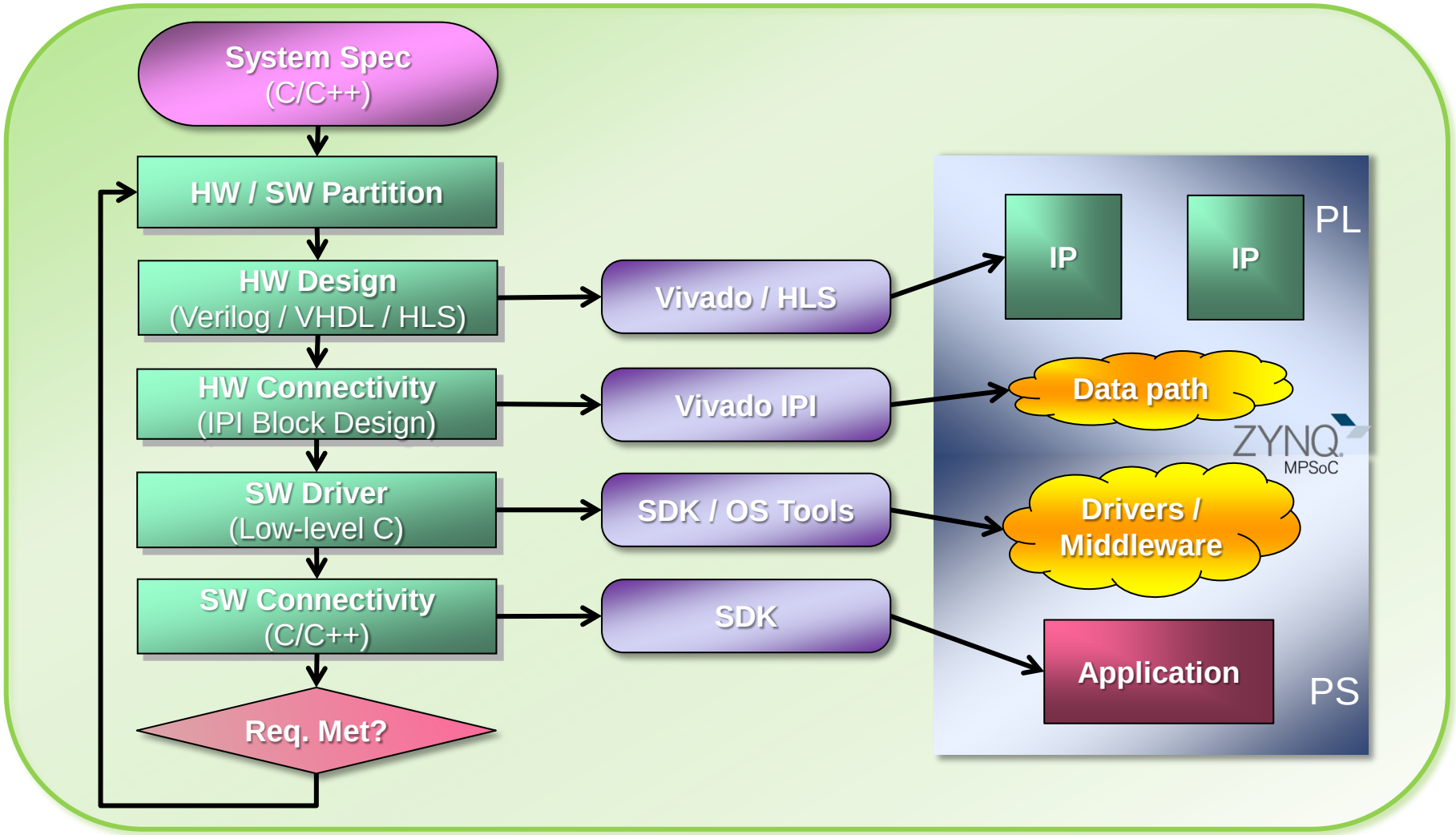
- **FPGA hardware**
  - Spartan - Artix
  - Kintex - Virtex
  - Zynq
    - 7000 - 7000S
  - Zynq UltraSCALE+
    - Dual A53 / Dual R5
    - Quad A53 / Dual R5 / Codec
    - Quad A53 / Dual R5 / GPU
- **Tools**
  - Vivado HLx
  - Matlab
  - …

Embedded Design Flow with SDSoC

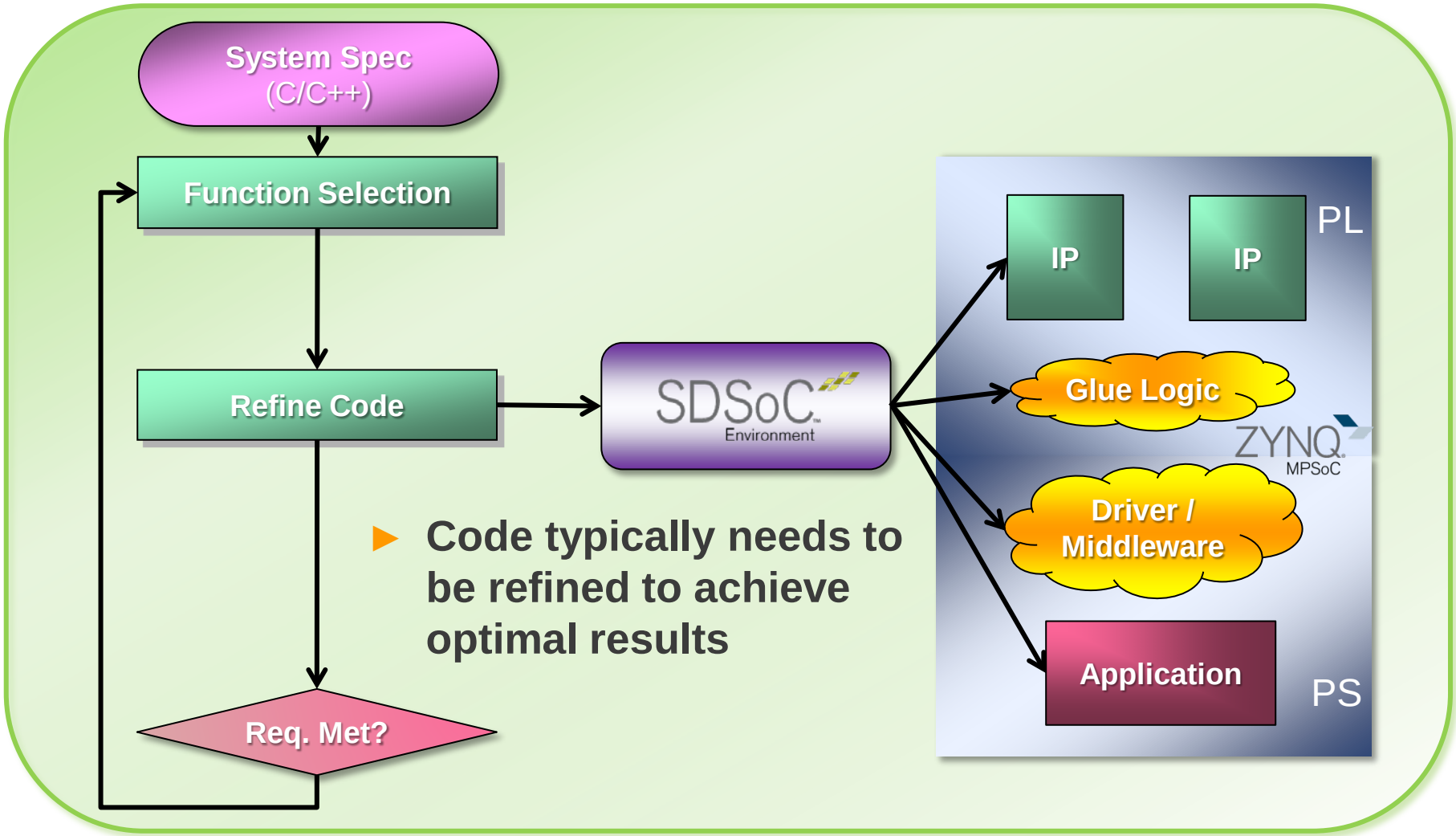
- Migrate C/C++ functions to hardware
- System-level debug and profile
- Simple hardware-software partitioning
- Full system generation including driver and hardware connectivity



Design Flow without SDSoC



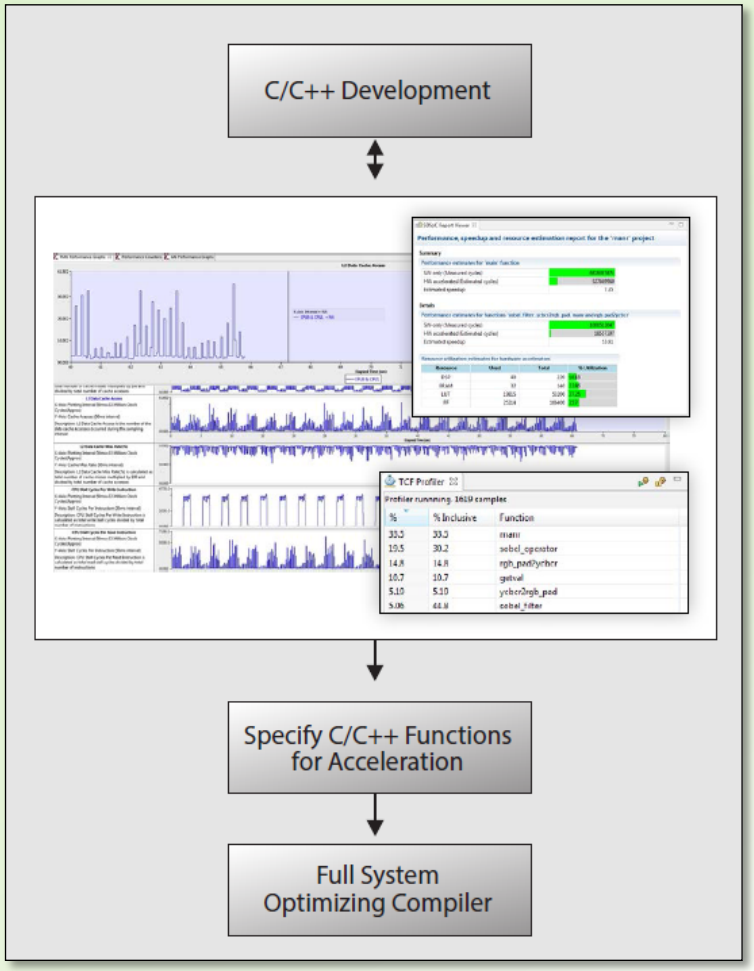
Design Flow with SDSoC



- Code typically needs to be refined to achieve optimal results

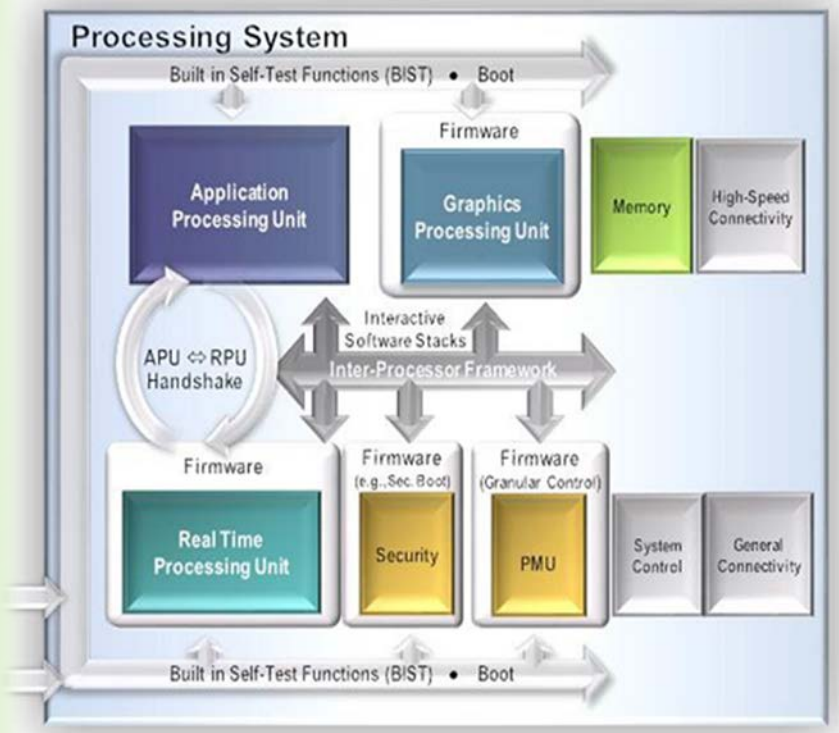
SDSoC System Level Profiling

- **Rapid system performance estimation**
  - **Full system estimation (programmable logic, data communication, processing system)**
  - **Reports SW/HW cycle level performance and hardware utilization**
- **Automated performance measurement**
  - **Runtime measurement by instrumentation of cache, memory, and bus utilization**



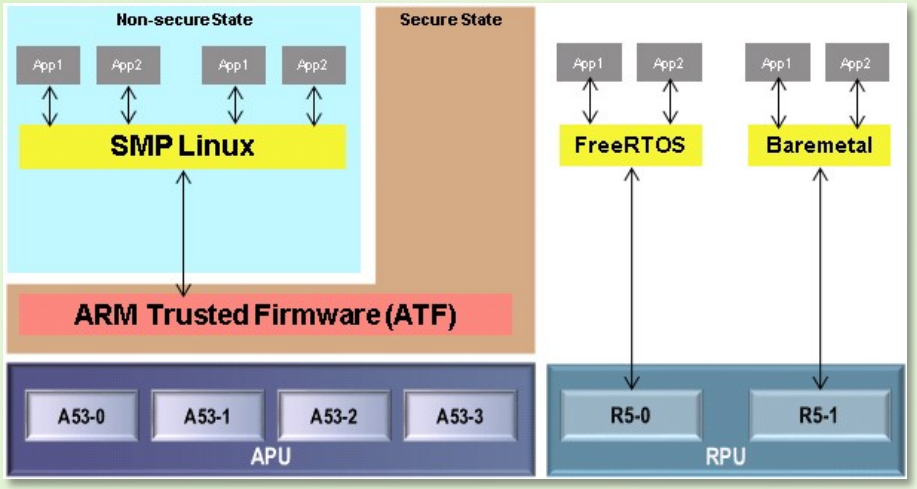
MPSoC HW/SW Considerations

- Quad-core ARM Cortex-A53
- Dual-core ARM R5
- ARM Mail-400MP GPU
- DDRx and SMC controllers
- Security firmware
- Platform Management Unit
- FSBL, uBoot
- ARM trusted firmware
- XEN hypervisor
- Software test libraries
- Inter-processor Framework
- Multi-OS boot image



Example Default Configuration: APU-Linux / RPU

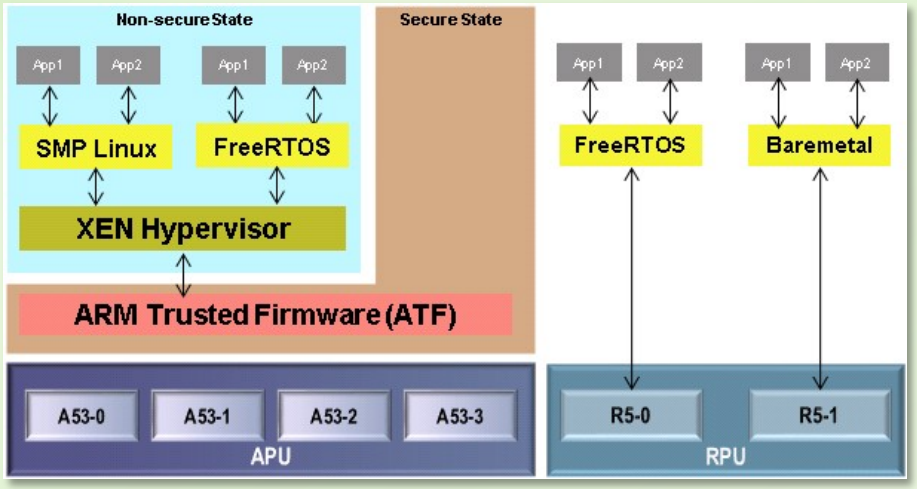
- System software
  - FSBL: First Stage Boot Loader
  - uBoot: Open source



- APU: Non-secure mode
  - ARM trusted firmware: From Xilinx, verified on APU
  - SMP Linux
  - No hypervisor: Non-secure mode
- RPU
  - In split mode (default)
  - R5-0: FreeRTOS
  - R5-1: Bare-metal

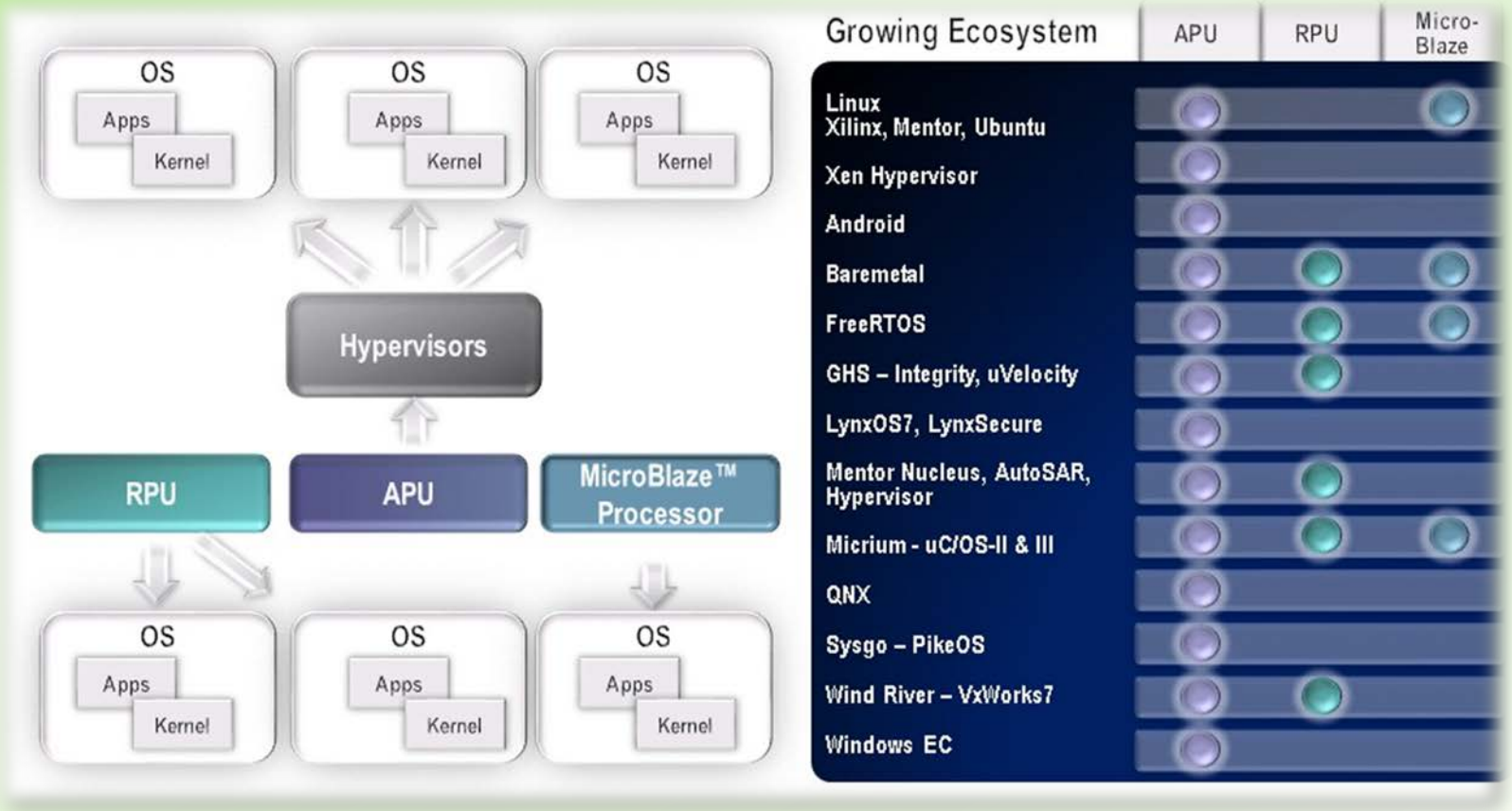
Example Configuration: APU-Hypervisor Linux / RPU

- System software
  - FSBL: First Stage Boot Loader
  - uBoot: Open source



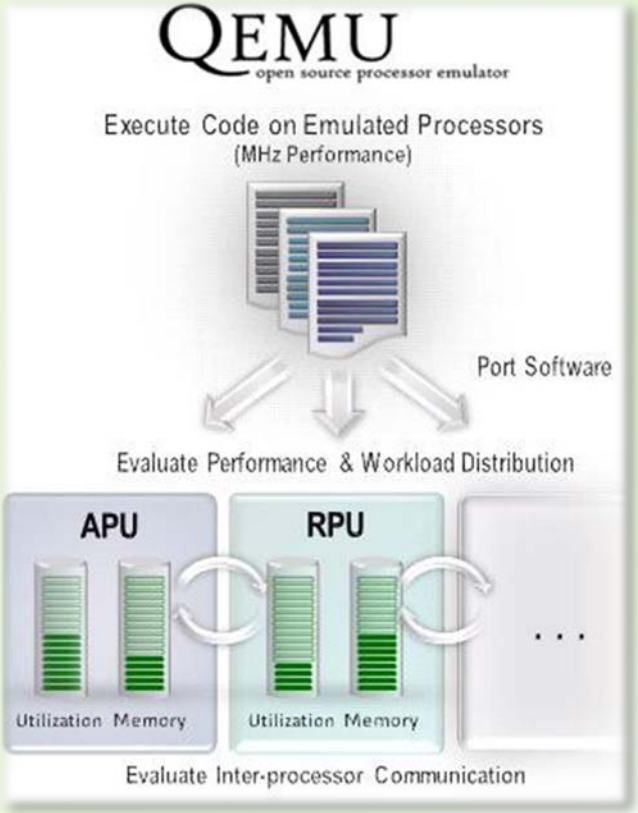
- APU: Non-secure mode
  - ARM trusted firmware/XEN hypervisor, verified on APU
  - Guest OS
  - Domain (1): Linux
  - Domain (2): Bare-metal
- RPU
  - In split mode (default)
  - R5-0: FreeRTOS
  - R5-1: Bare-metal

Run-Time Software

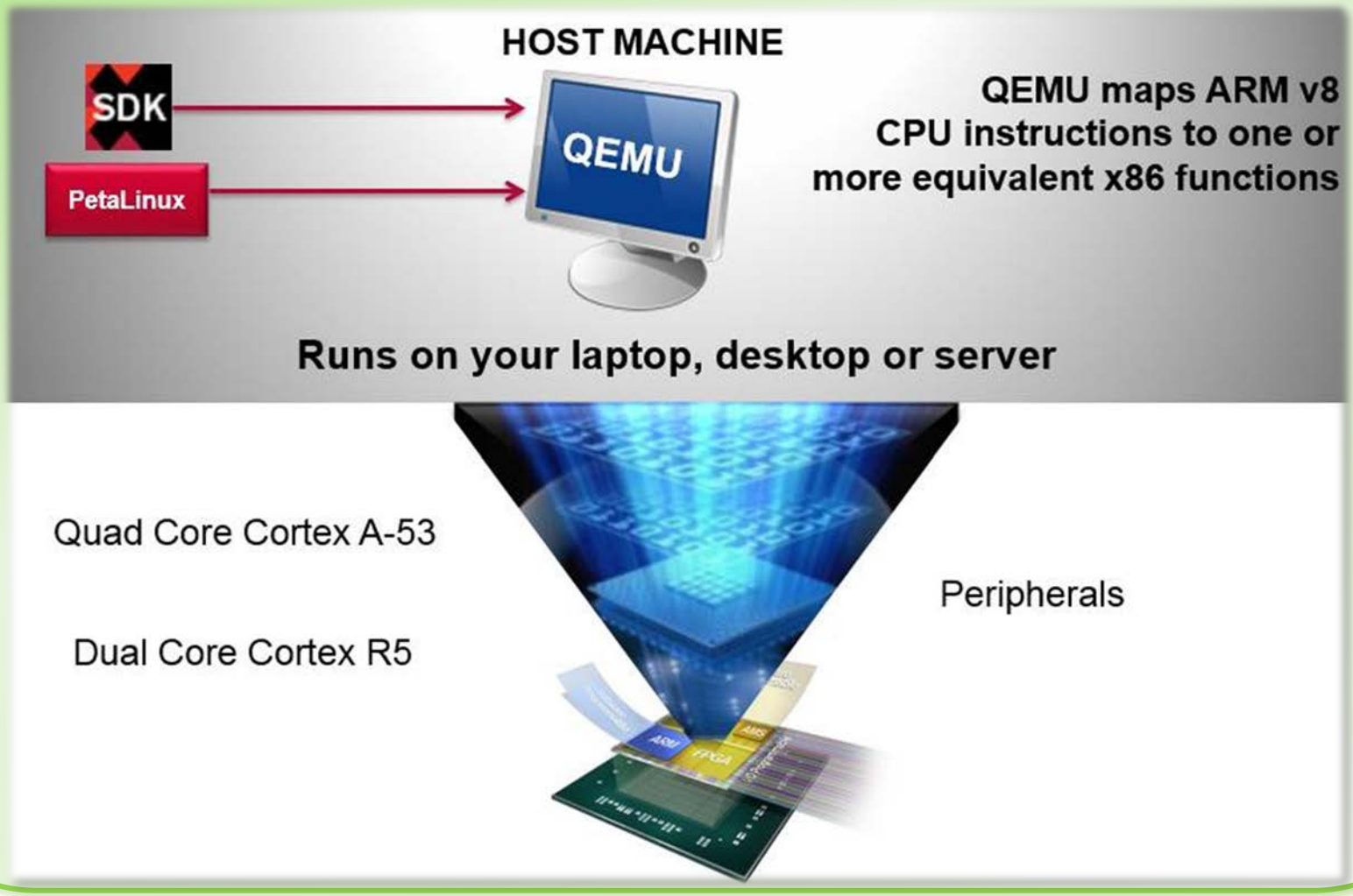


Qemu Emulation Platform

- QEMU emulation platform
  - Provides Linux hosted emulation platform
  - Accelerates and scales embedded software development
  - Enables architecture and porting of software
  - Emulates multiple blocks of the processing system
- QEMU enables you to start working on designs before hardware is available



How Qemu Works



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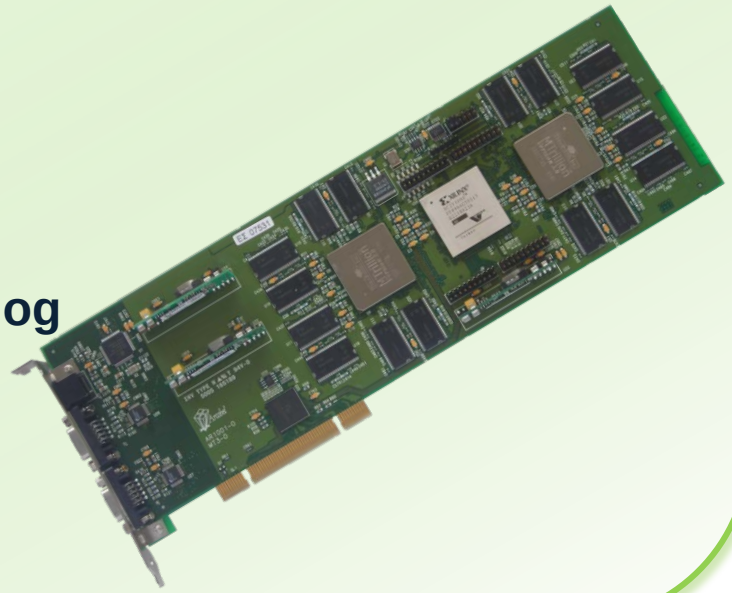
Our competences

Core|Vision has more than 125 man years of design experience in hard- and software development. Our competence areas are:

- System Design
- FPGA Design
- Consultancy / Training
- Digital Signal Processing
- Embedded Real-time Software
- App development, IOS Android
- Data Acquisition, digital and analog
- Modeling & Simulation
- PCB design & Layout
- Doulos & Xilinx Training Partner



Q&A

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Training Program

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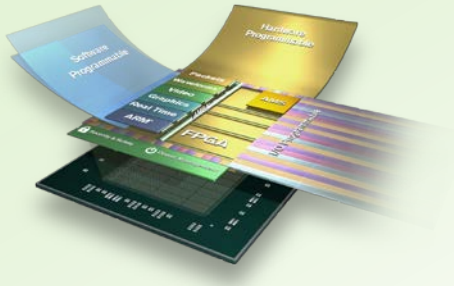
Essentials of FPGA Design	*1 day*
Designing for Performance	*2 days*
Advanced FPGA Implementation	*2 days*
Design Techniques for Lower Cost	*1 day*
Designing with Spartan-6 and Virtex-6 Family	*3 days*
Essential Design with the PlanAhead Analysis Tool	*1 day*
Advanced Design with the PlanAhead Analysis Tool	*2 days*
Xilinx Partial Reconfiguration Tools and Techniques	*2 days*
Designing with the 7 Series Families	*2 days*



Training Program

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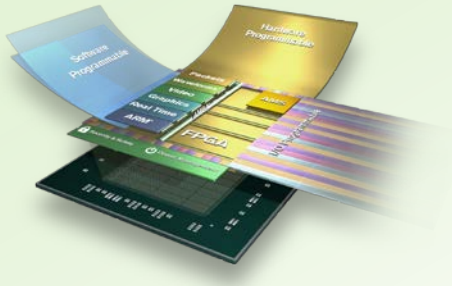
- Designing FPGAs Using the Vivado Design Suite 1 *2 days*
- Designing FPGAs Using the Vivado Design Suite 2 *2 days*
- Designing FPGAs Using the Vivado Design Suite 3 *2 days*
- Designing FPGAs Using the Vivado Design Suite 4 *2 days*
- Designing with the UltraScale and UltraScale+ Architecture *2 days*
- Vivado Design Suite for ISE Software Project Navigator User *1 day*
- Vivado Design Suite Advanced XDC and Static Timing Analysis for ISE Software User *2 days*



Training Program

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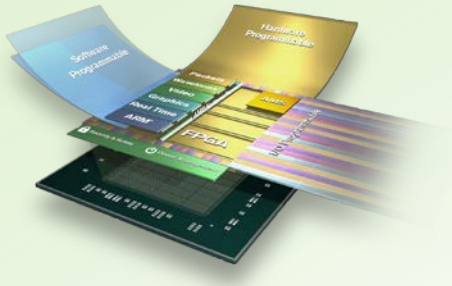
- Designing with Multi Gigabit Serial IO *3 days*
- High Level Synthesis with Vivado *2 days*
- C-Based HLS Coding for Hardware Designers *1 day*
- C-Based HLS Coding for Software Designers *1 day*
- DSP Design Using System Generator *2 days*
- Essential DSP Implementation Techniques for Xilinx FPGAs *2 days*



Training Program

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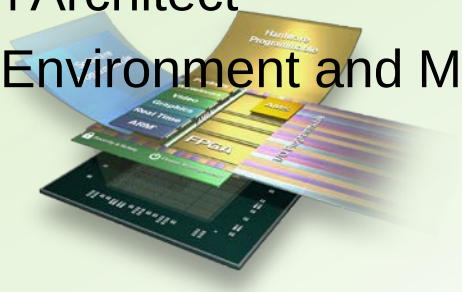
Embedded Systems Design	*2 days*
Embedded Systems Software Design	*2 days*
Advanced Features and Techniques of SDK	*2 days*
Advanced Features and Techniques of EDK	*2 days*
Zynq All Programmable SoC Systems Architecture	*2 days*
Zynq All Programmable SoC Accelerators	*1 day*
C Language Programming with SDK	*2 days*
Embedded Design with PetaLinux Tools	*2 days*
Zynq UltraScale+ MPSoC for the System Architect	*2 days*
Embedded C/C++ SDSoC Development Environment and Methodology	*1 day*



Training Program

- VHDL Design for FPGA *3 days*
- Advanced VDHL *2 days*
- Comprehensive VHDL *5 days*
- Expert VHDL Verification *3 days*
- Expert VDHL Design *2 days*
- Expert VHDL *5 days*
- Essential Digital Design Techniques *2 days*