RUTRONIK
ELECTRONICS WORLDWIDE

11 OKT BELGIË
12 OKT NEDERLAND
D&E event 2017

Secure data storage -

NAND Flash technologies and controller mechanisms

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Embedded Computing

Rutronik at a Glance

RUTRONIK ELECTRONICS WORLDWIDE

11 OKT BELGIË
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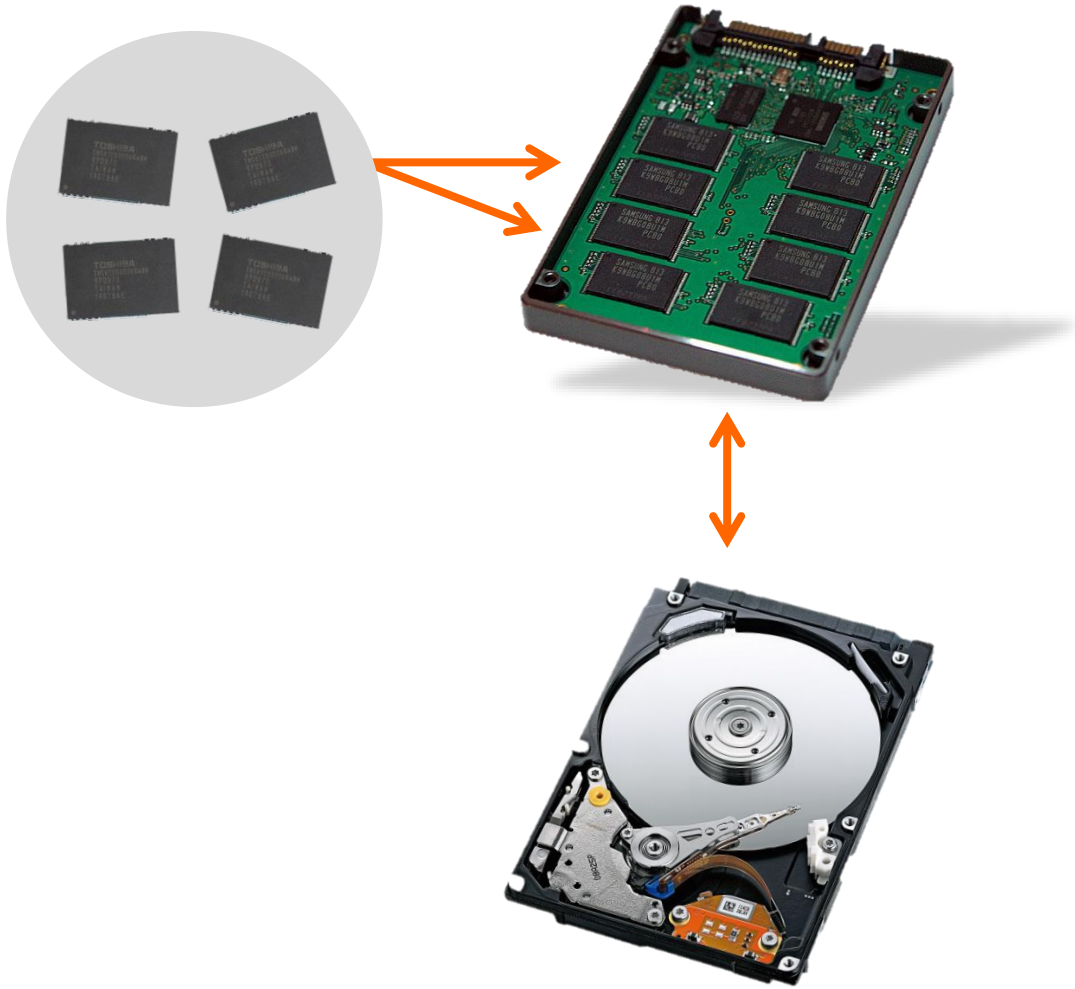
D&E event 2017

- Founded in 1973 / 2016 Revenue: 872 Mio €
- Headquartered in Ispringen/Germany / 1500 employees
- # 3 in the European distribution market (Source: Europartners)
- Global broadline distributor / Linecard with leading suppliers
  - Semiconductors
  - Passive components
  - Electromechanical components
  - Embedded & wireless
- Expertise in several markets
  - Digital Signage
  - Medical
  - Transportation
  - Industrial Automation

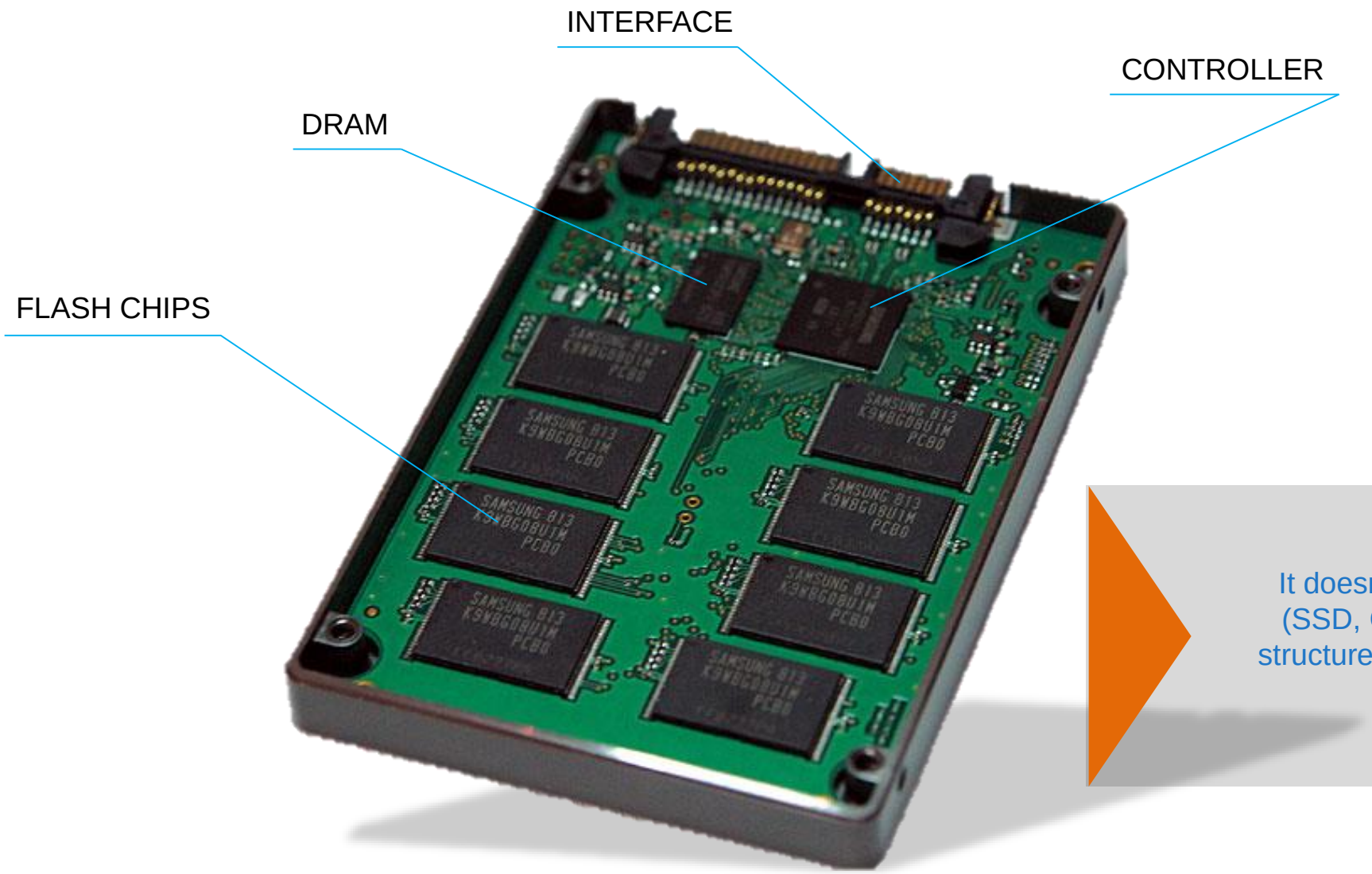
NAND flash memory

What is it?

- Electronical non volatile storage technology
- Non-rotating parts
- Noiseless operation
- Shock and vibration robust
- High and low temperature resistant
- Fast access times
- Smaller dimensions possible

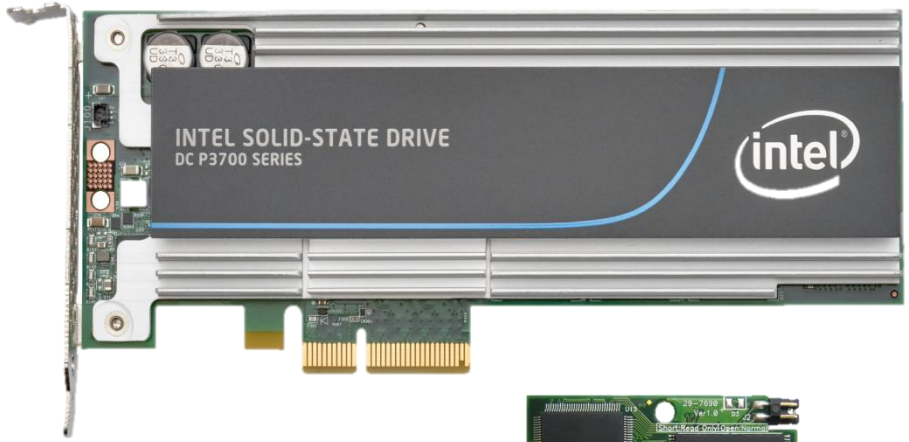


Construction of a Flash module



It doesn´t matters which „formfactor“ (SSD, CFast, SD, MicroSD etc.) the structure and the mode of operation will allways be the same

Common Formfactors



Add-in-Card

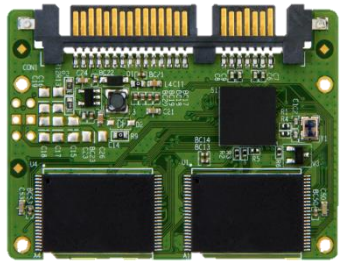
2,5“ SSD

USB-Stick

microSD

SD-Card

Flash Disc Module



Half-slim SSD

CFast

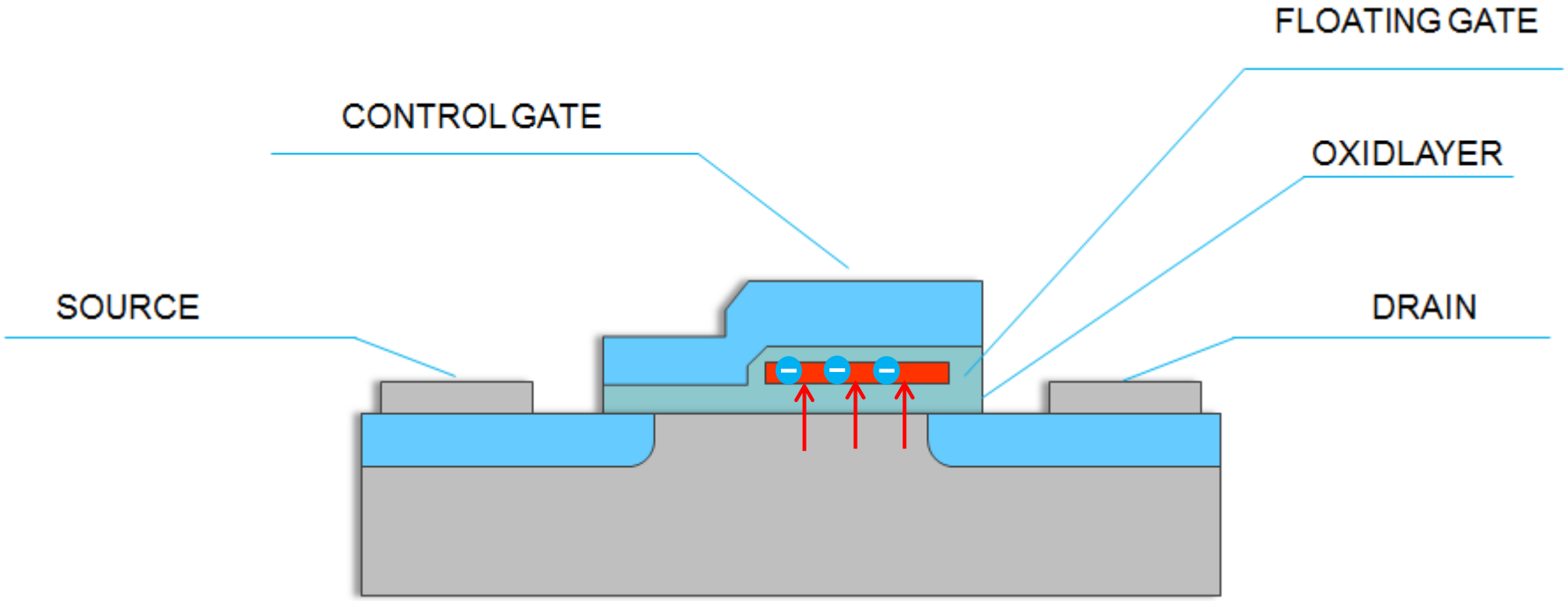
CF Cards

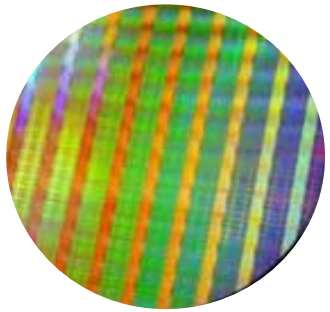
M.2 SSD

mSATA mini

mSATA

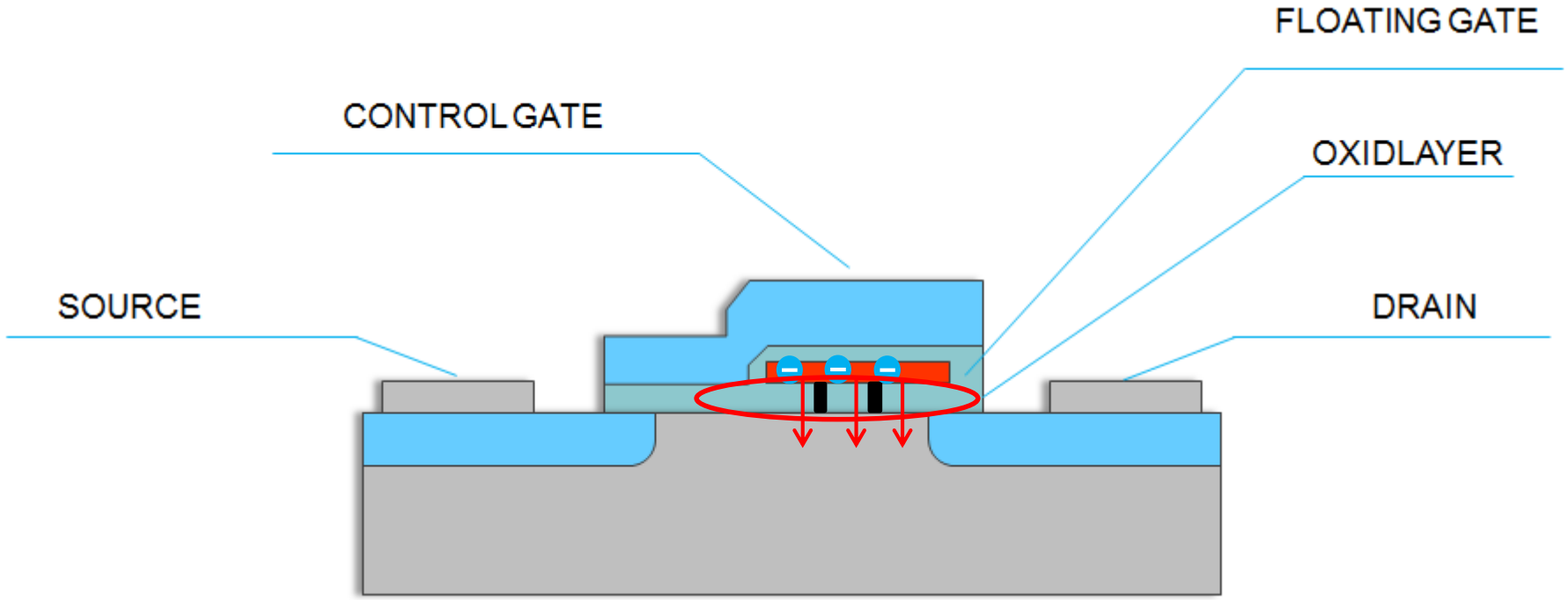
Construction of a Flash cell

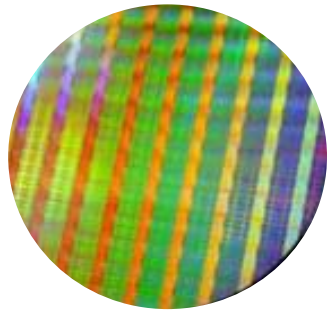




- **Programming in pulses pushing electrons through membrane**
- **Membrane wears out (programming becomes faster, retention decreases)**
- **Temperature has an impact on electrons' "excitement"**

Construction of a Flash cell





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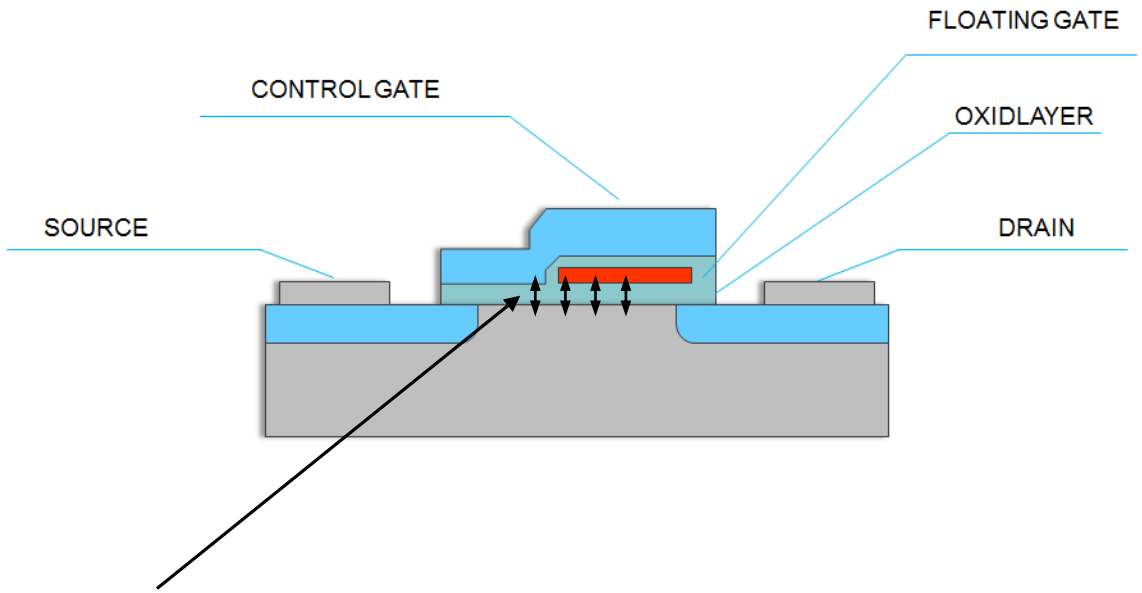
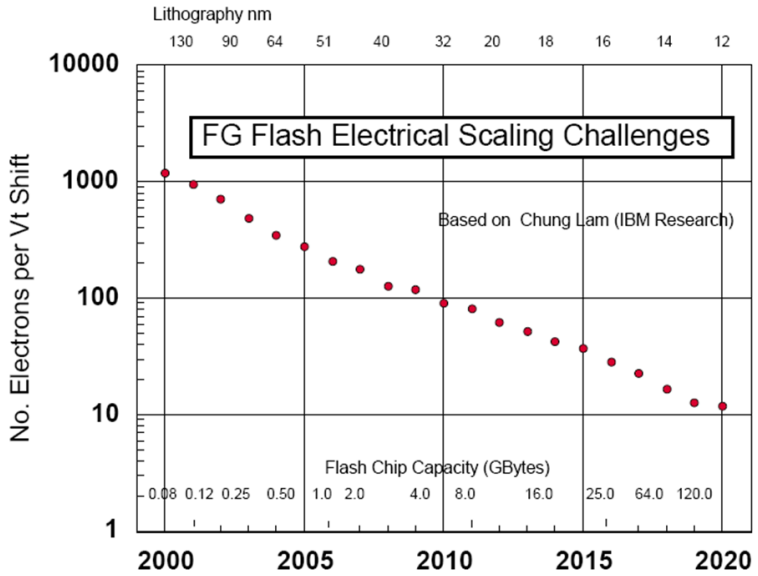
Effects of die shrinking



1. Oxid layer is getting thinner

Flash Cell Scaling Down

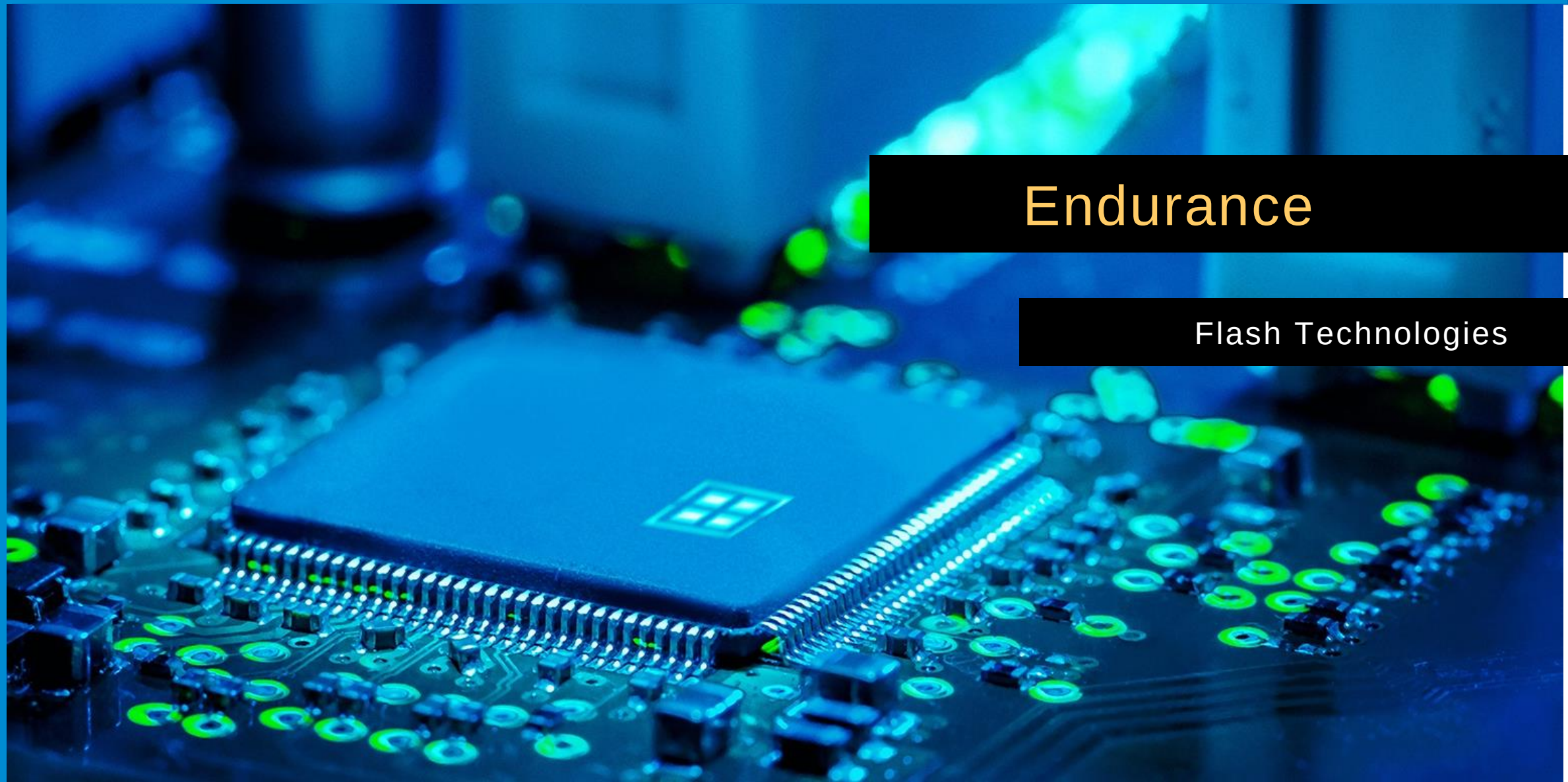
Number of electrons in a 20nm SLC is less than 100...



2. Number of electrons are decreasing

Main concerns

Concerns	Impacts	Mechanism
Endurance	P/E cycles Flash Technology Bit failures	Chosing right physics Wear Leveling Read Disturb Management
Data Retention	P/E cycles, High read only count Temperature	Chosing right physics Auto Refresh
Power Loss	Unstable power suply Volatile buffer	Capacitor PL protection Firmware PL recovery



Endurance

Flash Technologies

Endurance

Why is there an Endurance factor?

- Due to wearing out the oxidlayer, there are limited P/E cycles
- The more wear outs, the higher the probability of bit failures

Main issues due to wrong use case:

Shorter lifetime than expected

Uncorrectable errors in the field

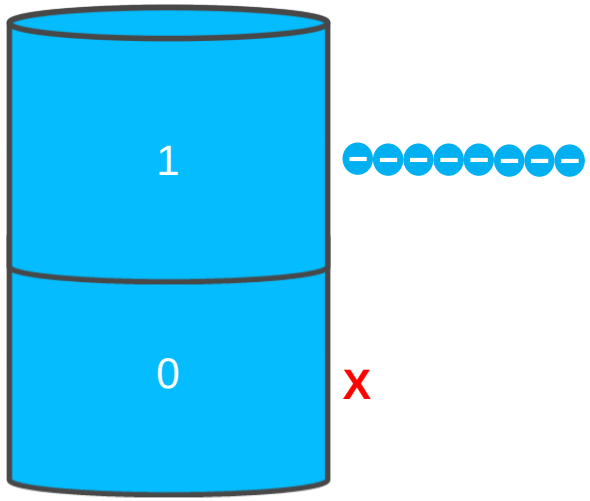
Physical Technology

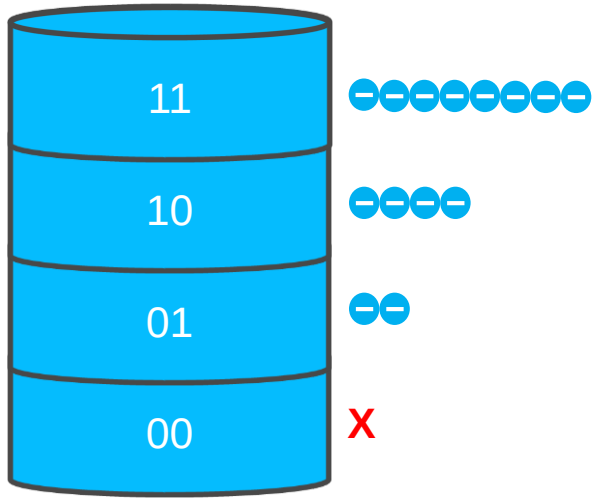
Controller
Wear Lveling, Read Disturb Management, Overprovioning

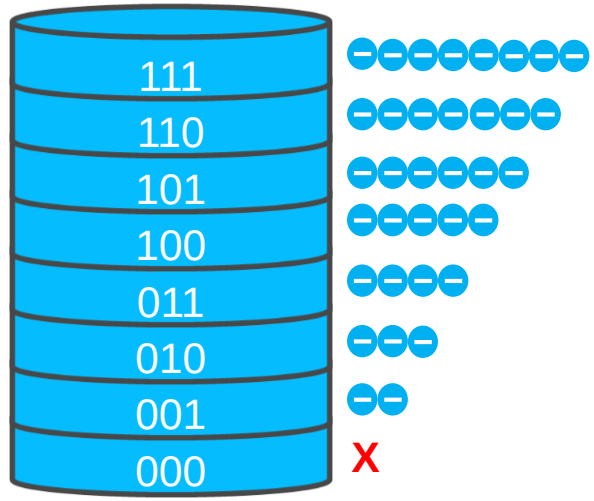
Flash technology comparison

	SLC	Pseudo-SLC	EM-MLC	MLC	TLC
Performance	very fast	fast	average	average	very low
Price per GB	$$$$	$$$	$$$	$$	$
Reliability & Data retention	+++	++	++	+	-
Flash Endurance (PE Cycles)	Up to 100k	Up to 30k	Up to 30k	Up to 3k	Up to 1k
Bits per cell	1	1	2	2	3
Power Consumption	low	low	average	average	Average
Lifecycle	Ca. 3-5 years	ca. 1-2 years	ca. 1-2 years	ca. 1-2 years	ca. ½ - 1 year

Bit Failures/Flips



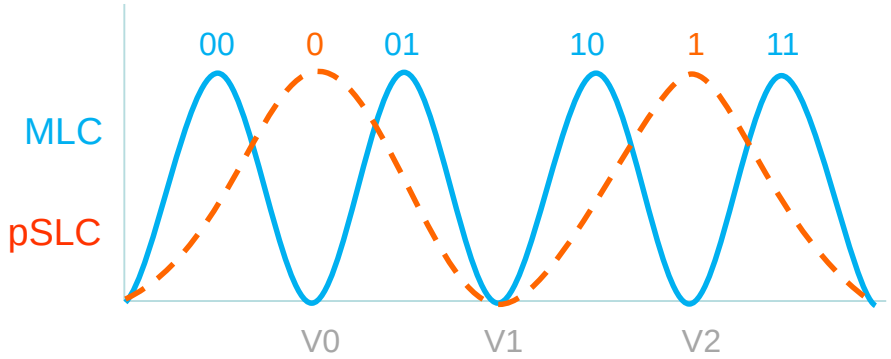




- SLC memory elements can represent one of two charge states, MLCs four states and TLCs eight.

- The applied voltage is fixed, which means that voltage must be applied to MLC cells up to four times during a write operation to achieve the maximum charge state. Therefore, MLCs and TLCs tolerate fewer write operations.

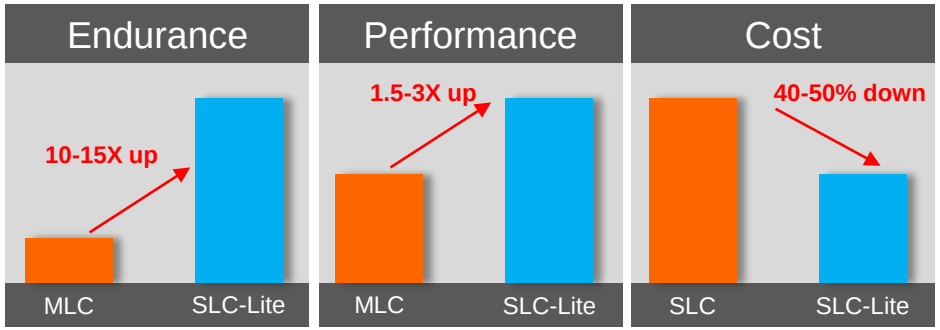
Pseudo SLC vs EM-MLC

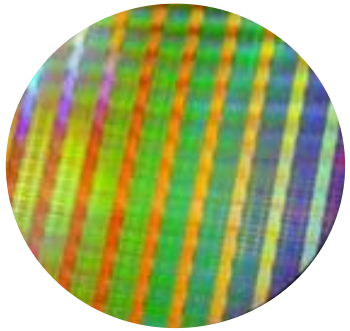


SLC-Lite products are based on MLC architecture, but their performance & reliability are improved by customized firmware

Benefits: Cost is 40-50% cheaper compared to SLC! Endurance will be increased at least 10 times compared to MLC! Improved performance especially sequential write!

Threats: Endurance will be specified by module supplier



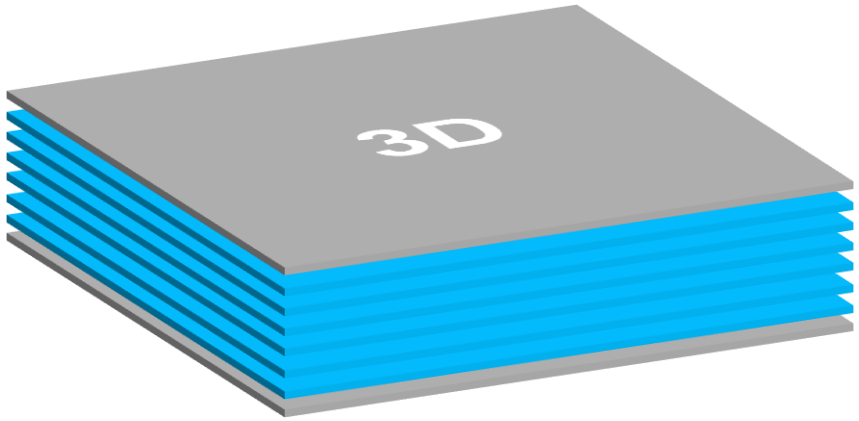


EM-MLC chips are based on screened MLC architecture. Quality of flash dies differ. The dies with better physical features will be specified as EM-MLC.

Benefits: Cost is 40%-50% cheaper compared to SLC! Endurance will be increased at least 10 times compared to MLC! Endurance guaranteed by flash vendor!

Threats: Performance a bit lower than SLC Lite

3D NAND Technology



- Cells will be sorted in vertical position
- Dies will be stacked in layers (48 - 64 layers)
- Only MLC and TLC technology
- Geometries are bigger again
- Density increases
- Costs decrease

Data Retention

Flash Technology Specs

Temperature impact

Data Retention

What is data retention?

- Electrons are leaking due to worn out isolation layer
- Temperature has a bad effect on data retention!
- The more wear outs, the faster electrons are fleeting

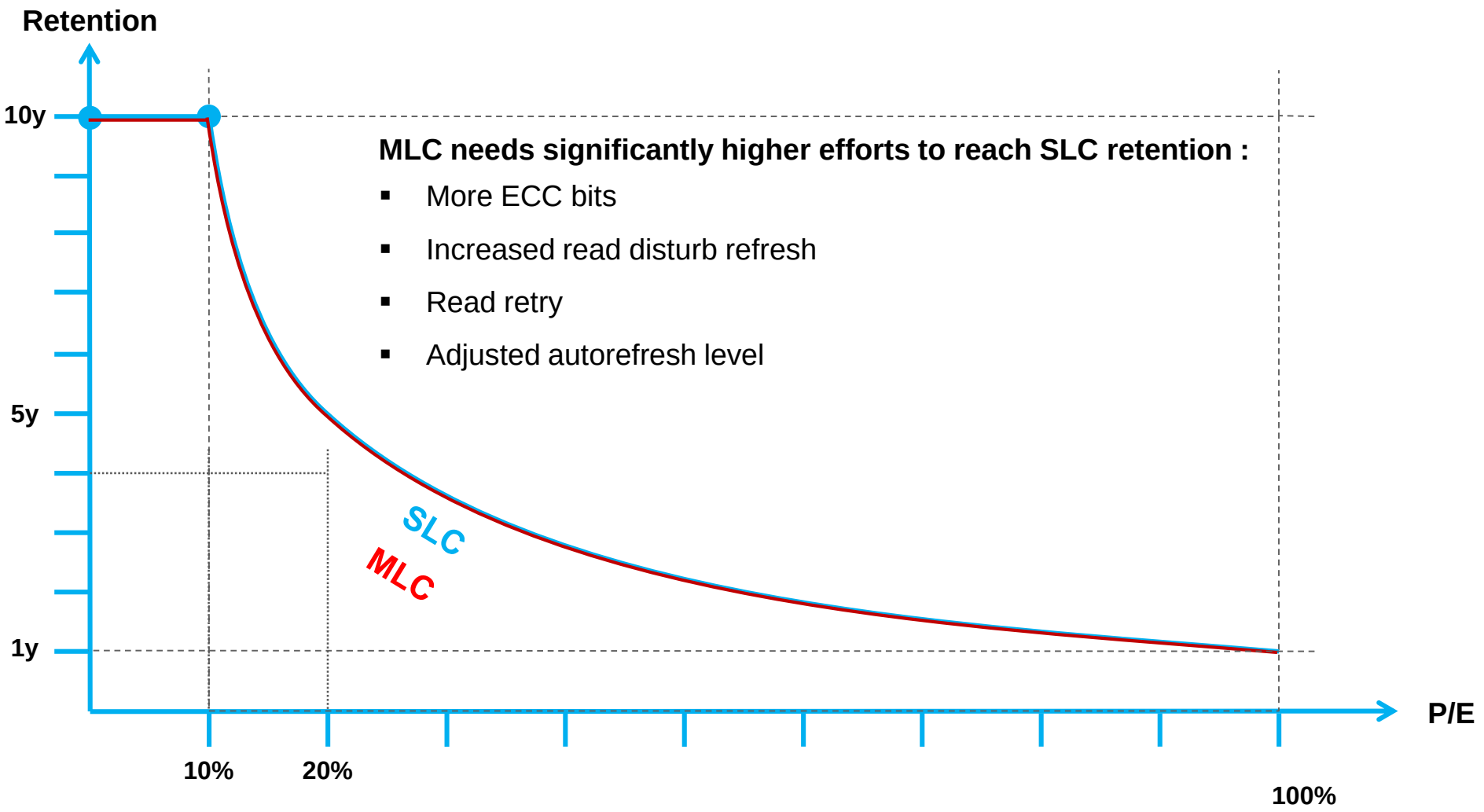
Main issues due to data retention:

Static or unused data can be lost

Physical Technology

Auto Refresh

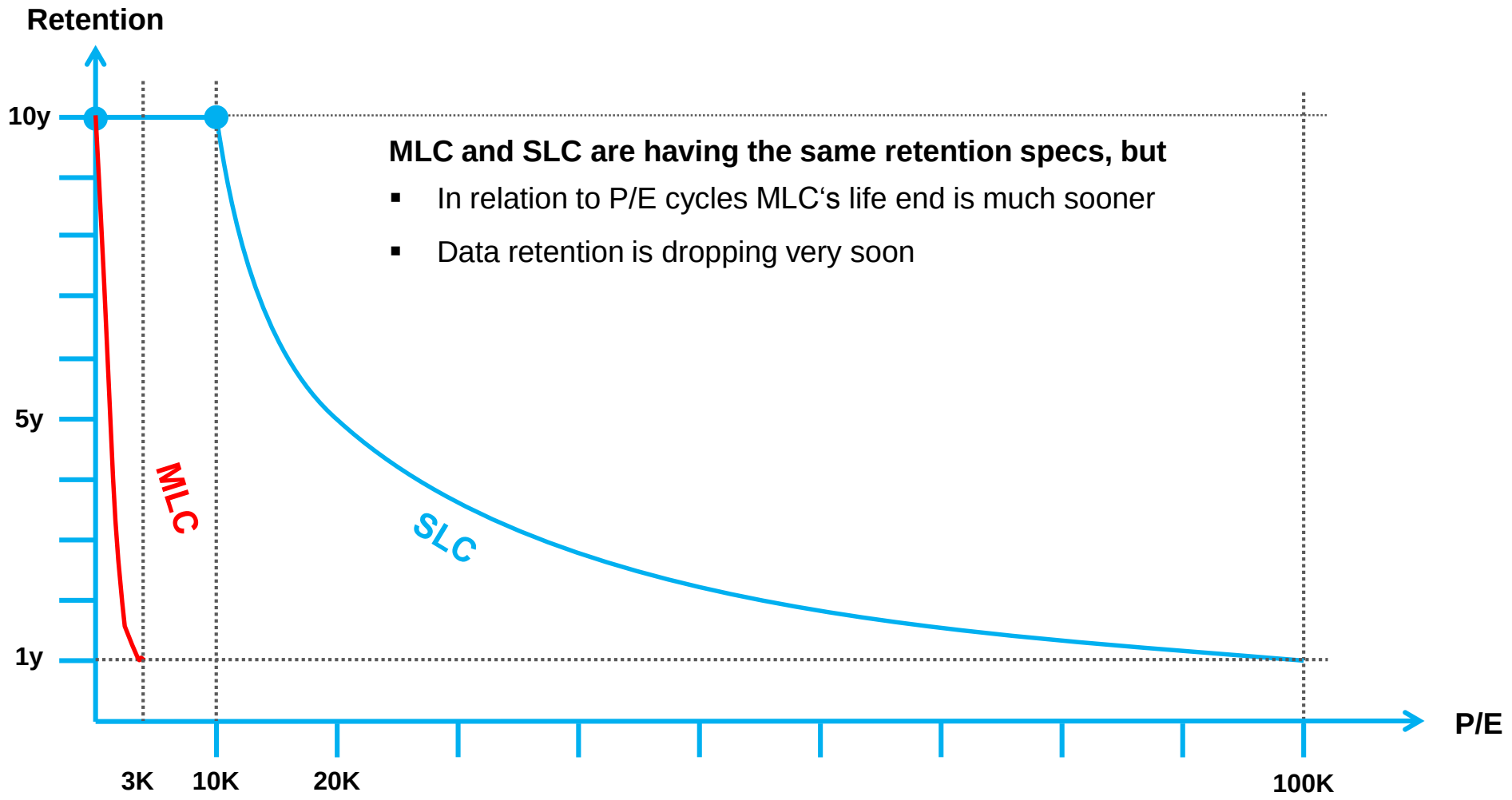
Retention Spec.



MLC needs significantly higher efforts to reach SLC retention :

- More ECC bits
- Increased read disturb refresh
- Read retry
- Adjusted autorefresh level

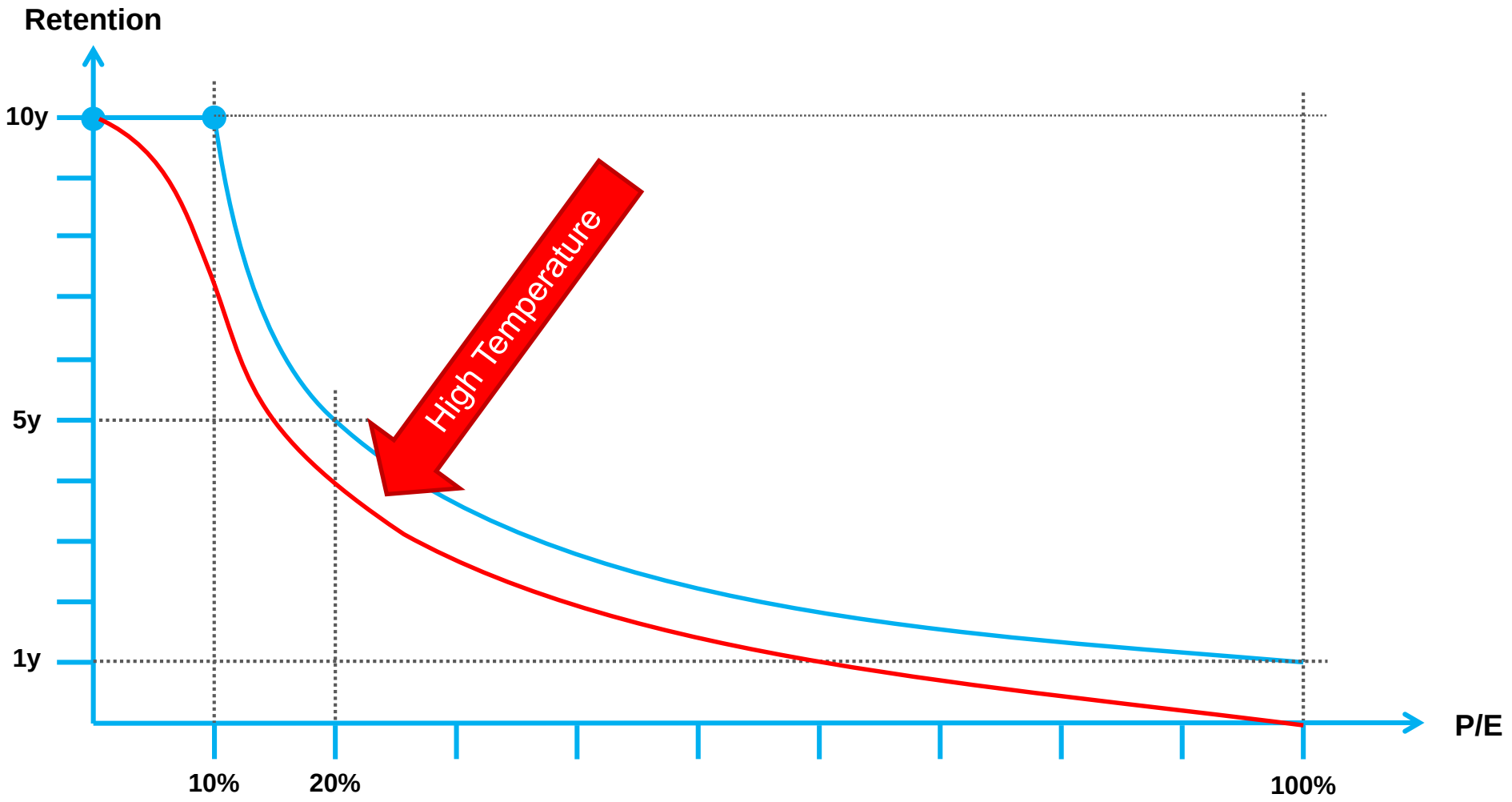
Retention vs. Endurance

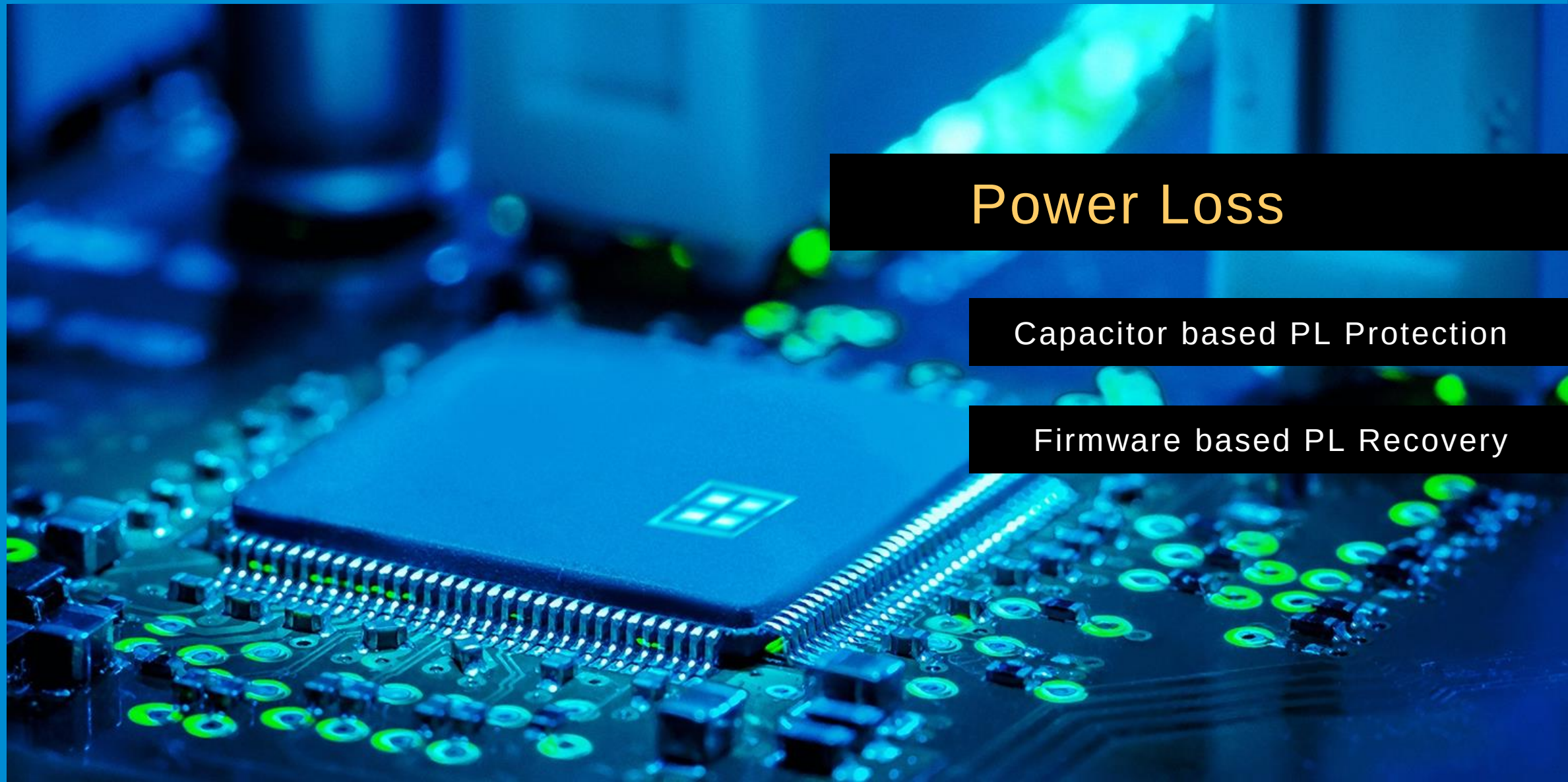


MLC and SLC are having the same retention specs, but

- In relation to P/E cycles MLC‘s life end is much sooner
- Data retention is dropping very soon

Temperature influence



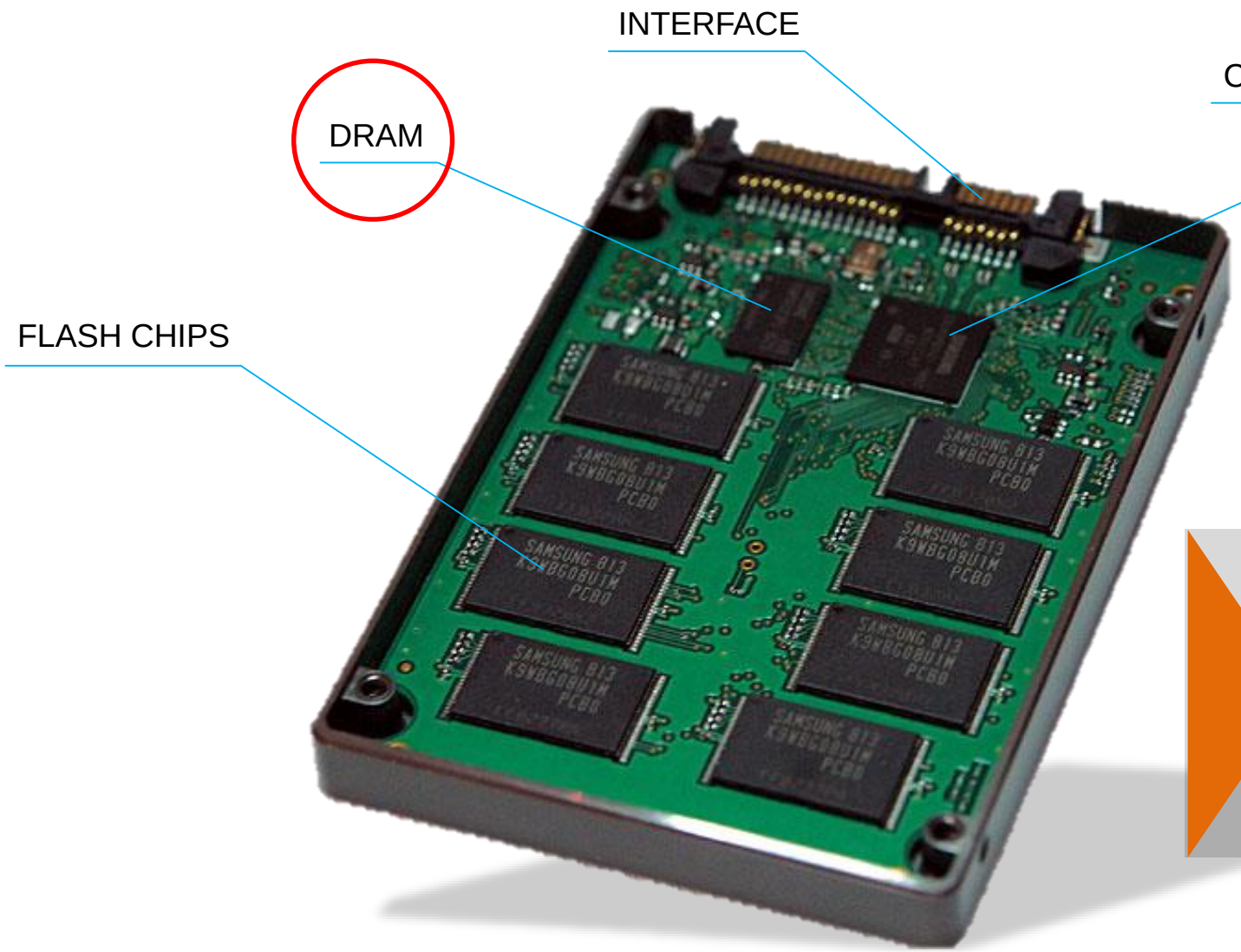


Power Loss

Capacitor based PL Protection

Firmware based PL Recovery

Weak point at construction



With performance needs, system integrity gets harder to achieve

Power Fail

What is a power fail?

- Sudden power loss due to switching off the power cord or a blackdown
- Power glitches due to unstable power supply

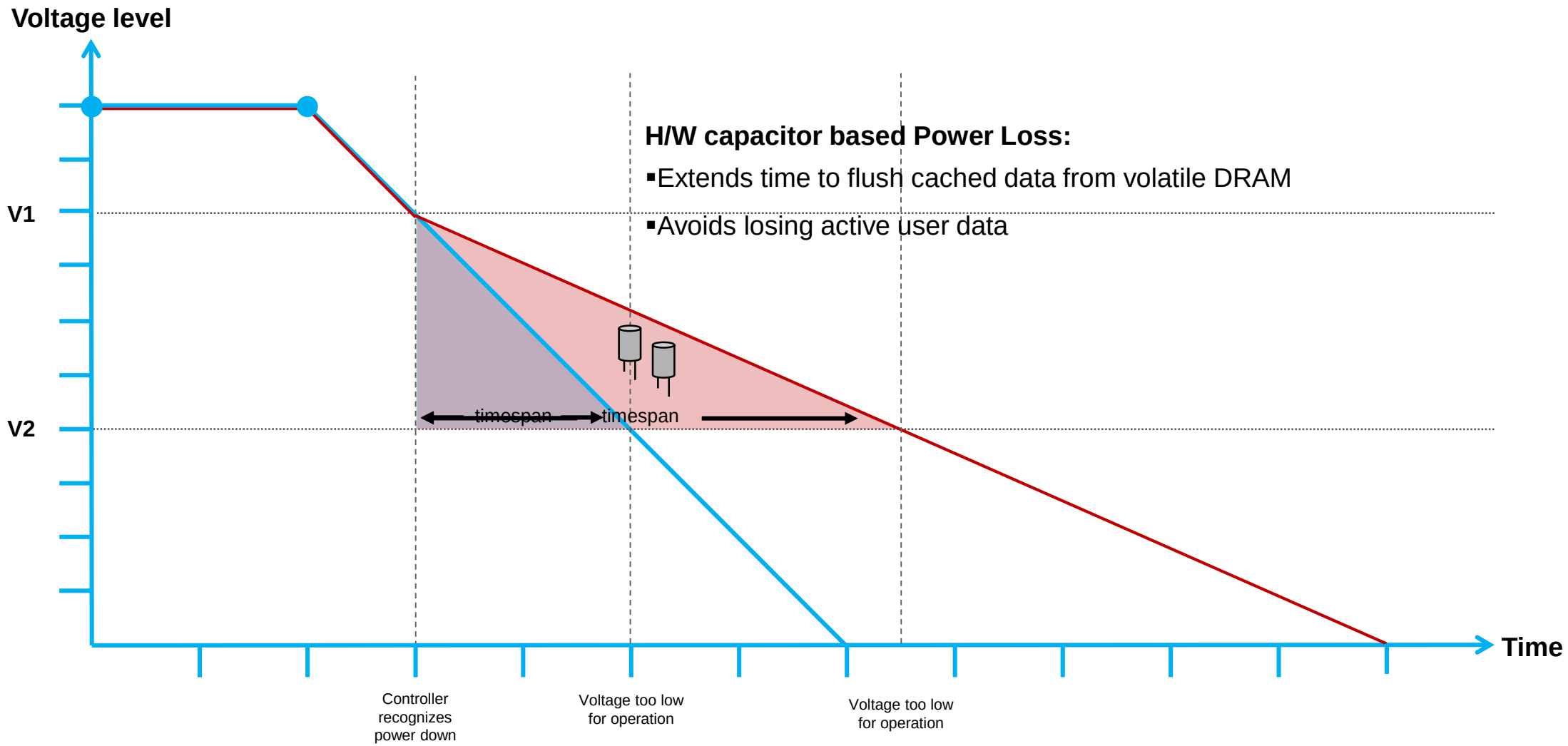
Main issues due to Power Loss:

User data can be lost when using DRAM cache — Capacitors

Uncompleted write processes create corrupt files — Firmware

Management data can be corrupted.
System fails!

Capacitor based PL Recovery



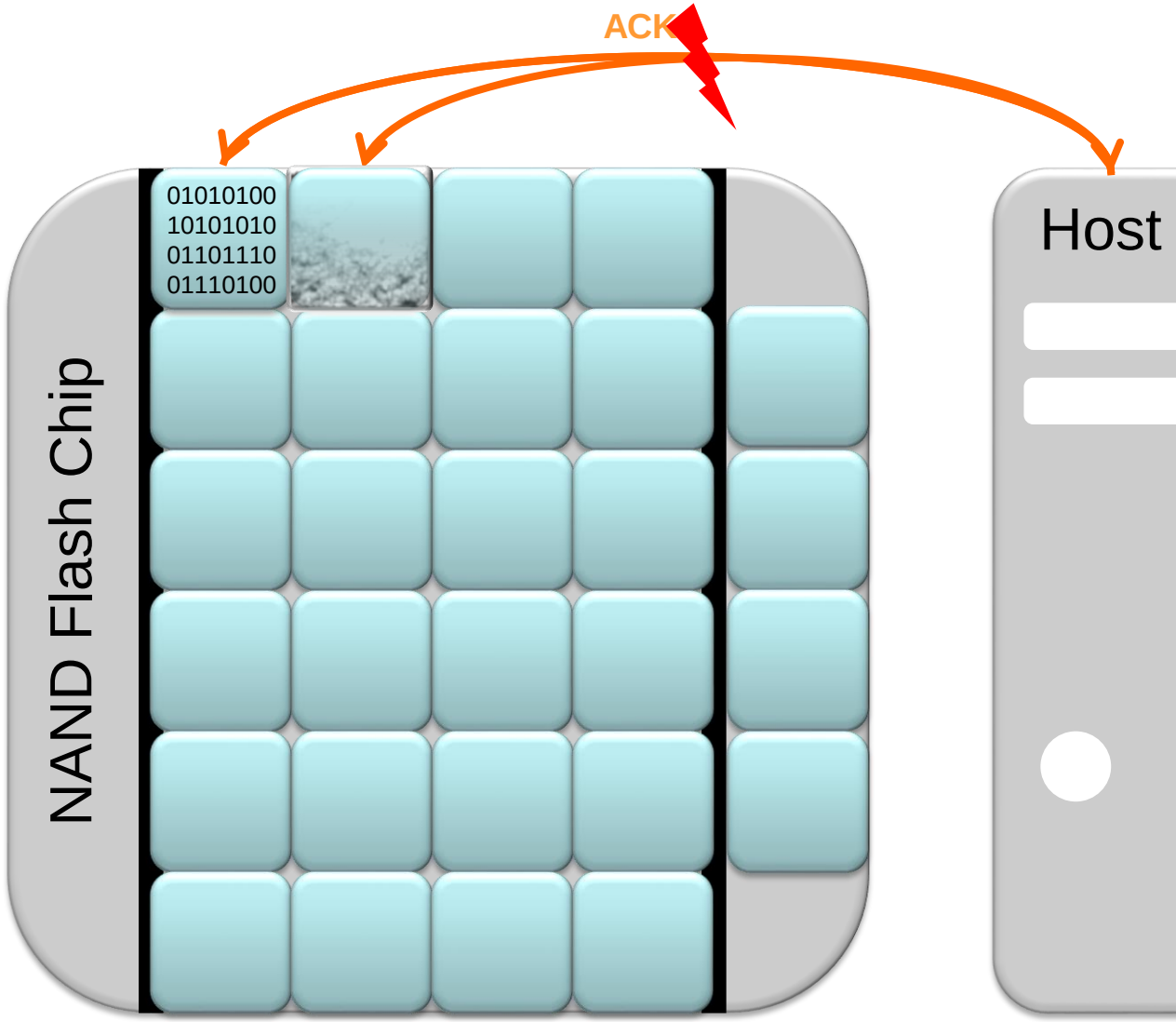
H/W capacitor based Power Loss:

- Extends time to flush cached data from volatile DRAM
- Avoids losing active user data

No firmware based PL Recovery

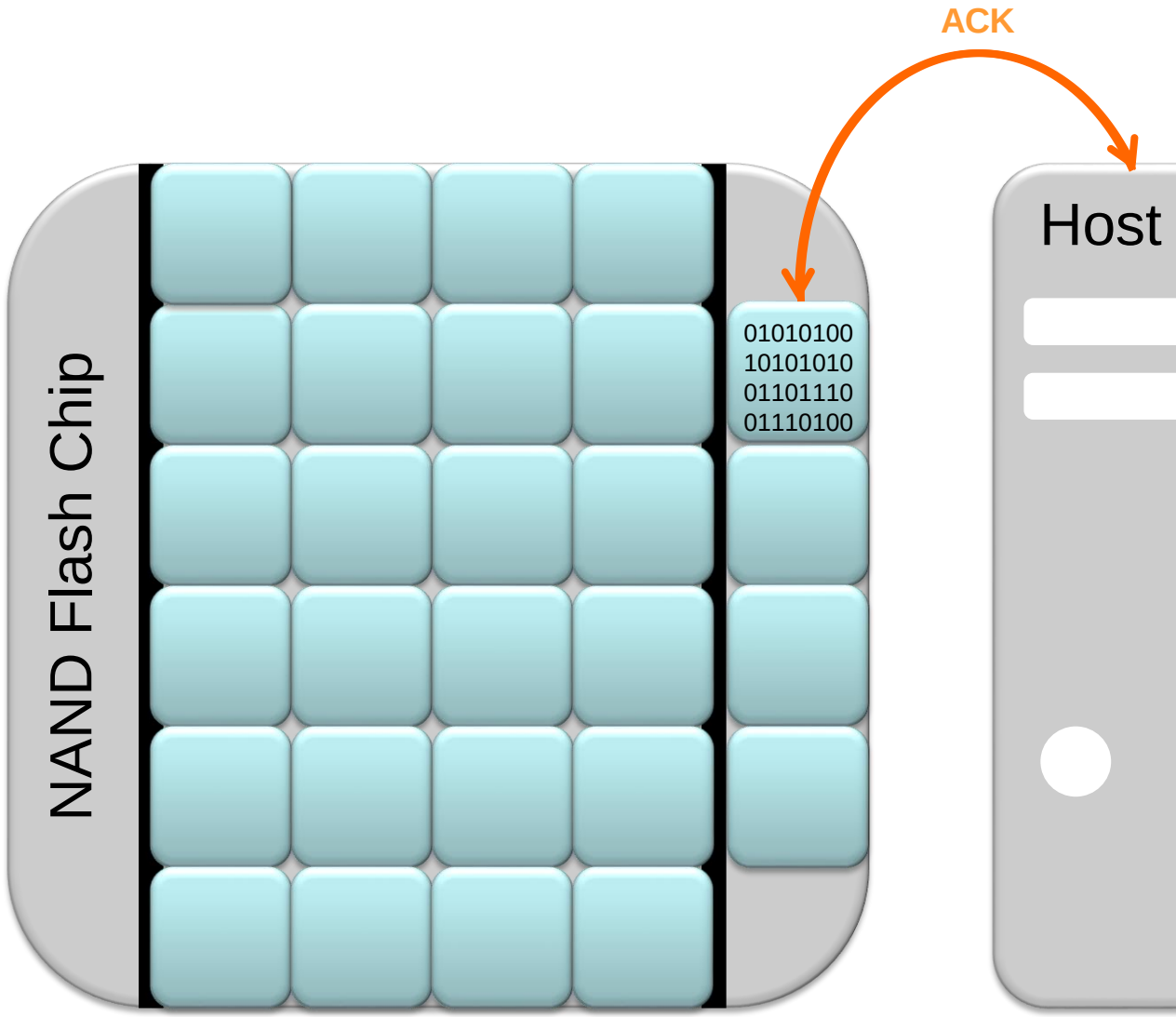
1. Write command from Host
2. Block acknowledges after succesful write
3. New write command from Host
4. Power down – data not written completely
5. Corrupted data!

Files are unvalid. System could be damaged.



Firmware based PL Recovery

1. Write command from Host into inactive area
2. Block acknowledges after succesful write

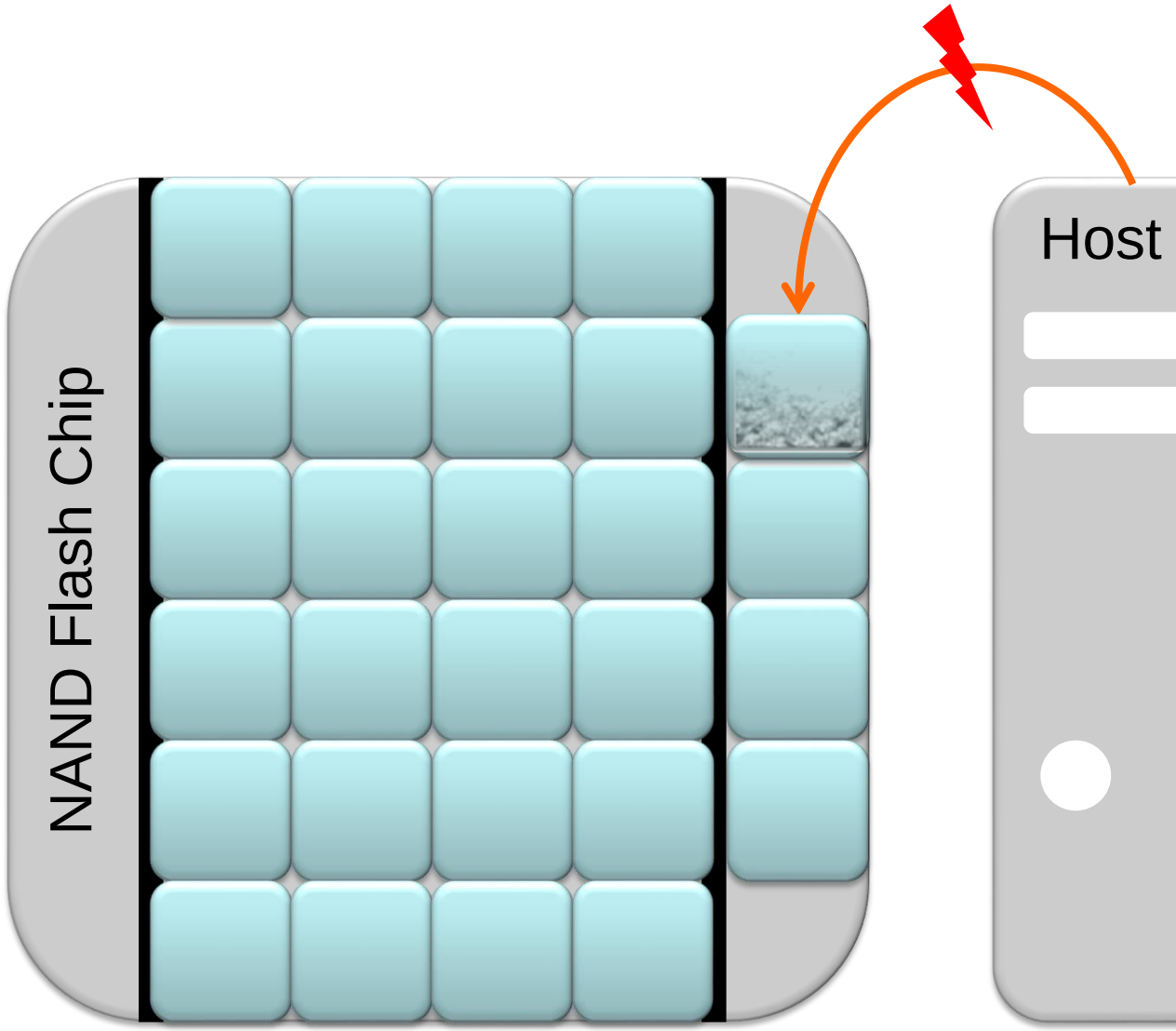


Firmware based PL Recovery

1. Write command from Host into inactive area
2. Block acknowledges after succesful write
3. Block will be activated

4. New write command in process
5. Power Down occurs
6. Corrupted data stays inactive!
7. Boot up with last correct data set

Redundand system. No system crash.
Always boot up with correct data.



Performance vs. Security

Performance

Security

	Secured User data	Secured Boot up
•DRAM cache w/o FW and cap. PL Recovery	NO	NO
•DRAM cache with capacitor PL Recovery	YES	NO
•DRAM cache with FW based PL Recovery	NO	YES
•DRAM cache with capacitor and FW based PL Recovery	YES	YES
•Avoiding DRAM cache + FW based Power Loss Recovery	YES	YES

Thank you

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