

Renesas Synergy Concept

Much more than a microcontroller family

AVNET[™] SILICA



Renesas Synergy Concept

Much more than a microcontroller family



AVNET[®] SILICA

Developers know that time to market is a huge factor in a company's success. Missed deadlines mean lost opportunities that can often never be replaced. The Renesas Synergy Platform allows developers to save precious design time and get their products to market faster. This session will give you a brief overview of this innovative concept; a game changer in embedded development of both software and hardware.

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Avnet Silica

Avnet Silica is the European semiconductor specialist division of Avnet, one of the leading global technology distributors, and acts as the smart connection between customers and suppliers. The distributor simplifies complexity by providing creative solutions, technology and logistics support. Avnet Silica is a partner of leading semiconductor manufacturers and innovative solution providers over many years. With a team of more than 200 application engineers and technical specialists, Avnet Silica supports projects all the way from the idea to the concept to production.

QUICK FACTS

- Focus on semiconductor market
- 940+ employees across Europe
- 46 offices in 22 countries across EMEA
- 70 selected franchises on highly specialised linecard
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Avnet Silica is the smart connection between our Customers and our Suppliers. We simplify complexity by providing creative solutions, technologies and logistics via our passionate, energized and empowered team.

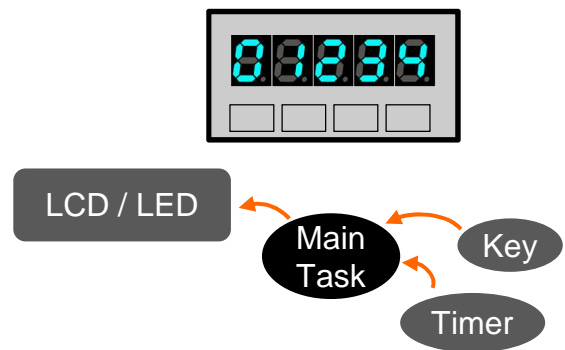
Avnet Silica provides the best technologies, services and ideas to high-tech companies across Europe. We listen to our customers' challenges and turn them into competitive opportunities. Our people are engaged customer advocates. They act fast and ensure a seamless execution.

OUR SUPPORT STRUCTURE



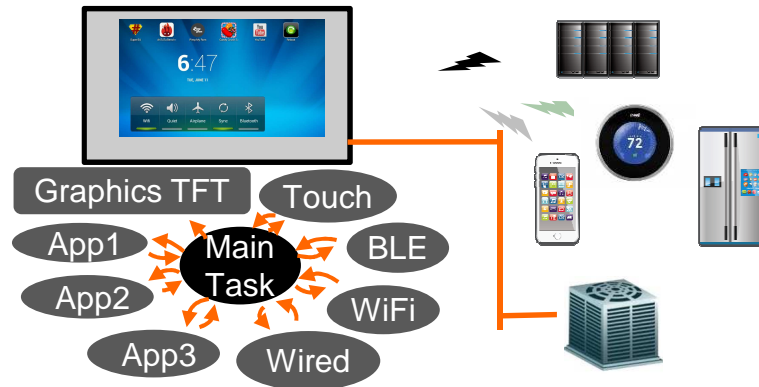
Embedded Systems Have Changed

Legacy Embedded System



- Single function
- Closed within the device
- A few interrupt sources

Connected Embedded System



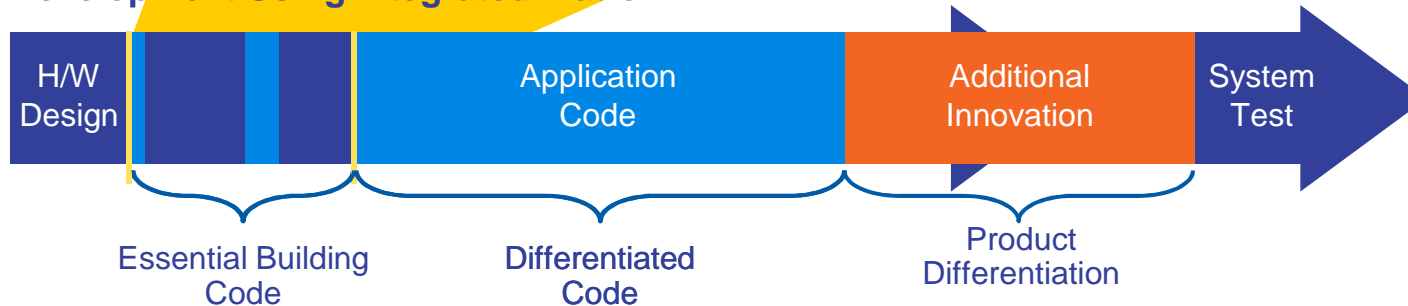
- Multi-function
- Connected with devices via network
- Many interrupt sources

Developers Want to Reduce Development Time

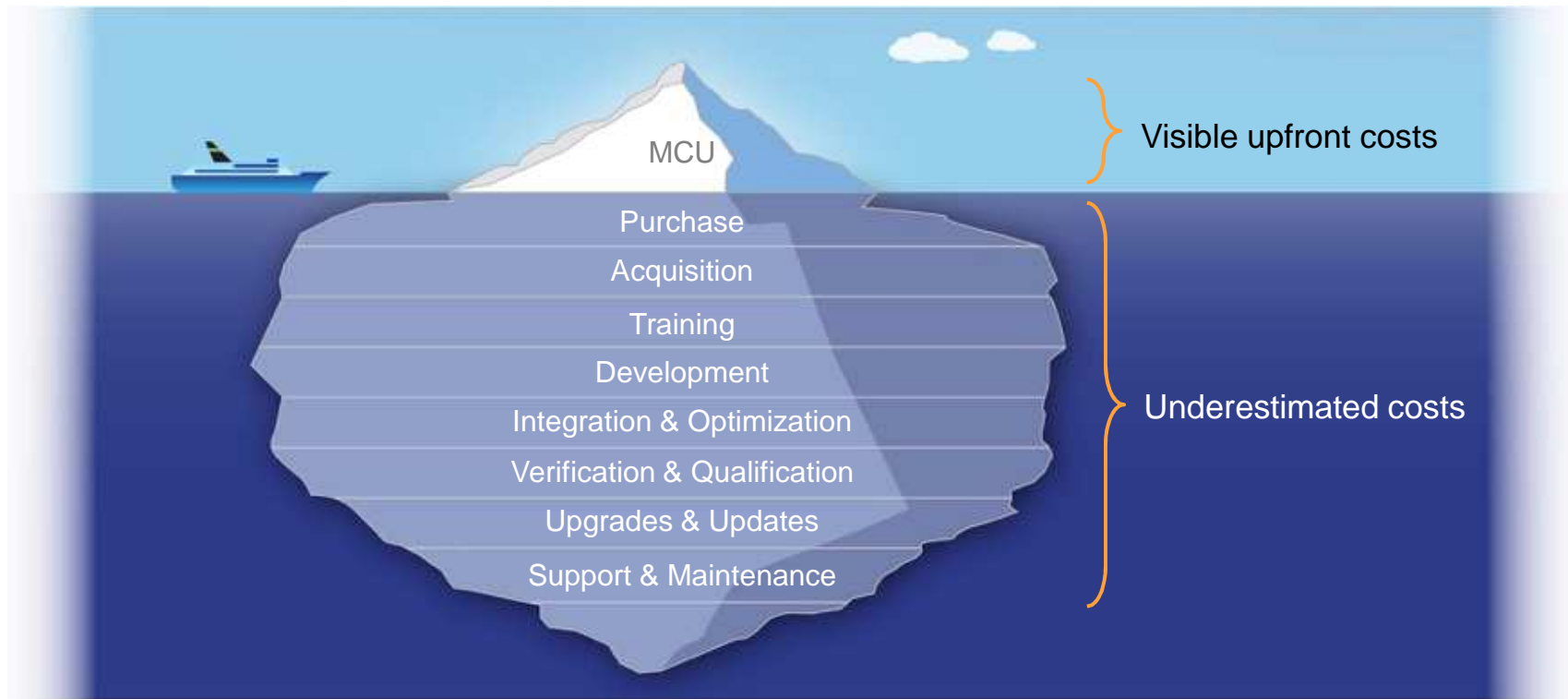
Traditional Development



Development Using Integrated Platform



Developers Want to Minimize Total Costs



How Does Synergy Platform Address These Needs?



An Ideal Platform for Embedded Developers



A complete and qualified platform that **accelerates** embedded development, inspiring **innovation** and enabling **differentiation**.

Our Three Values



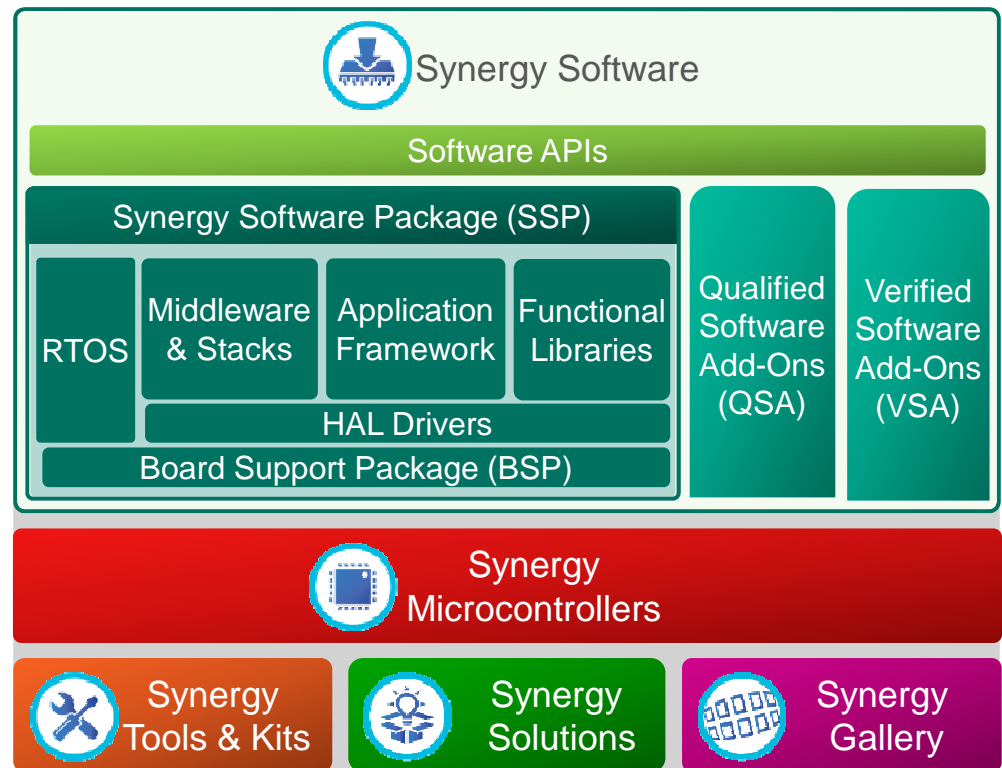
Faster
Time to
Market








Reduce
Total Cost
of Ownership



Lower
Barriers
to Entry

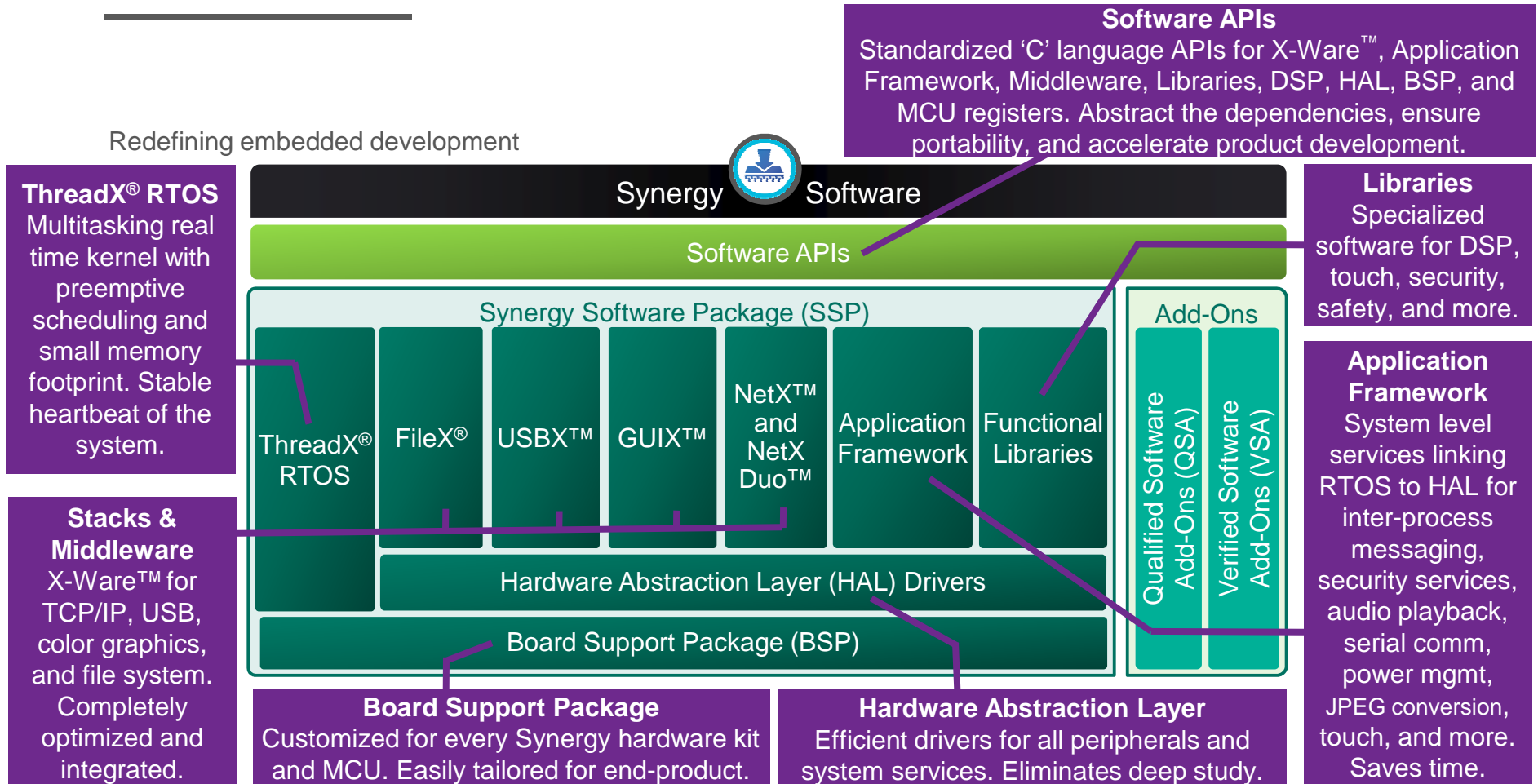


What it is: Synergy Platform Elements

Software	Microcontrollers	Tools & Kits	Solutions	Gallery
<ul style="list-style-type: none">• Qualified Synergy Software Package (SSP) for guaranteed operation• Complete package fully integrated and maintained• Applications can be written at the Software API level 	<ul style="list-style-type: none">• Wide MCU spectrum based on 32bit ARM® Cortex®-M CPU cores• Completely scalable and pin compatible• On-chip Flash memory up to 4 MB• Security & encryption acceleration• Ultra low power 	<ul style="list-style-type: none">• Integrated Solution Development Environment (ISDE) with context-aware documentation• Starter Kits (SK) and Development Kits (DK) for immediate access to entire software package 	<ul style="list-style-type: none">• Product Example (PE) kits: Complete design journeys representative of end-product designs• Application Example (AE) kits: Technology building-block examples to build upon 	<ul style="list-style-type: none">• Web access to Synergy specific software, tools, licensing plus 3rd party software & services• Future growth to complete secure cloud access infrastructure for end-products to use 

Renesas Synergy™ Software

Redefining embedded development



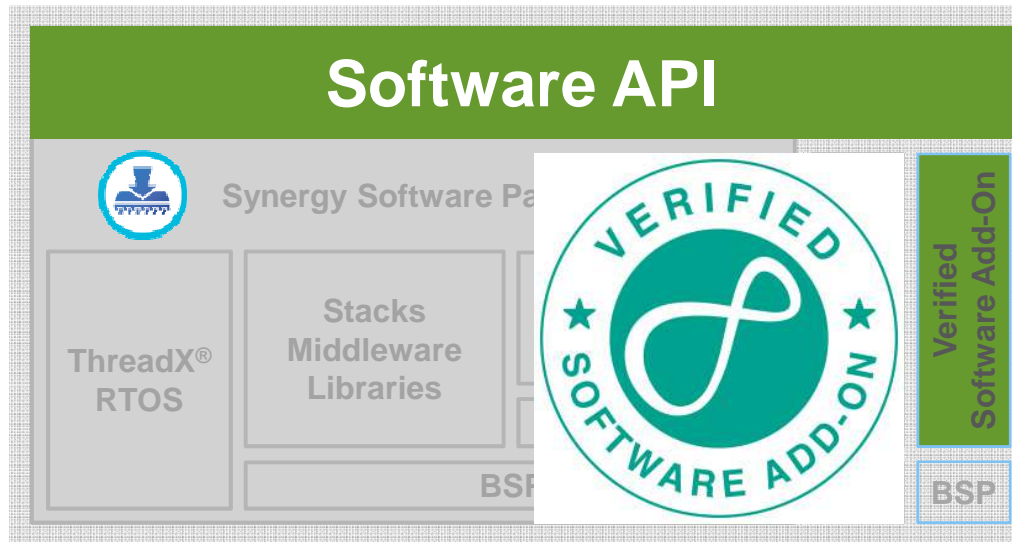


Verified Software Add-ons

How to access VSA's?

VSA evaluation software is downloaded from the Renesas Synergy™ Gallery.

VSA production software is licensed from the 3rd party software vendors.



VSA Compliance

Proven compatibility with Synergy platform per Renesas specifications.

Tested on Renesas hardware.

Documented Functionality: Test procedures and results provided.

Are VSA's chargeable?

Case by case.

VSA's can be free-of-charge or chargeable. Depends on common software market pricing.

How are VSA's supported?

Synergy is supported by Renesas.

For VSA's, Renesas will support initial assessment and ensure the best possible source of support takes over.

Quality: How Renesas defines software as a product

Best Practices

Software Development Life Cycle (SDLC):

- Traceability.
- Coding standards.
- Code reviews.
- Continuous integration.
- Professional release process.

Industry Standards

Well-respected standards for software development:

- MISRA C:2012 compliant.
- ISO/IEC/IEEE 12207 – Software life cycle processes.
- CERT 2nd Edition – C Programming Language Secure Coding Standard.

Software Quality Assurance (SQA)

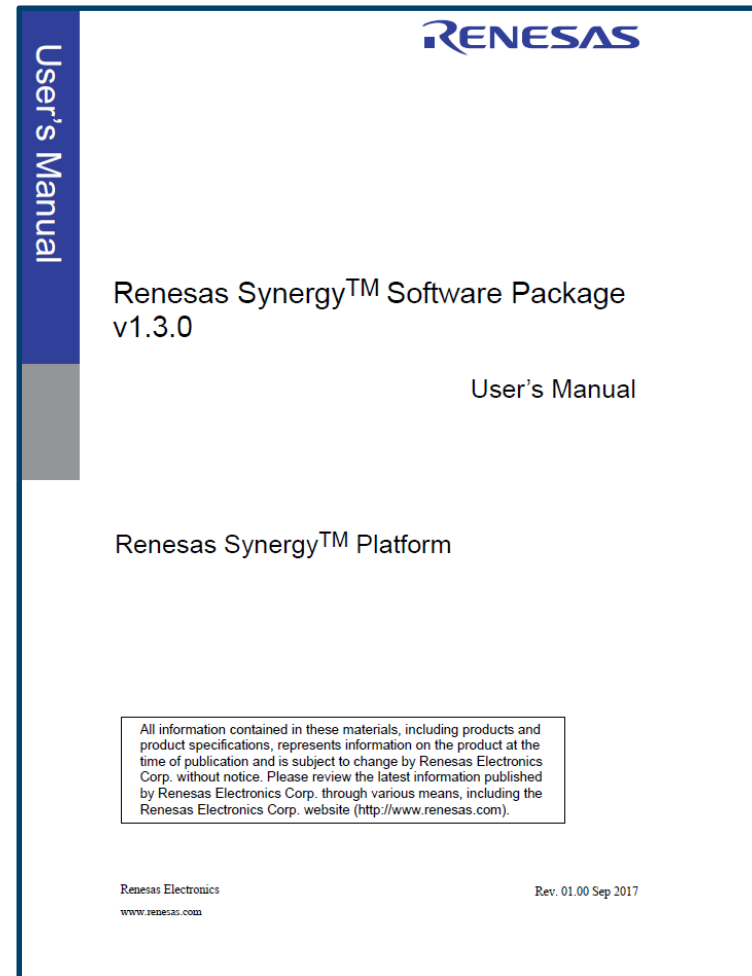
Established dedicated SDA team, also working with external auditing:

- Software Quality Assurance plan.
- Requirements traceability throughout development.
- SQA metrics & reports available to customers.

Subject to Change







Quality: Software data sheets

- **For Synergy Software Package (SSP) and QSA:**
- Published and maintained on Renesas Gallery.
- Specifications and performance metrics tested and documented.
- Benchmarks, code size, context switch times, latencies, execution times...
- Basis of SSP warranty

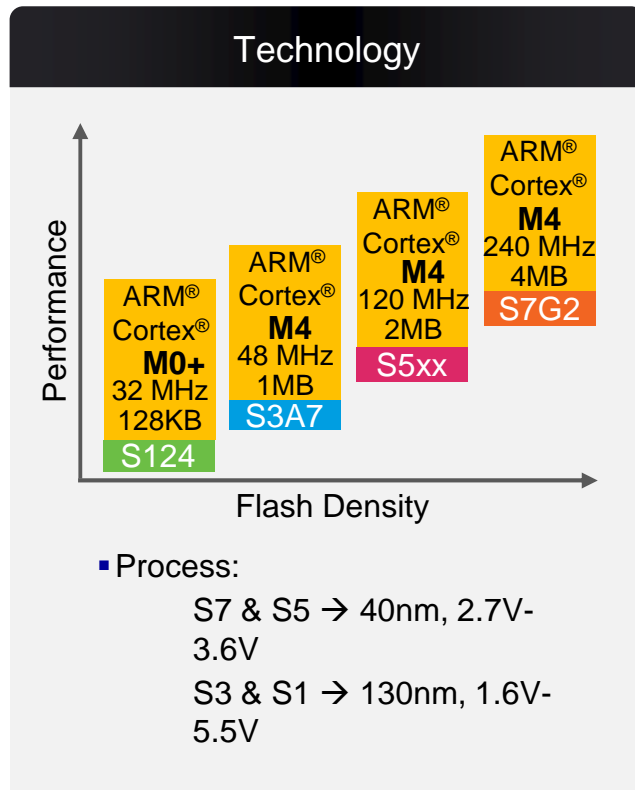


3488 pages !

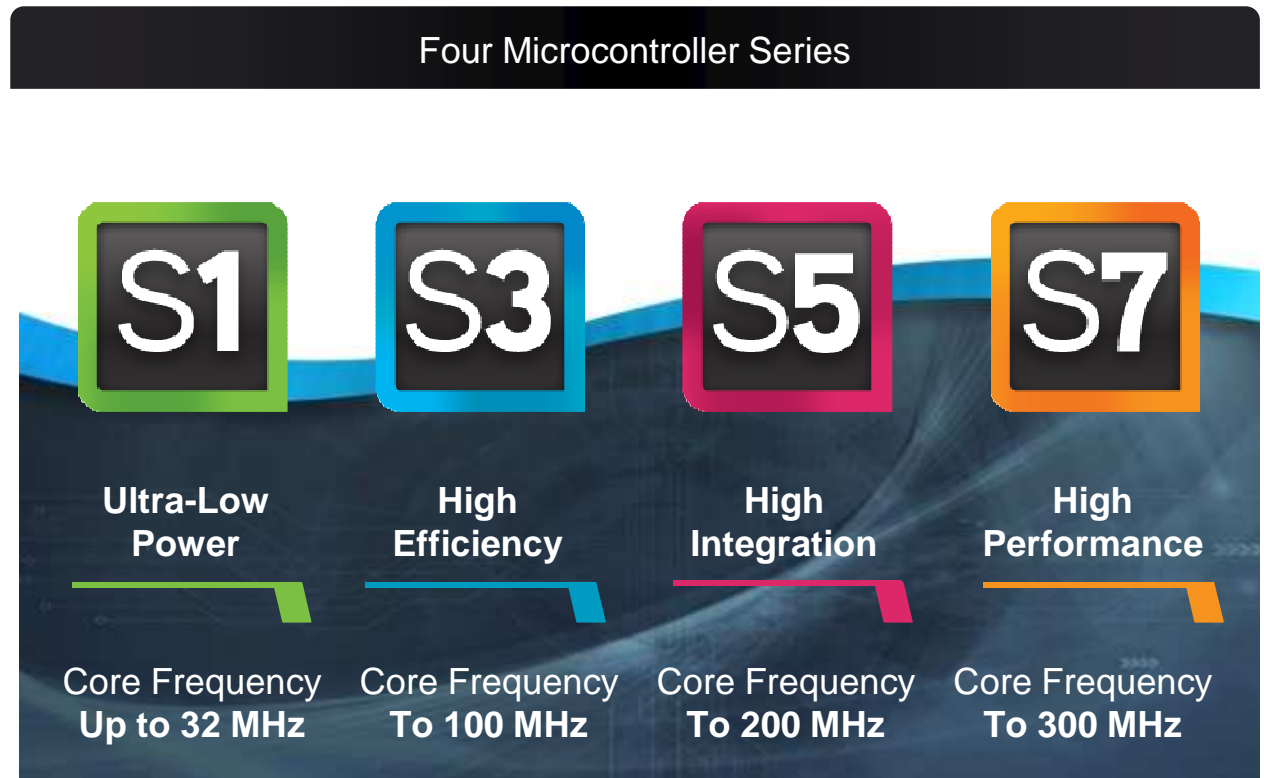
Support: Renesas as single point of contact

 Online Chat <ul style="list-style-type: none">• 24/5 technical support via online chat• Renesas Synergy™ trained operators	 Forum & FAQ <ul style="list-style-type: none">• Renesas Rulz moderated forum by Renesas Synergy specialist• Renesas Synergy Platform Knowledge Database and FAQs	 Smart Documentation <ul style="list-style-type: none">• Extensive Renesas Synergy Software & hardware documentation• Wiki-based and Context aware
 Application Engineers <ul style="list-style-type: none">• Application Engineers accessible via established sales routes	 IDH network <ul style="list-style-type: none">• From specific tasks to turn-key designs• Often near you in local language	 On-site Training <ul style="list-style-type: none">• On-site trainings of various scope and venues• At customer site, distribution site or public

Renesas Synergy™ Microcontrollers



- Operating temperature range:
 - 40°C to 105°C



Synergy MCU Packages BY MCU Group

As of SEP 2017: S7G2, S5D9, S5D5, S3A7, S3A6, S128, S124 MCU Groups



17



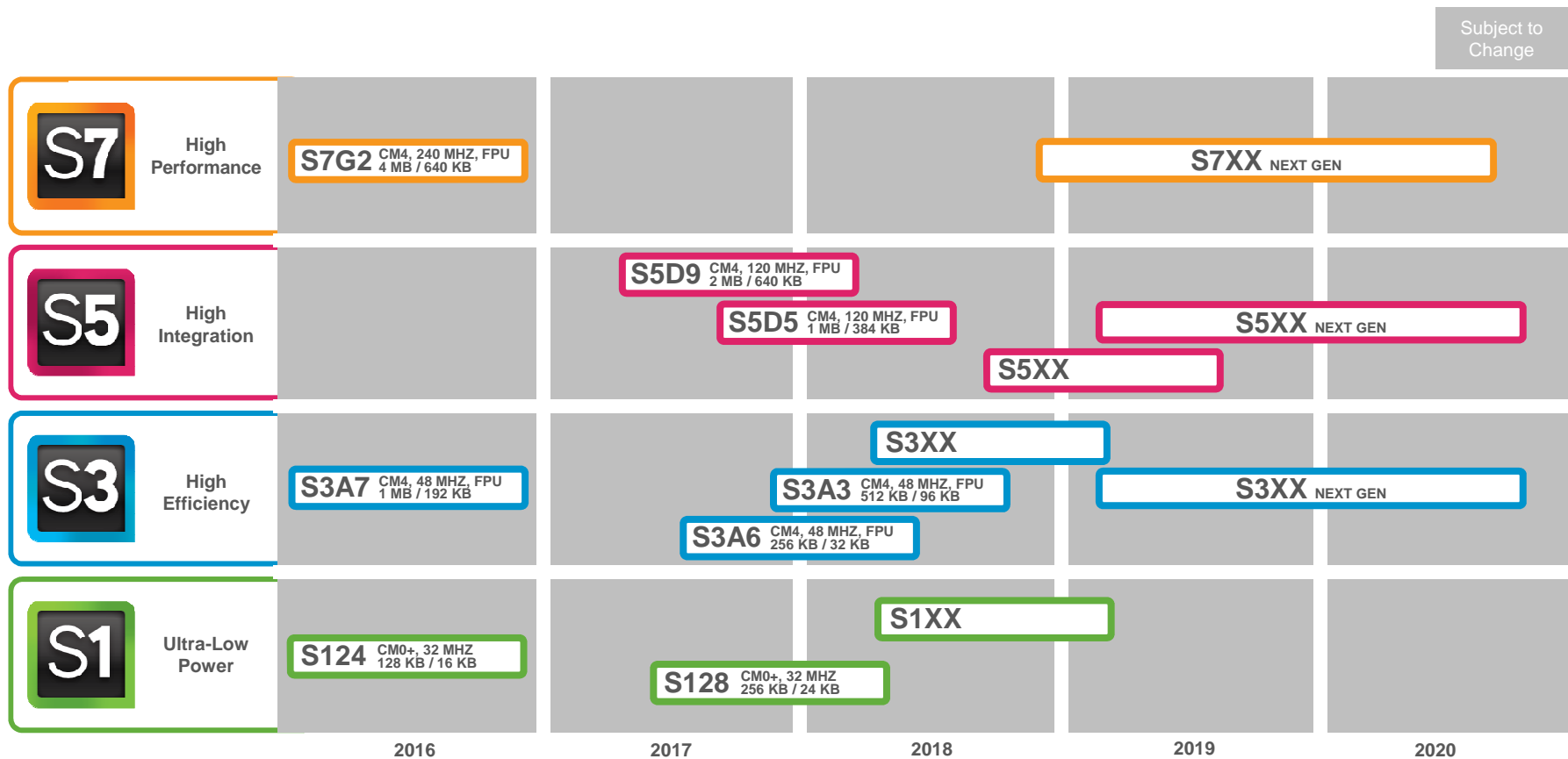
13 October 2017

Confidential

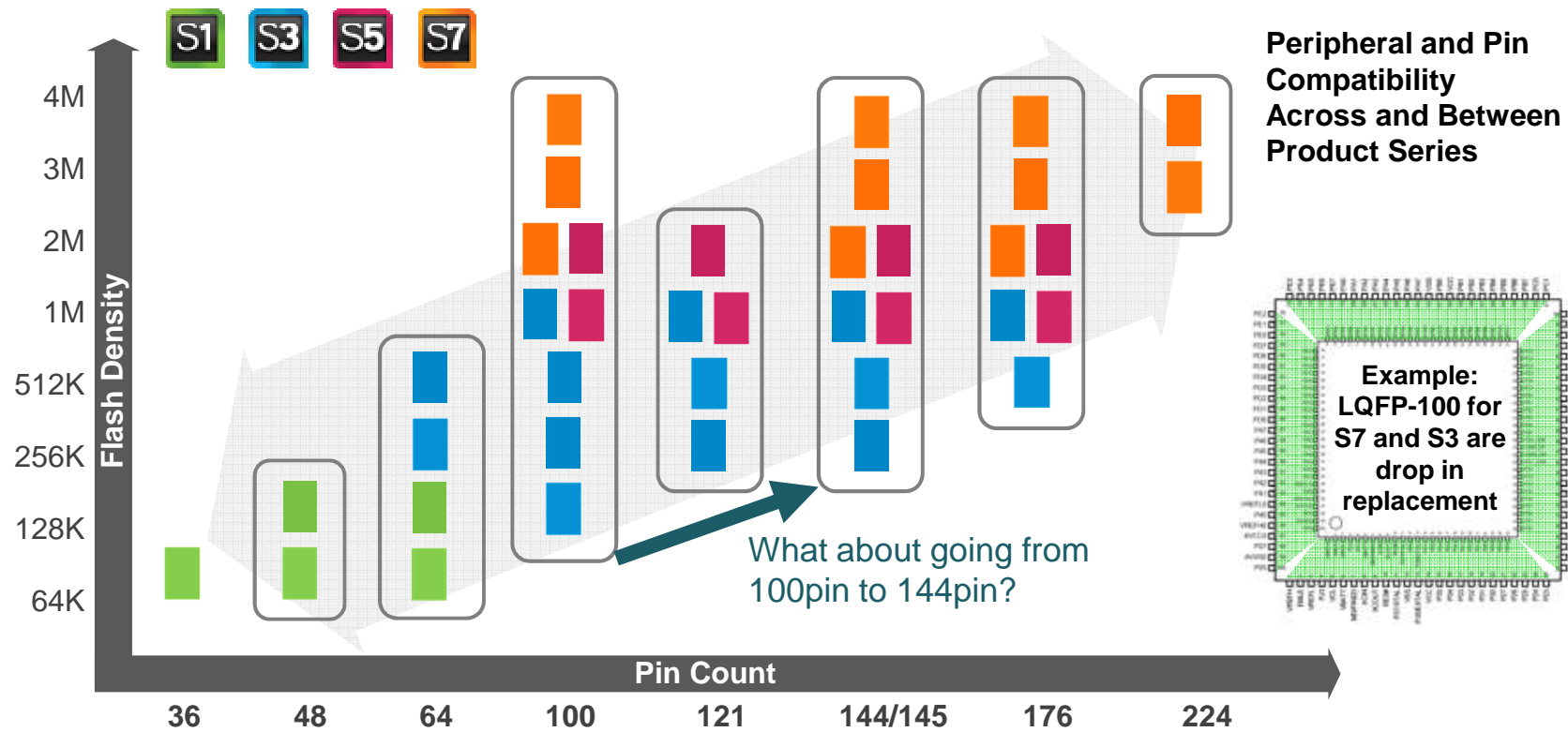
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Synergy Platform Roadmap

as Of Sep 2017: Includes MCU, SSP, Tools, Kits, Solutions

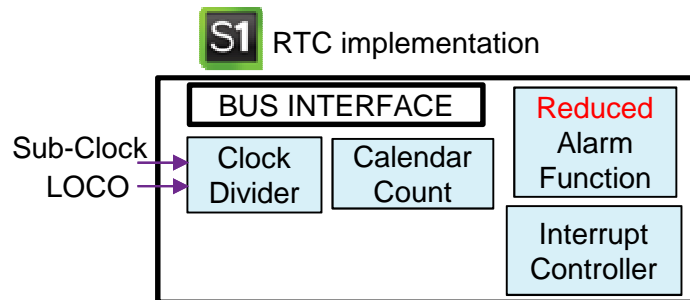


Microcontroller Portfolio

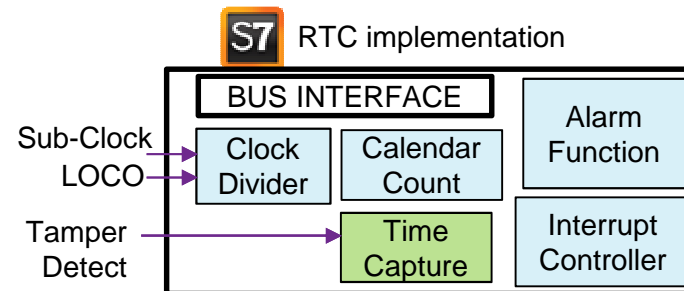


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Synergy Has Scalable Peripherals



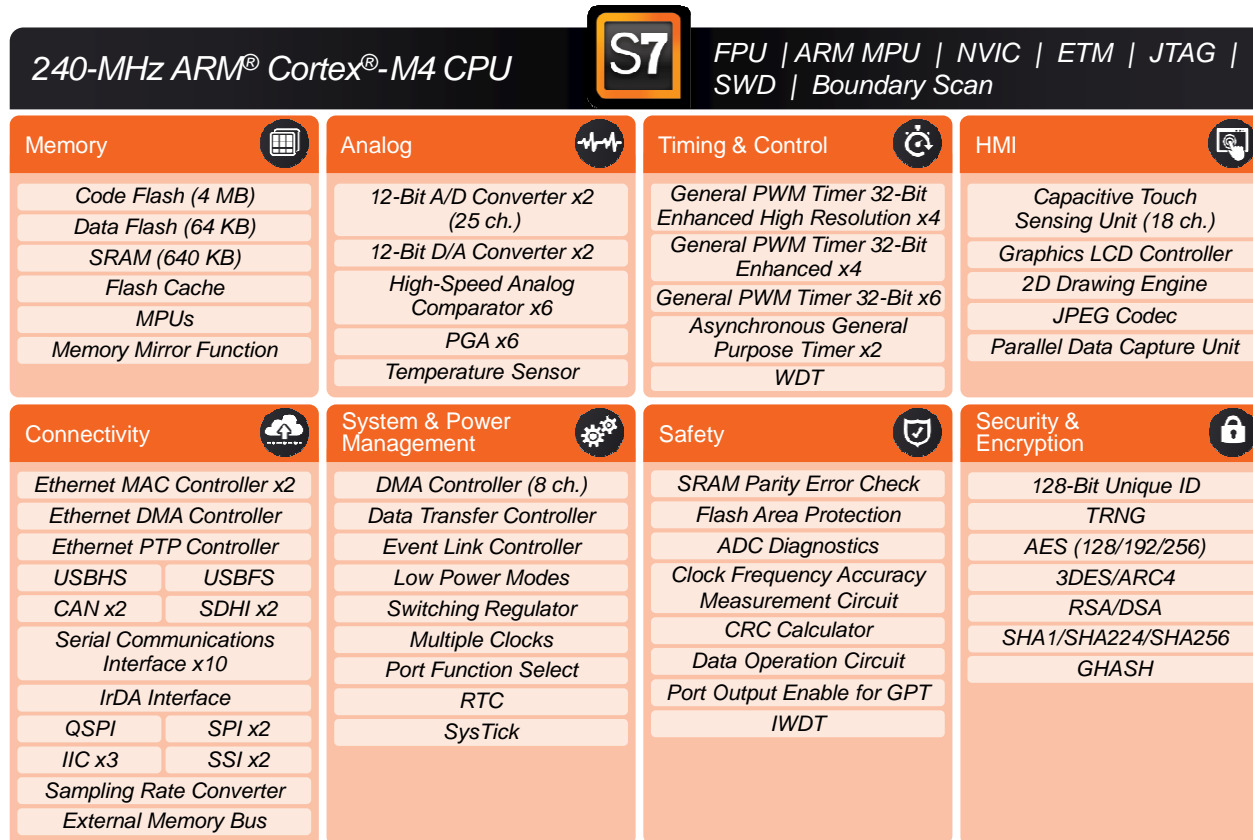
4004 4000h		R64CNT
4004 400Eh		RYRCNT
4004 4010h		RSECAR
4004 401Eh		RYRAREN
4004 4010h		RSECAR
4004 401Eh		RYRAREN
4004 4022h		RCR1
4004 402Eh		RADJ
4004 4022h		RCR1
4004 402Eh		RADJ
4004 4040h		RTCCRy
4004 405Ch		RMONCPy



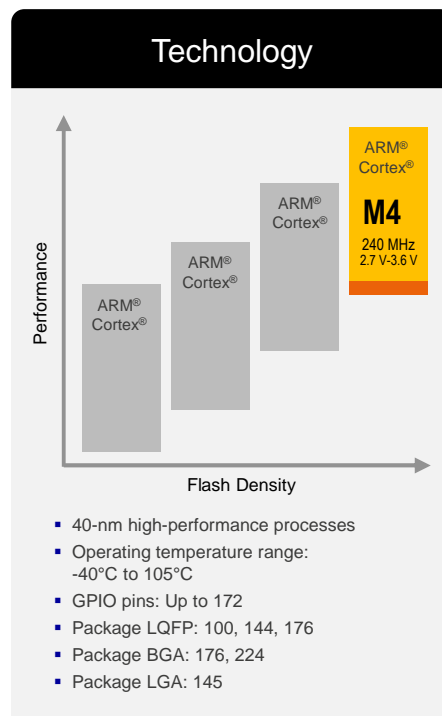
4004 4000h		R64CNT
4004 400Eh		RYRCNT
4004 4010h		RSECAR
4004 401Eh		RYRAREN
4004 4010h		RSECAR
4004 401Eh		RYRAREN
4004 4022h		RCR1
4004 402Eh		RADJ
4004 4022h		RCR1
4004 402Eh		RADJ
4004 4040h		RTCCRy
4004 405Ch		RMONCPy

- Physical features of the peripheral in the S1 MCU is a pure orthogonal subset of the features in the S7 MCU
- The control registers have no dependencies as they are scaled down to a lower feature set
- The control register address offsets are constant even as features are removed

Synergy MCU S7 Series

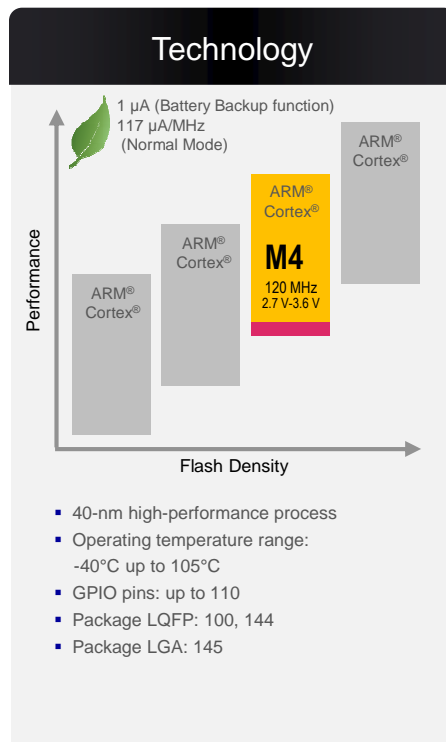


Example - Synergy S7 Series MCUS – High End



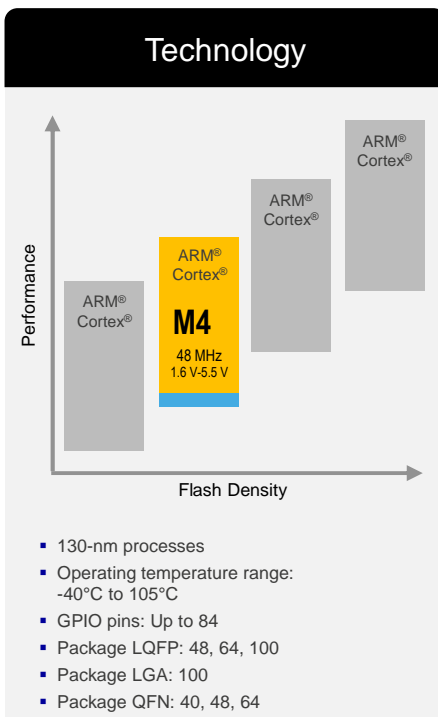
240 MHz ARM® Cortex®-M4 CPU S7G2 FPU ARM MPU NVIC ETM JTAG SWD Boundary Scan			
Memory <ul style="list-style-type: none"> Code Flash (4 MB) Data Flash (64 KB) SRAM (640 KB) Flash Cache MPUs Memory Mirror Function 	Analog <ul style="list-style-type: none"> 12-Bit A/D Converter x2 (25 ch.) 12-Bit D/A Converter x2 High Speed Analog Comparator x6 PGA x6 Temperature Sensor 	Timing & Control <ul style="list-style-type: none"> General PWM Timer 32-Bit Enhanced High Resolution x4 General PWM Timer 32-Bit Enhanced x4 General PWM Timer 32-Bit x6 Asynchronous General Purpose Timer x2 WDT 	HMI <ul style="list-style-type: none"> Capacitive Touch Sensing Unit (18 ch.) Graphics LCD Controller 2D Drawing Engine JPEG Codec Parallel Data Capture Unit
Connectivity <ul style="list-style-type: none"> Ethernet MAC Controller x2 Ethernet DMA Controller Ethernet PTP Controller USBHS USBFS CAN x2 SDHI x2 Serial Communications Interface x10 IrDA Interface QSPI SPI x2 IIC x3 SSI x2 Sampling Rate Converter External Memory Bus 	System & Power Management <ul style="list-style-type: none"> DMA Controller (8 ch.) Data Transfer Controller Event Link Controller Low Power Modes Multiple Clocks Port Function Select RTC SysTick 	Safety <ul style="list-style-type: none"> SRAM Parity Error Check Flash Area Protection ADC Diagnostics Clock Frequency Accuracy Measurement Circuit CRC Calculator Data Operation Circuit Port Output Enable for GPT IWDT 	Security & Encryption <ul style="list-style-type: none"> 128-bit Unique ID TRNG AES (128/192/256) 3DES/ARC4 RSA/DSA SHA1/SHA224/SHA256 GHASH

Example - Synergy S5 Series MCUS – Mid Range



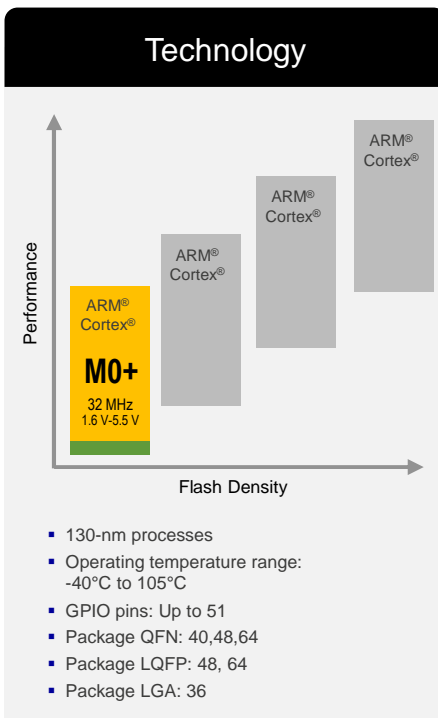
120 MHz ARM® Cortex®-M4 CPU S5D5 FPU ARM MPU NVIC ETM JTAG SWD Boundary Scan			
Memory <ul style="list-style-type: none"> Code Flash (512KB or 1 MB) Data Flash (32 KB) SRAM (384 KB) Flash Cache MPUs Memory Mirror Function 	Analog <ul style="list-style-type: none"> 12-Bit A/D Converter x2 (22 ch.) 12-Bit D/A Converter x2 High Speed Analog Comparator x8 Temperature Sensor 	Timing & Control <ul style="list-style-type: none"> General PWM Timer 32-Bit Enhanced High Resolution x4 General PWM Timer 32-Bit Enhanced x4 General PWM Timer 32-Bit x6 Asynchronous General Purpose Timer x2 WDT 	HMI <ul style="list-style-type: none"> Capacitive Touch Sensing Unit (18 ch.) Parallel Data Capture Unit
Connectivity <ul style="list-style-type: none"> Ethernet MAC Controller Ethernet DMA Controller USBFS Host/Device CAN x2 SDHI x2 Serial Communications Interface x10 IrDA Interface QSPI SPI x2 IIC x3 SSI x2 Sampling Rate Converter External Memory Bus 	System & Power Management <ul style="list-style-type: none"> DMA Controller (8 ch.) Data Transfer Controller Event Link Controller Low Power Modes Multiple Clocks Port Function Select RTC SysTick 	Safety <ul style="list-style-type: none"> ECC in SRAM SRAM Parity Error Check Flash Area Protection ADC Diagnostics Clock Frequency Accuracy Measurement Circuit CRC Calculator Data Operation Circuit Port Output Enable for GPT IWDT 	Security & Encryption <ul style="list-style-type: none"> 128-bit Unique ID TRNG AES (128/192/256) 3DES/ARC4 RSA/DSA SHA1/SHA224/SHA256 GHASH

Example - Synergy S3 Series MCUS – Mid Range



48 MHz ARM® Cortex®-M4 CPU			
S3A6			
FPU ARM MPU NVIC ETB JTAG SWD Boundary Scan			
Memory <ul style="list-style-type: none"> Code Flash (256 KB) Data Flash (8 KB) SRAM (32 KB) Flash Cache Memory Protection Unit 	Analog <ul style="list-style-type: none"> 14-Bit A/D Converter (28 ch.) 12-Bit D/A Converter Low-Power Analog Comparator x2 OPAMP x4 Temperature Sensor 	Timing & Control <ul style="list-style-type: none"> General PWM Timer 32-Bit x2 General PWM Timer 16-Bit x6 Asynchronous General Purpose Timer x2 WDT 	HMI <ul style="list-style-type: none"> Capacitive Touch Sensing Unit (27 ch.) Segment LCD Controller
Connectivity <ul style="list-style-type: none"> USBFS CAN SDHI/ MMC Serial Communications Interface QSPI IIC x2 SPI x2 SSI 	System & Power Management <ul style="list-style-type: none"> DMA Controller (4 ch.) Data Transfer Controller Event Link Controller Low Power Modes Multiple Clocks Port Function Select RTC SysTick Low Voltage Detection 	Safety <ul style="list-style-type: none"> ECC in SRAM SRAM Parity Error Check Flash Area Protection ADC Diagnostics Clock Frequency Accuracy Measurement Circuit CRC Calculator Data Operation Circuit Port Output Enable for GPT IWDT 	Security & Encryption <ul style="list-style-type: none"> 128-Bit Unique ID TRNG AES (128/ 256) GHASH

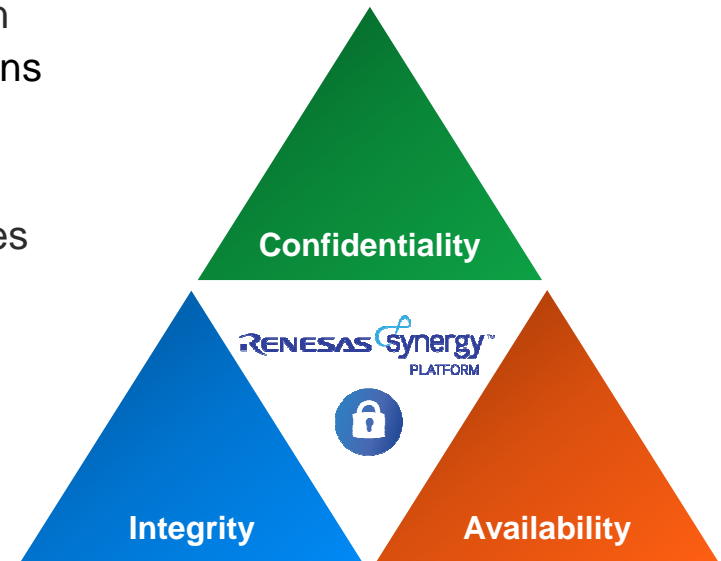
Example - Synergy S1 Series MCUS – Low End



32 MHz ARM® Cortex®-M0+ CPU S124 NVIC SWD MTB			
Memory <ul style="list-style-type: none"> Code Flash (up to 128 KB) Data Flash (4 KB) SRAM (16 KB) 	Analog <ul style="list-style-type: none"> 14-Bit A/D Converter (18 ch.) 12-Bit D/A Converter Low-Power Analog Comparator x2 Temperature Sensor 	Timing & Control <ul style="list-style-type: none"> General PWM Timer 32-Bit General PWM Timer 16-Bit x6 Asynchronous General Purpose Timer x2 WDT 	HMI <ul style="list-style-type: none"> Capacitive Touch Sensing Unit (31 ch.)
Connectivity <ul style="list-style-type: none"> USBFS CAN Serial Communications Interface x3 SPI x2 IIC x2 	System & Power Management <ul style="list-style-type: none"> Data Transfer Controller Event Link Controller Low Power Modes Multiple Clocks Port Function Select RTC SysTick 	Safety <ul style="list-style-type: none"> SRAM Parity Error Check Flash Area Protection ADC Diagnostics Clock Frequency Accuracy Measurement Circuit CRC Calculator Data Operation Circuit Port Output Enable for GPT IWDT 	Security & Encryption <ul style="list-style-type: none"> 128-Bit Unique ID TRNG AES (128/256)

Synergy Enabling Confidentiality, Integrity & Availability

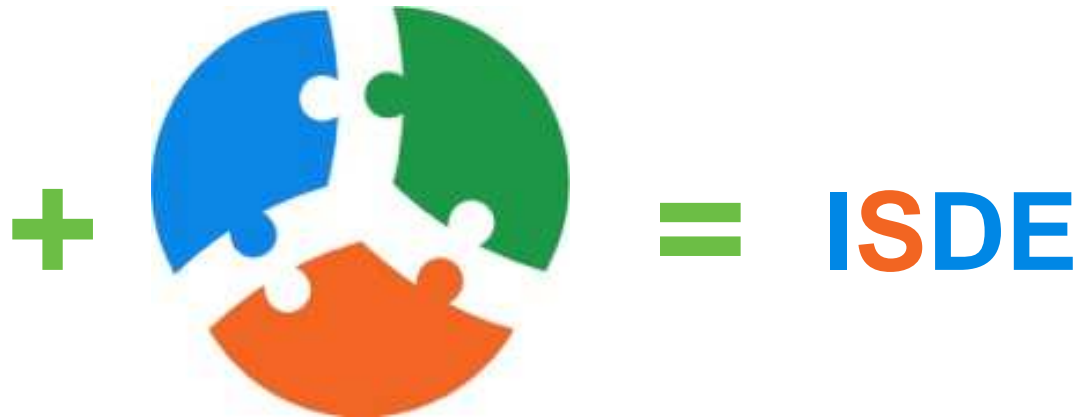
- Enabling **confidential** data and secure authentication
 - World class cryptography for secure communications
 - Secure authentication and identification
- Delivering platform **integrity** to enable trusted services
 - Root of trust to manage keys securely
 - Isolation of critical code to restrict attacks
 - Authenticated boot capability
 - Secure JTAG (Debug) access
- Safeguarding critical system **availability**
 - Isolation of critical system to help ensure uptime
 - Management of applications & system behaviour
 - Lifecycle management & secure updates



IDE vs. Synergy ISDE – New Age Development Environment



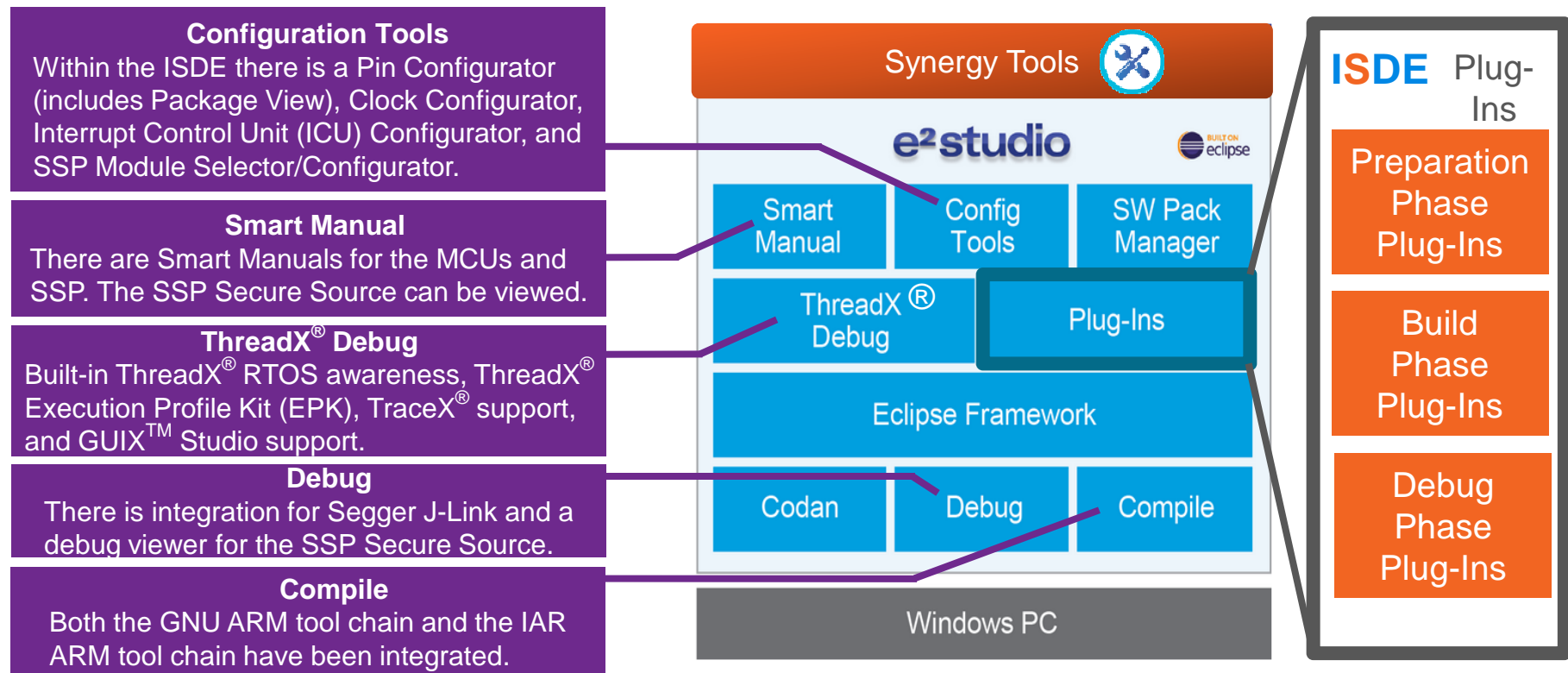
IDE
Integrated
Development
Environment



**Solution-oriented
components**

**Integrated
Solutions
Development
Environment**

Renesas Synergy™ Tools



Synergy MCU Smart Manual is within the e² studio ISDE

```
int main(void)
{
    while (1) {
        SYSTEM.SCK1.BYTE = 0;
    }
    return 0;
}
```

Highlight the MCU register name...

...brings up detailed information...

1010
0101 Counter-Clock Extension Register n (SYSTEM.SCK1)

Counter-Clock Extension Register n (SCKn) (n = 1, 2)

Address(es): SCK1 0008 C880h, SCK2 0008 C890h

Bit	Symbol	Bit Name	Description	R/W
b1 b2			0 0: MCLKD/TCLKD external pin input*1	

Synergy Software Smart Manual is within the e² studio ISDE

```
***** AMS_ERR_QUEUE_UNAVAILABLE Argument is not one of the predefined values
* @retval AMS_ERR_QUEUE_UNAVAILABLE Cannot open s/w queue
* @retval AMS_ERR_NULL_PTR Null pointer is(are) given
* @retval AMS_ERR_INTERNAL Internal error occurs
* @note This function is reentrant for any channel.<br>
* @note Handle must be cleared by caller before calling this function.
*****
ams_err_t AMS_UART_Open(ams_uart_dev_t * const p_dev, ams_uart_cfg_t * const p_cfg)
{
    ams_err_t err;
    drv_uart_cfg_t tmp_lower_lvl_cfg;


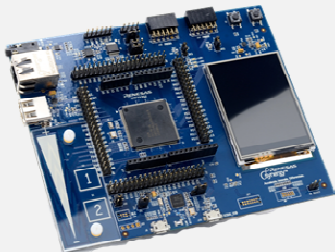

    /** (1) Checks error. Further parameter checking can be done at the driver layer. */
    #ifdef AMS_UART_CFG_PARAM_CHECKING_ENABLE
    if ((NULL == p_dev) || (NULL == p_cfg))
    {
        return AMS_ERR_NULL_PTR;
    }
    if (((((NULL == p_cfg->p_lower_lvl_api->open)
    || (NULL == p_cfg->p_lower_lvl_api->close))
    || (NULL == p_cfg->p_lower_lvl_api->control)))
```

Highlight the API name...

...brings up detailed information...

Name: AMS_UART_Open
Prototype: AMS_UART_Open(ams_uart_dev_t *const p_dev, ams_uart_cfg_t *const p_cfg)
Description:
This is one of AMS UART framework driver API, which opens a designated UART channel. UART framework driver, Open API. The open API acquires mutex/event flag objects and handles driver initialization at UART HAL layer.
Parameters:
p_dev - Handle for UART driver context for a channel(Value returns from this function). This value must be cleared by user.
p_cfg - UART configuration includes UART interface information which includes channel and API
Parameters:
AMS_SUCCESS - UART channel is successfully opened
AMS_ERR_BAD_CHAN - Illegal UART channel is specified
AMS_ERR_OMITTED_CHAN - Omitted UART channel is specified
AMS_ERR_CH_NOT_CLOSED - UART channel have already been opened
AMS_ERR_BAD_MODE - Unsupported or incorrect mode
AMS_ERR_INVALID_ARG - Argument is not one of the predefined values
AMS_ERR_QUEUE_UNAVAILABLE - Cannot open s/w queue

Renesas Synergy™ Kits

Parameters	Target Board (TB)	Starter Kits (SK)	Development Kits (DK)
Footprint			
Purpose	MCU sample on PCB	Synergy Platform introduction and first steps	Complete project prototyping
MCU Pin Access	All pins	Most Pins	All Pins
Expandability/Connectors	Pmod footprint	Arduino and Pmod	Expansion and Pmod
SSP Qualification Basis	Limited	Yes	Yes
BLE Connectivity	✗	✓	Most
On-board J-Link® Debugger	✓	✓	✓
Suggested Retail Price	Low cost, about 30 USD	Typically less than a hundred USD	Typically a few hundred USD

Renesas Synergy™ Solutions

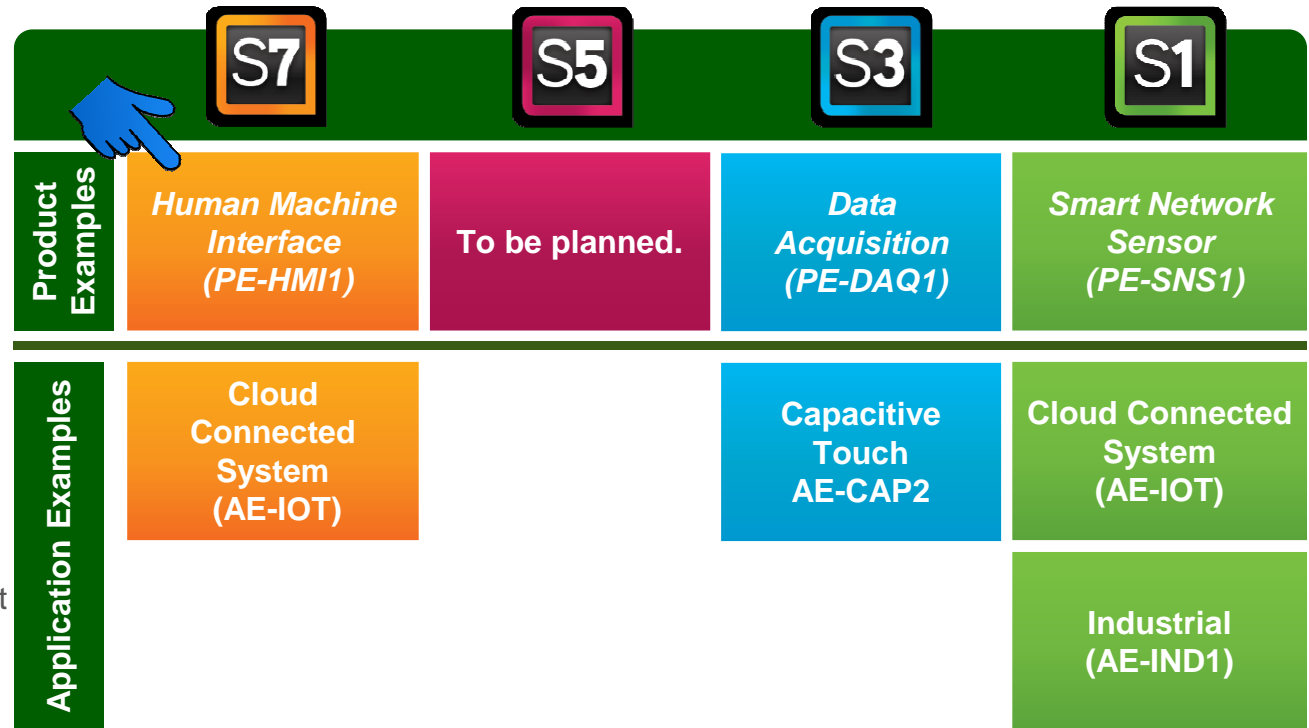
Starting points that you can count on

Product Examples

- Custom hardware which is a design instance of an end product
- Contains design journey document describing design considerations
- Includes e²studio project, BOM, schematics, and board layout files

Application Examples

- Example code running on standard Renesas Synergy hardware kit showcasing specific hardware and software components
- Contains Application Note document
- Includes e²studio project



HMI Product Example

- Represents one design instance of an HMI product
- PE + design journey documentation = jump start for application
- Reference platform to show graphics performance of S7G2 MCU + SSP
- Software demo thermostat
 - Extension to include audio framework for alarm sound
 - Extension to include a Pmod peripheral
 - Extension to control backlight using the ambient light sensor ALS

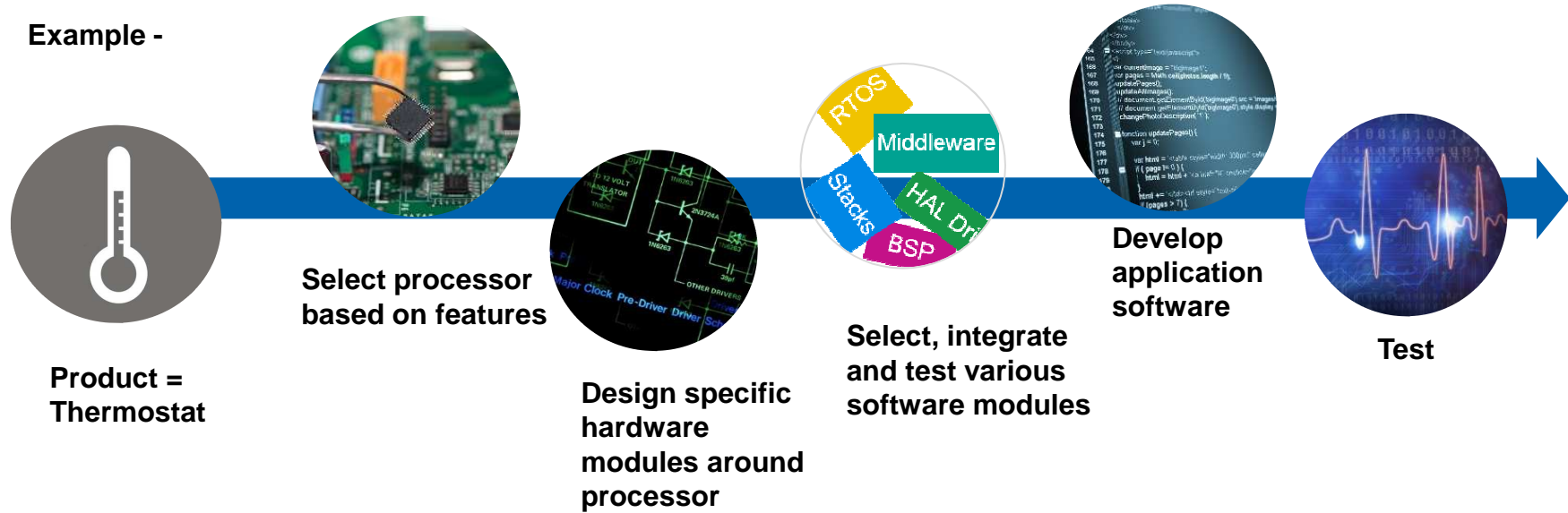


Platform-Based Development

Typical Embedded Development Process Today

Focused on features, hardware design, software integration

Example -



Focus is on development process

Synergy Changes the Development Process

Focus shifts to product experience and added value

Instead -



Focus is on customer's product experience, product innovations

A close-up photograph of a person's hands holding a white envelope. The person is wearing a dark suit jacket over a white shirt. The envelope is held in the right hand, with the left hand supporting it from below. A red banner with the word 'Summary' is overlaid on the image.

Summary

Summary

The only fully qualified Microcontroller platform solution available today

- Fully qualified, integrated and professional software platform design to work on synergy microcontrollers
- You can download it and use it today, with no upfront or license costs





Thank you!