Power Delivery Network Analysis

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CB Distribution

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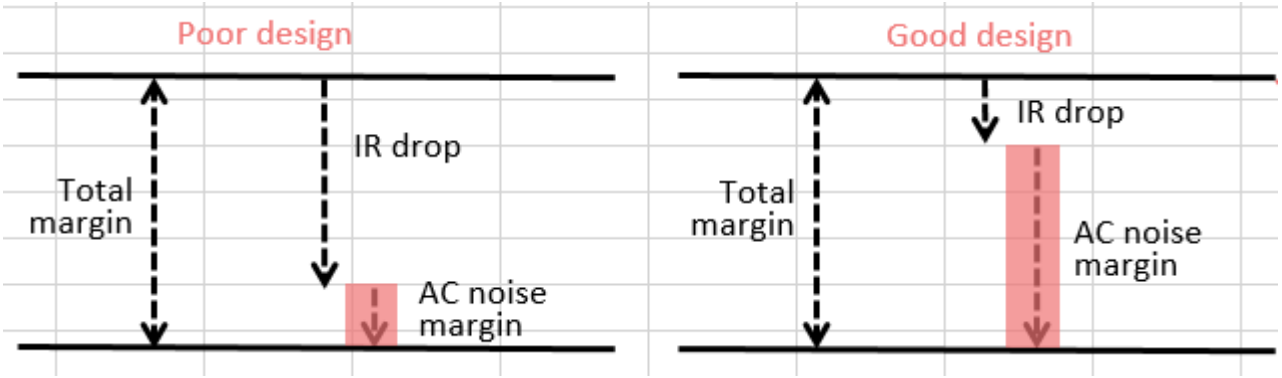
Agenda

- Why Power Delivery Network Analysis?
- Analysis types,
  - DC simulation
  - Thermal aware simulation
  - AC simulation
- PDN analysis at Prodrive Technologies
- Tools and integration

Why Is Power Distribution Analysis ?

- DC voltage is the most fundamental criterion for the operation of the circuitry in the system
  - The voltage supply is allowed to deviate by an amount specified by the vendor
  - This deviation (or fluctuation) of the supply is composed of DC loss and AC noise
  - The total voltage tolerance is commonly 5% (or less) of the nominal operating voltage
  - If the tolerance is constant, then a reduction in DC loss yields a larger AC noise budget



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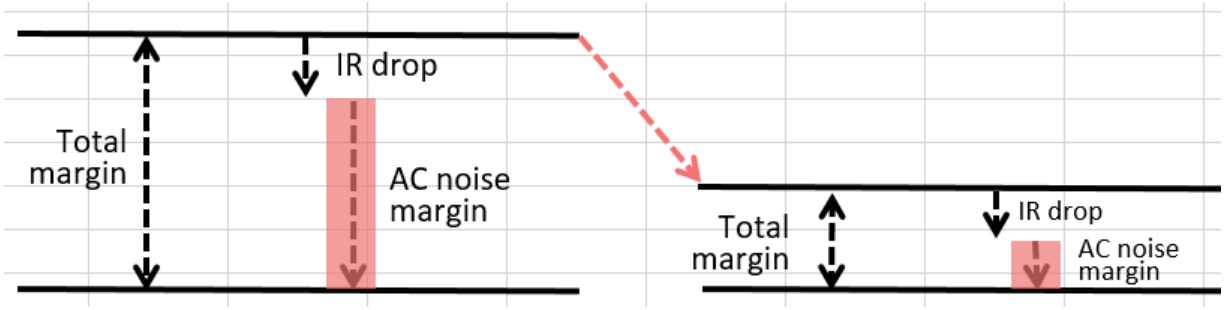
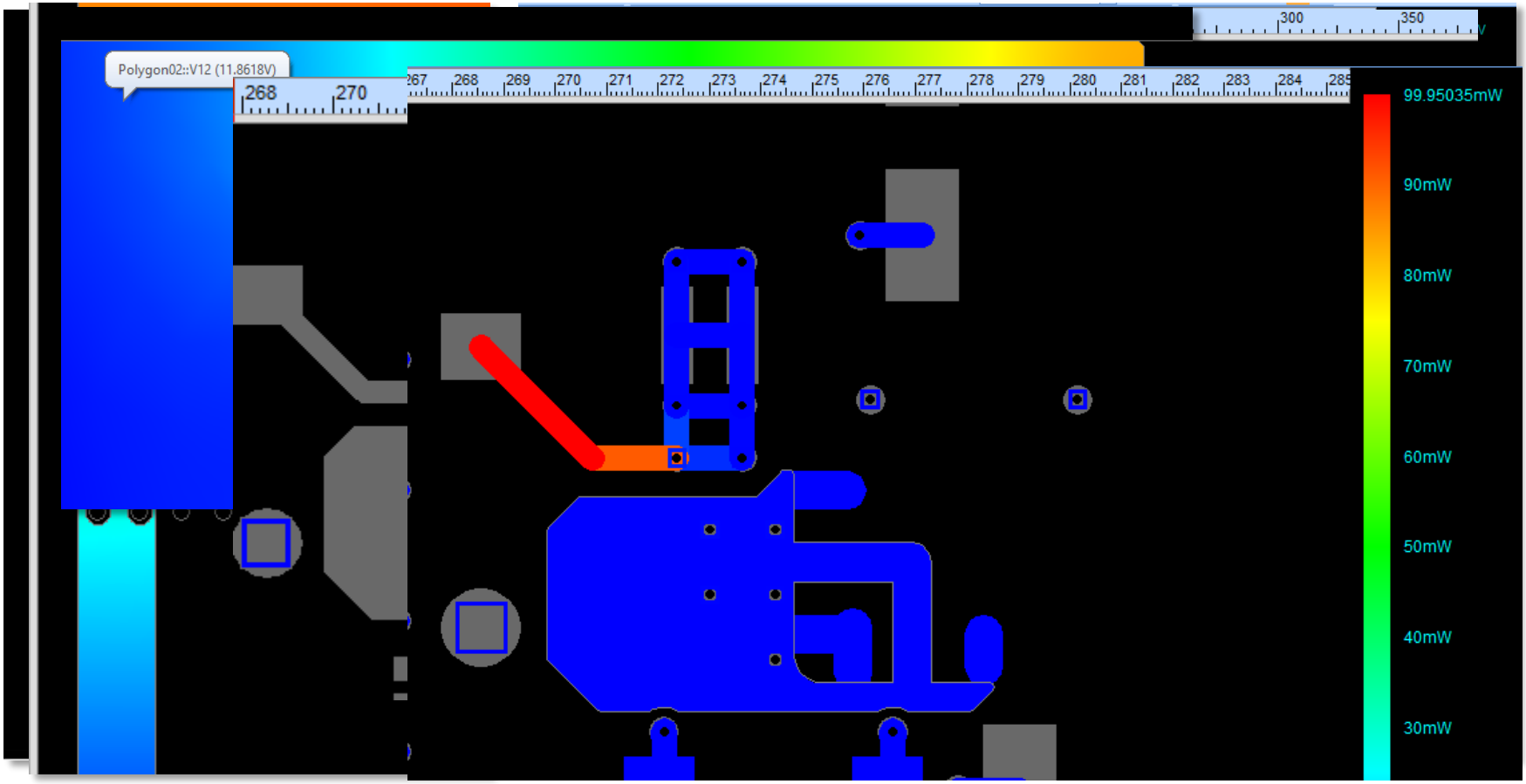
Why Power Analysis Is Important?

- Numerous factors have combined to exacerbate the problem
  - Core voltage levels continue to drop: 1.2V and less are now common. Total margin drops from 250mv to 60mv
  - As voltage is reduced, current requirements typically increase:
    IR drop = I * R
  - Miniaturization of electronics results in fewer layers and higher densities thus reducing the available area for power net



DC analysis

- With IR drop analysis you see
  - Voltage levels across the board
  - Current density



What about Thermal effects ?

- Heating due to current changes resistance of copper
- Without Thermal effect IR drop estimates will be inaccurate.
- High temperature due to localized current density can cause smoke or fire hazard
- Cadence DC analysis includes effects of
  - Component heating (power dissipation), including heatsinks
  - Joule heating (PCB copper)

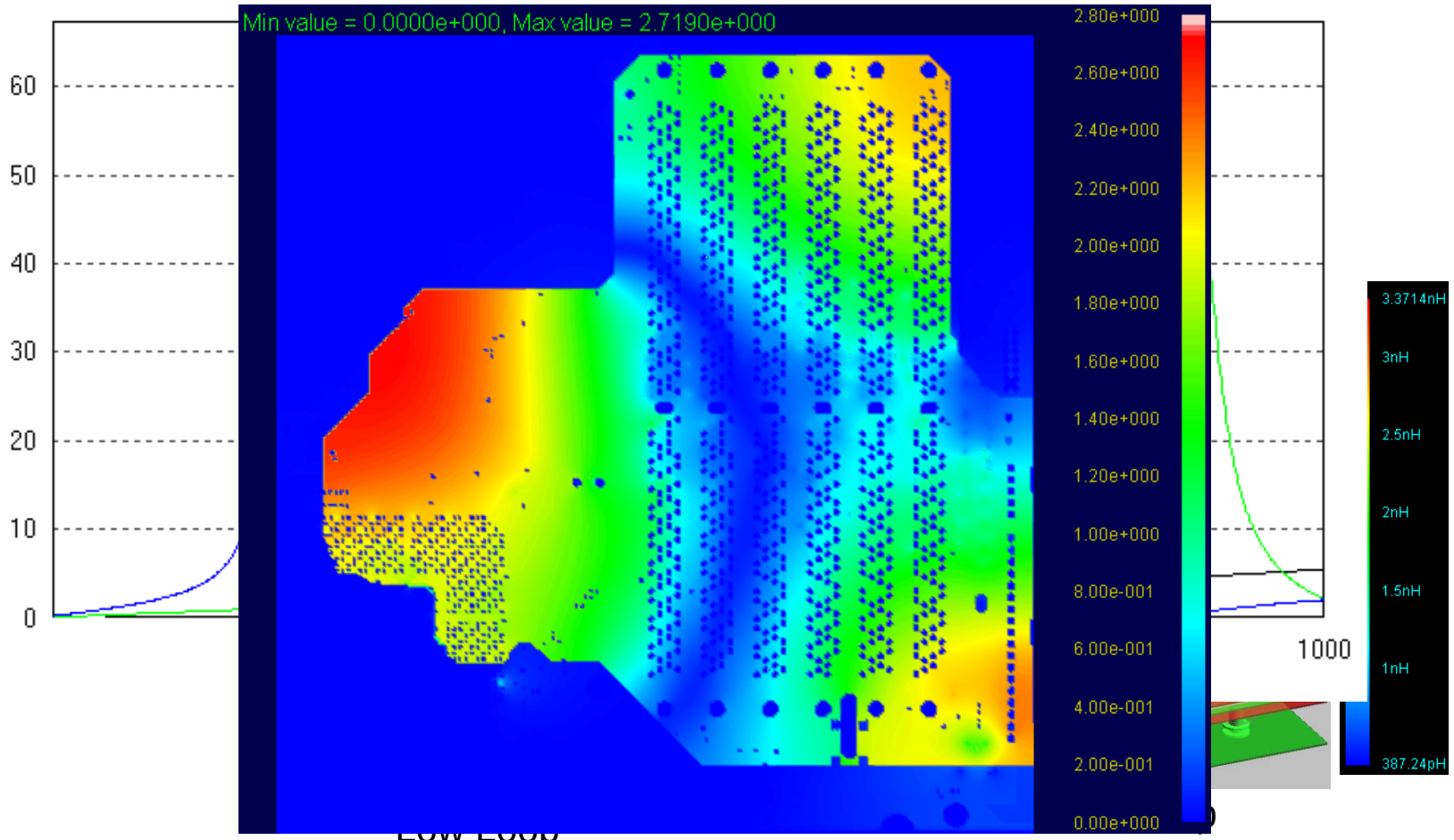
	Pure Heat Transfer Simulation (component heating only)	Electrical / Thermal Co-Simulation (component & Joule heating)	Effect of Joule Heating
Max Component Temperature	79 °C	85 °C	+6 °C
Max Board Temperature	72 °C	82 °C	+ 10 °C

Why AC power analysis?

- Switching circuit requires current to charge the load. VRM needs to supply this power
- VRM is unable to respond if output impedance exceeds target impedance.
  - Introduces switching noise: $Z_t = \frac{Vdd * ripple}{50\% * I_{max}}$
- Impedance should be smaller than Z_t at broad frequency range to lower switching noise.
- AC analysis calculates PDN impedance

How to lower impedance?

- Add decoupling capacitors, bulk/ceramic capacitors
  - AC analysis will locate impedance hotspots and helps to get correct capacitor locations
- Loop inductance reduction, effect at higher frequencies



Low Loop Inductance

Inductance

Design Decisions depending on PDN Analysis

- To determine proper metal thickness for power/gnd planes
- To find out
  - If and where to add additional via or power/gnd shape to ease the overheat
  - Whether to add additional plane layers needed in the board stackup
  - Power dissipation and temperature profiles in PKG/PCB
  - If and where to add sense line compensation for VRM
- Decoupling capacitors
  - Quantity, type and location

Prodrive Technologies

Bram Bruekers

- Since 2003 working at Prodrive Technologies
- Analogue / Mixed signal hardware design
- PCB design
  - 15+ years experience
  - High current & voltage
  - Low noise
- PCB tooling support & maintenance

Prodrive Technologies

- One of the fastest growing privately owned technology companies in Europe
- HQ located in Son, Netherlands
- International located: Germany, USA, Israel, China
- Design of electronics, software and mechanics
- Manufacturing
- Core competences
  - High end computing
  - Power conversion
  - Motion & mechatronics
  - Industrial automation
  - Vision & sensing
  - IoT
- Industries of main interest:
  - Industrial
  - Automotive
  - Infra & energy
  - Medical

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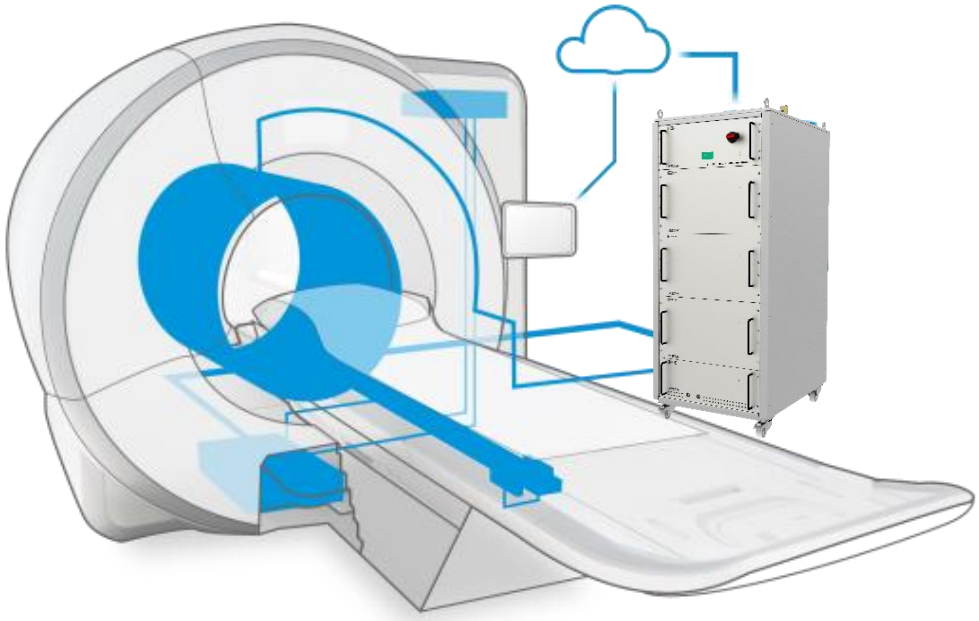
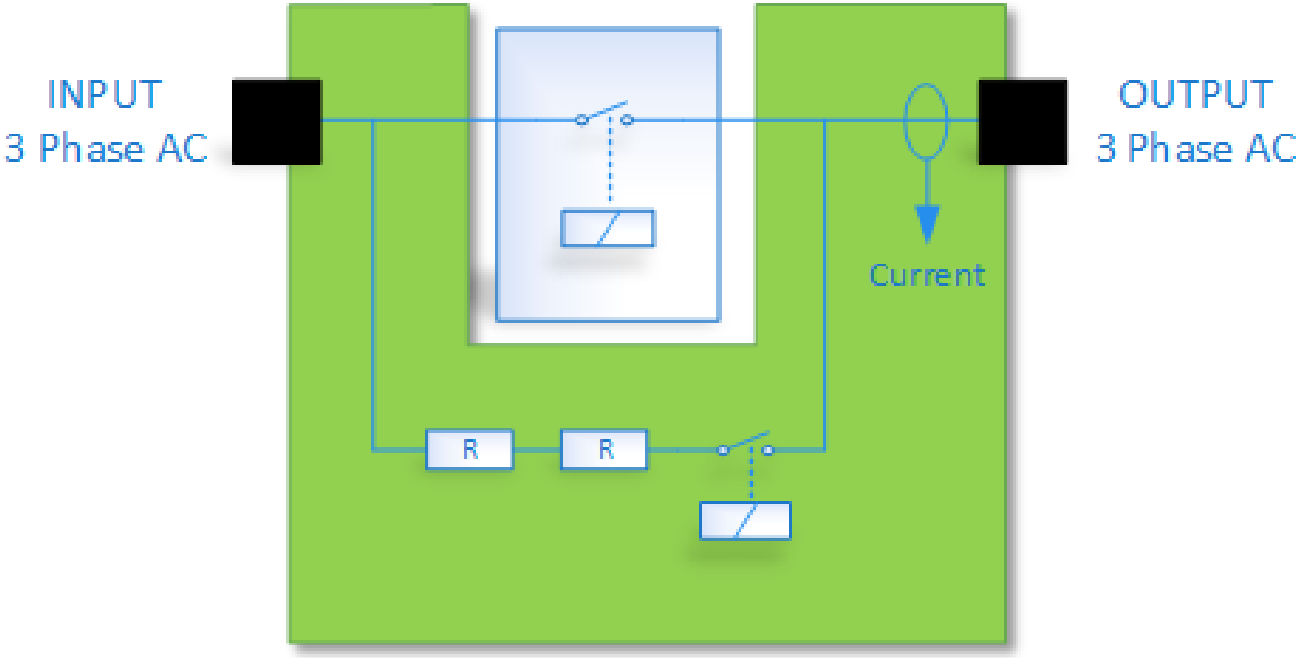
MRI Gradient Amplifier

- 3-axes gradient amplifier cabinet
- 2100V / ±1200A Patented end stage
- Maximum 45kW continuous output power for three axes
- Integrated high precision current sensors
- High reliability of >30,000 hours
- Lifetime: >10 years
- Multiple FRUs (Field Replaceable Units)



Mains Input Board

- Inrush current limiter
- Power distribution
- Integrated current measurements
- Designed for 3x 130A continuous



Design Choices

- What type of interconnection to use?

	Pro	Con
Cable	Easy / flexible routing	Assembly issues, many connections Where to place electronic circuits?
Bus-bar	current carrying capability	Difficult to ‘route’ through complex product Where to place electronic circuits?
PCB	Electronic circuits possible Ease of assembly	Complex design Heating

Design Choices

PCB

- Design complexity
  - How many layers ?
  - Copper weight ?
  - Total Thickness -> Limited by components !

- Thick copper
  - Lower temperature ?

    Not necessarily !
  - Higher costs + leadtime PCB FAB house
  - PCB Assembly issues

  So, thicker is not always better

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Simulation to make design choices

- PCB heating most critical factor for this circuit
  - Absolute voltage drop not interesting

- Initial stackup : 6 layers 4oz (~140µm) copper
  - Creating hotspots due to stackup, routing and plane cuts.
  - Long leadtime for raw material
  - UL certification for 140µm+ copper in several PCB FABs not available

- Final stackup : 12x 2oz (~70µm) copper
  - Hotspots are more spread because of overlapping planes
  - ‘Standard’ available materials = short lead time !

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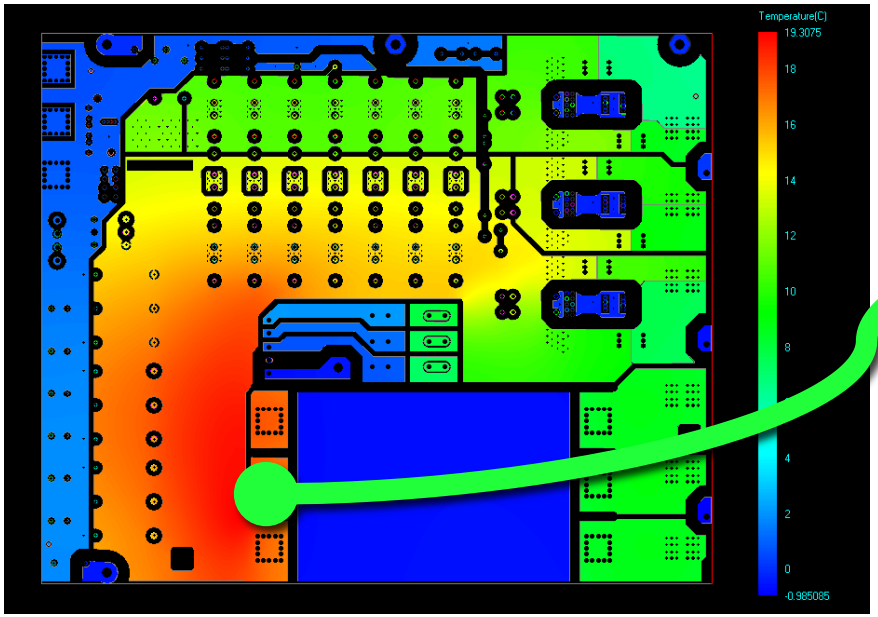
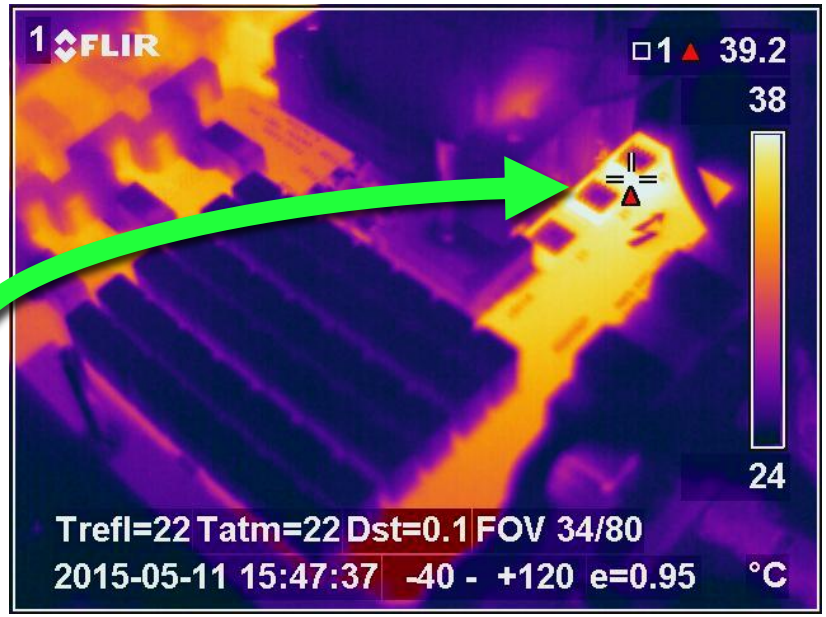
Comparison 2 PCB stack-ups

	Initial	Final design
# Layers	6	12
Copper weight	4oz	2oz
Material availability	-	+++
PCB costs	€€€€€	€€€
# PCB Fabs	-	+++

Simulated vs. Measured





ΔT simulated ~19˚C

ΔT measured ~16˚C

Total current of 390A
No airflow

Other practical applications

- Feasibility check
- Debugging

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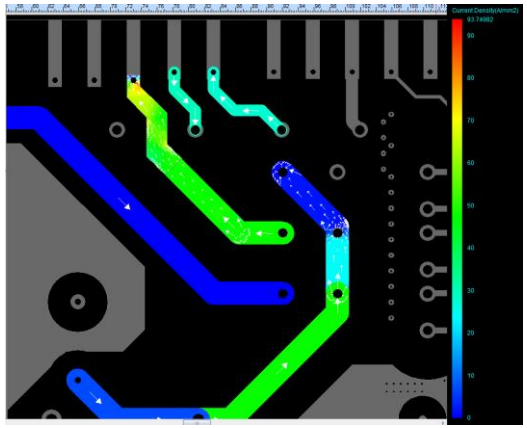
Feasibility

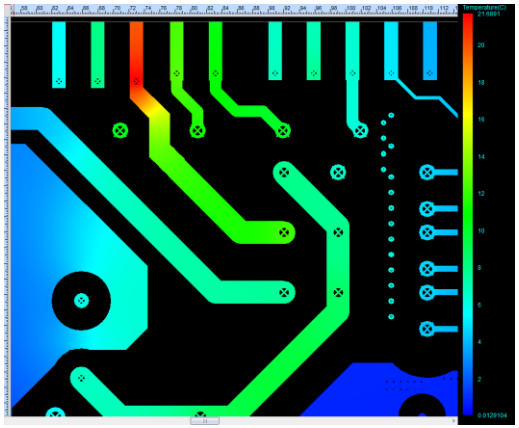
- Question from a customer:

  “Can the routing cope with a current of 7A?”

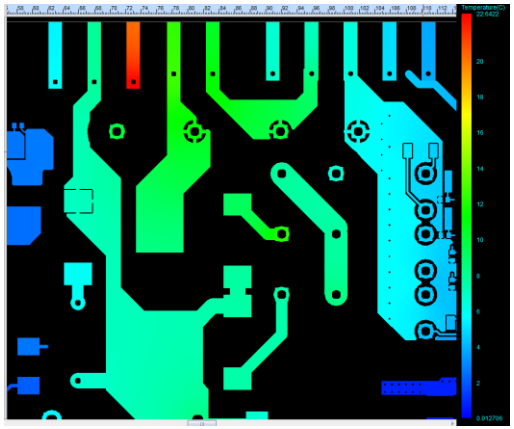
- Microcontroller board
  - Dense design, not much place for wide traces
- Used PowerDC to simulate the current through the specific part of the PCB
  - Result: Yes, routing can handle the specified current.
    Hotspot is caused by the connector.



Current density



Top

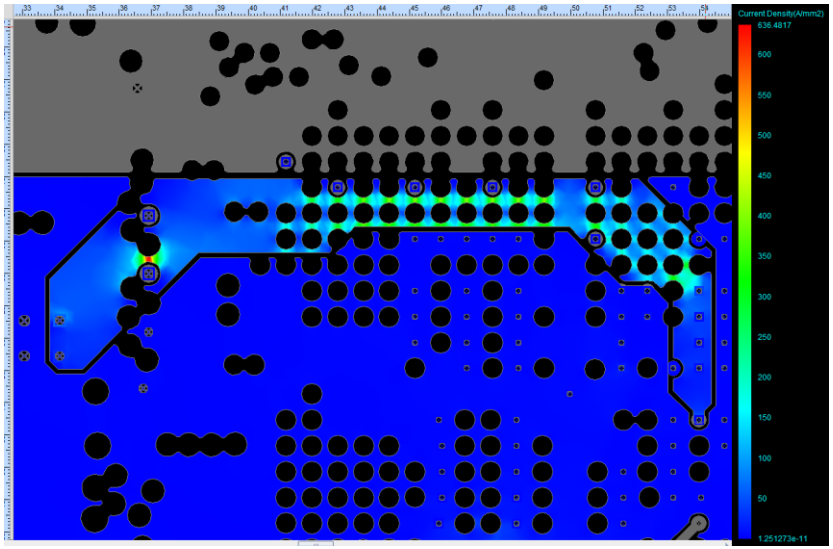


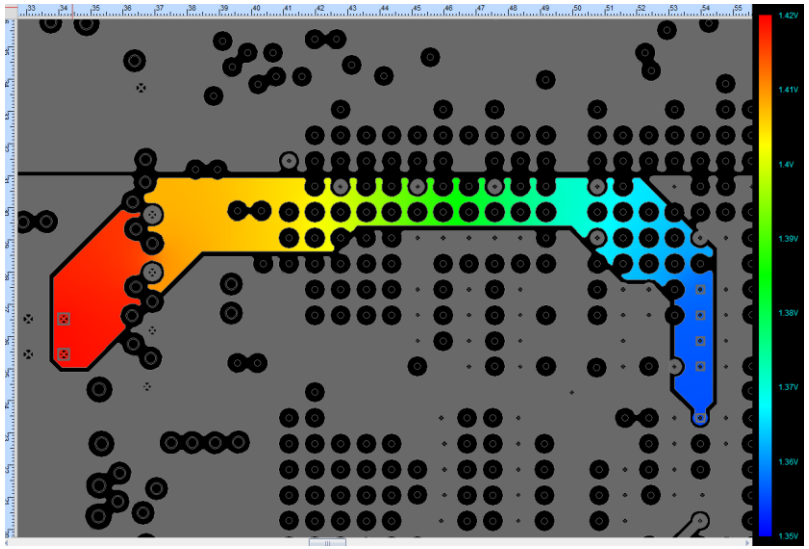
Bottom

ΔT simulated ~14˚C

Debugging

- Issue with core supply of microcontroller
  - Stability issues during qualification
- IR drop simulation to simulate the voltage drop from the supply to the microcontroller





- Last minute PCB change, extra VIAs were added
- ΔV is about 65mV → only ~5mV supply voltage margin!

Why we use PowerDC

- Initially usage:
  - High-current designs
    - IPC2221B / IPC2152 not possible to use on complex boards
  - Temperature rise of a PCB

- Now also for power distribution and voltage drop simulations

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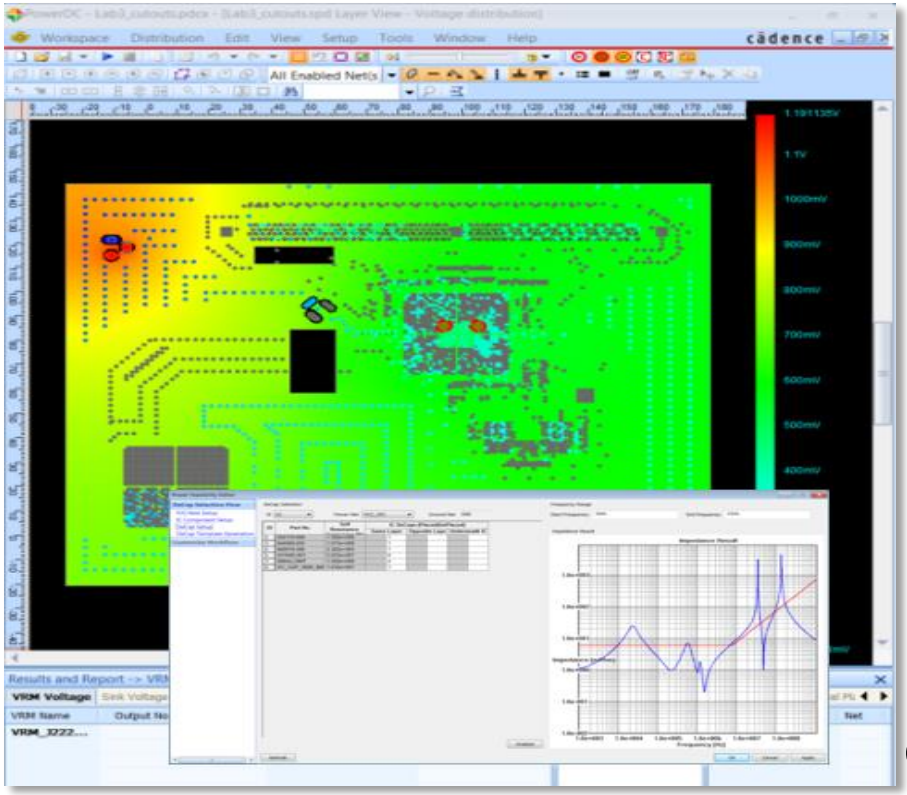
Integration with PCB tools

- Direct integration with OrCAD/Cadence PCB Editor
  - Use PI constraints during layout
  - DRC markers
- Capable to analyze designs from:
  - Altium
  - Mentor Graphics
  - ODB++
  - Zuken



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Automatic Report generation

PowerDC Simulation Report

1 General Information

1.1 Spd File Name and Location

PowerDC Version: 15.0.2.02061

File Names and Locations:

- Workspace File : D:/presentations/NordCAD/1503_Update/pi_sim_workshop/lab_d
- Layout File : D:/presentations/NordCAD/1503_Update/pi_sim_workshop/lab_data/s

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1.2 Board Stackup

Layer #	Layer Name	Thickness(mm)	Material	Conductivity(S/m)	Er	LossTangent	Fill-in Dielectric	ShapeName	TraceWidth(mm)	Roughness(mm)
1	SignalTOP	0.03048	COPPER		1	0		SignalSTOPpkgshape	0.1	0
	Medium41	0.2032	FR-4	0						
2	SignalL2-GND	0.03048	COPPER		4.5	0		PlaneSL2-GNDpkgshape	0.1	0
	Medium43	0.2032	FR-4	0						
3	SignalL3-PWR	0.03048	COPPER		4.5	0.035		PlaneSL3-PWRpkgshape	0.1	0
	Medium45	0.2032	FR-4	0						
4	SignalL4-PWR	0.03048	COPPER		4.5	0		PlaneSL4-PWRpkgshape	0.1	0
	Medium47	0.2032	FR-4	0						
5	SignalL5-GND	0.03048	COPPER		4.5	0		PlaneSL5-GNDpkgshape	0.1	0
	Medium49	0.2032	FR-4	0						
6	SignalBOTTOM	0.03048	COPPER		1	0		SignalSBOTTOMpkgshape	0.1	0
	Total Thickness	1.19888								

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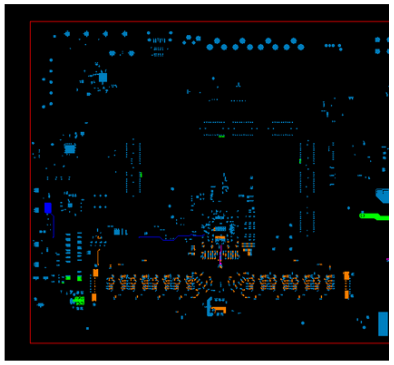
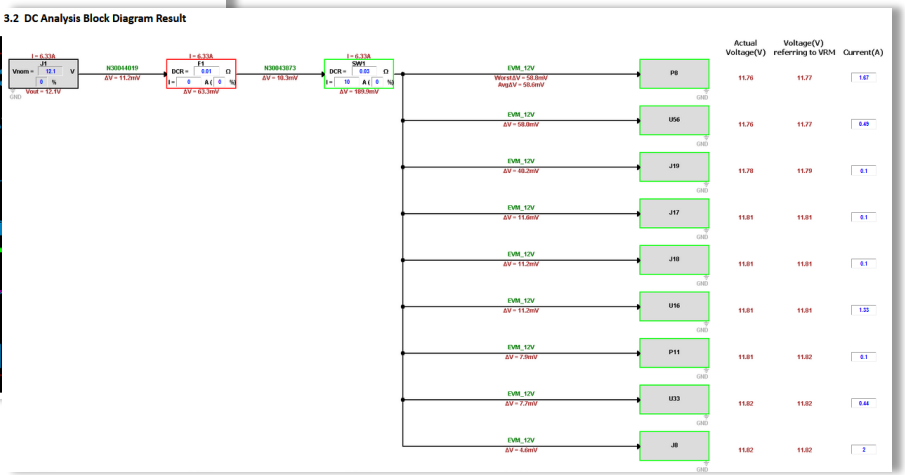
1.3 Layout Top and Bottom Layer views

1.3.1 Layout Top Layer View with Enabled Nets only



3.2 DC Analysis Block Diagram Result



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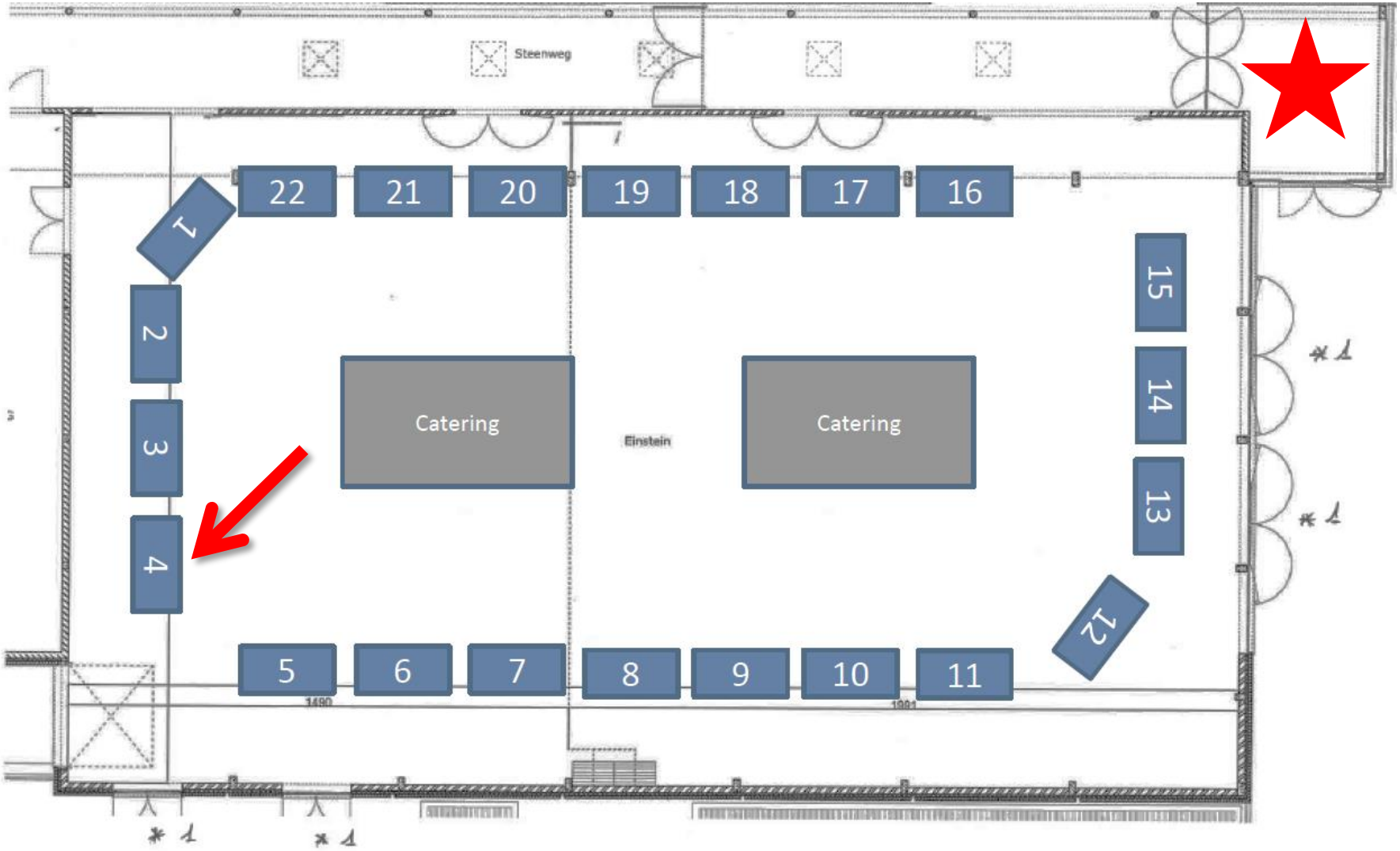
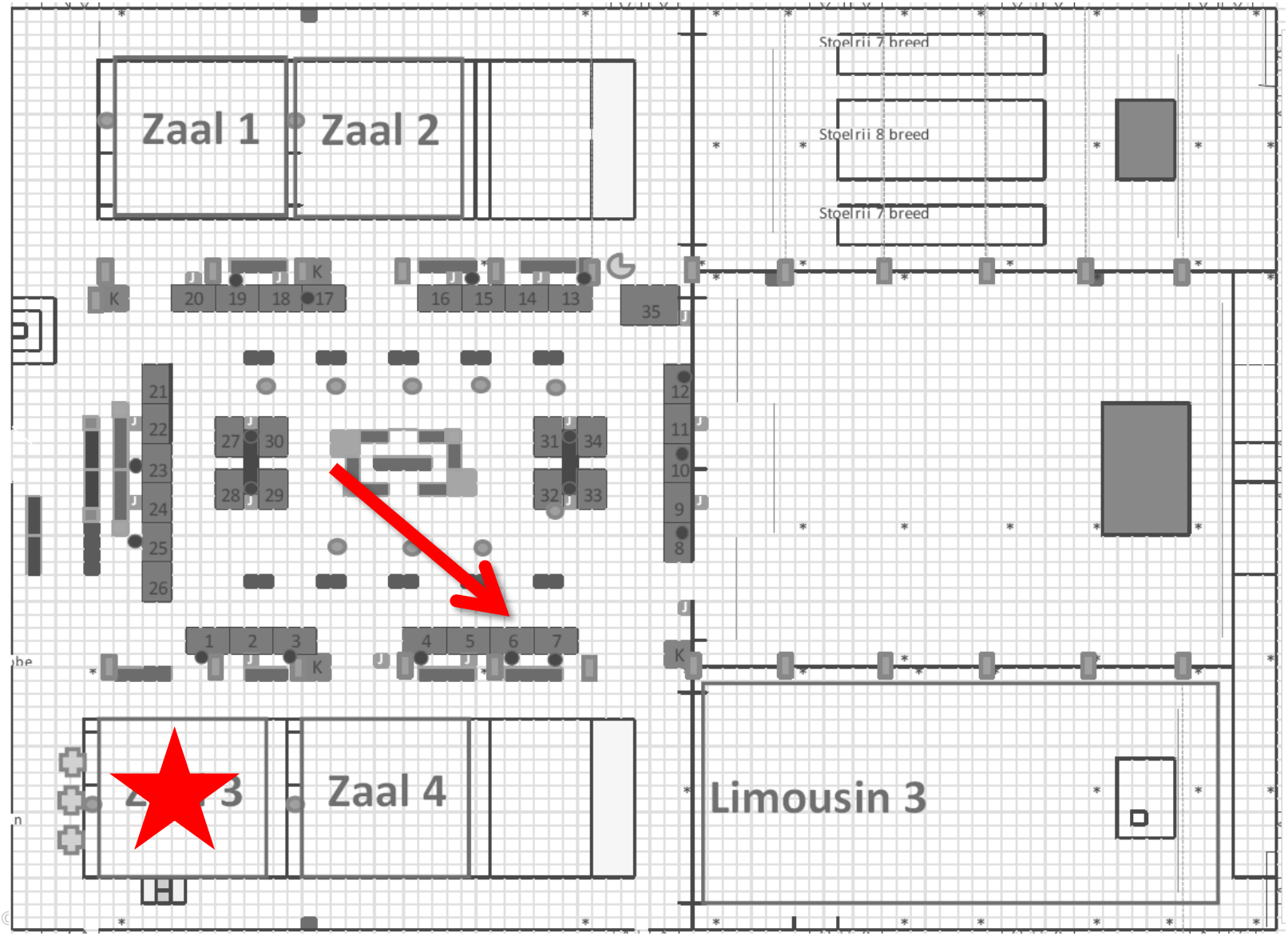
For more information visit at booth 4



For more information visit at booth 6



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For more information:

Visit us at booth 4

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Cadence Power Integrity tools

- Cadence PowerDC (DC Analyse, Thermal aware)
  - Pre- and postlayout
  - Setup Layout Constraints
- Cadence Power SI (AC Analysis)
  - Impedance analysis
  - Location and type of capacitors
- Cadence Optimize PI
  - Automatic decap optimization
  - Tradeof between performance, cost