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Implementing Physics of Failure into the Design Process

Craig Hillman
CEO
chillman@dfrsolutions.com

D&E Event
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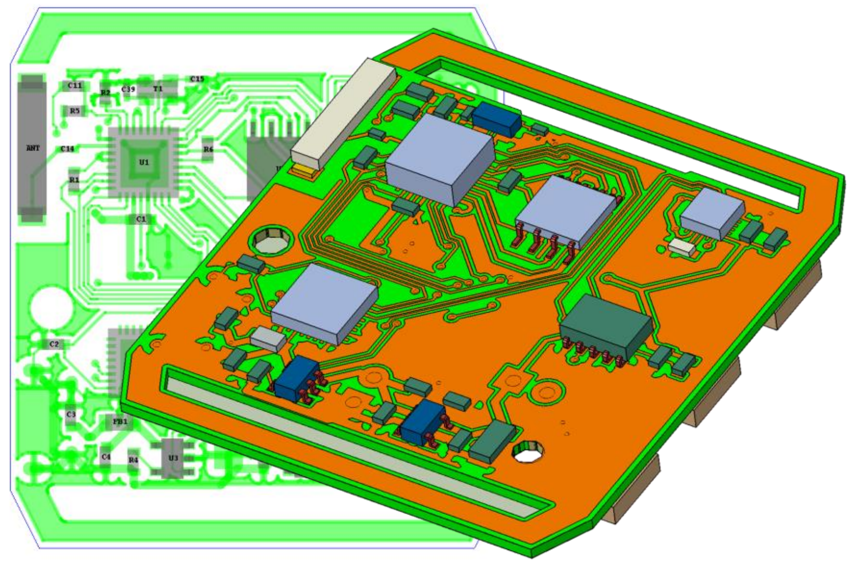
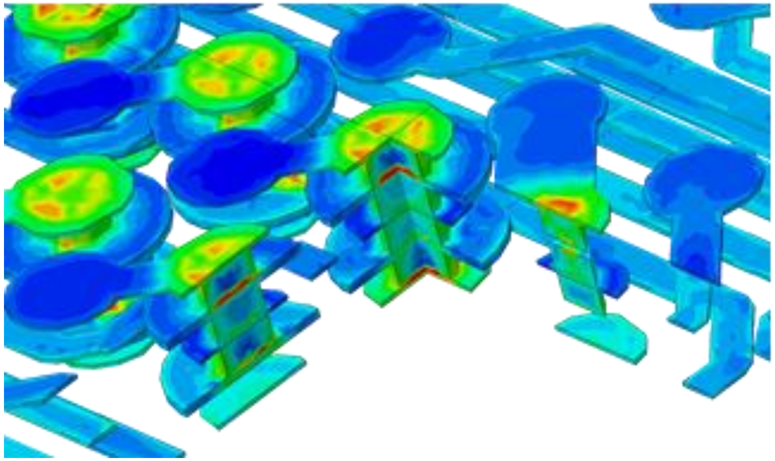
WHAT IS PHYSICS OF FAILURE (PoF)?

- Also known as reliability physics

- Common Definition:
  - The process of using modeling and simulation based on the fundamentals of physical science (physics, chemistry, material science, mechanics, etc.) to predict reliability and prevent failures

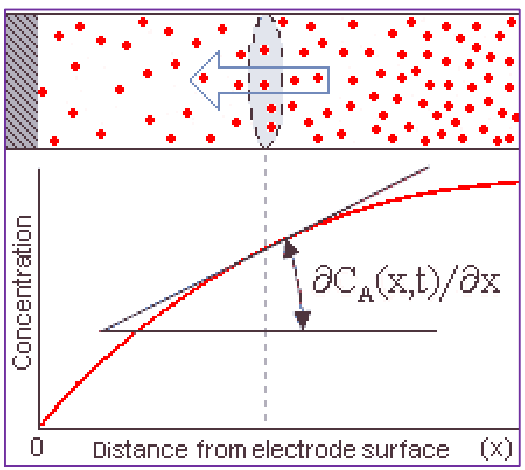




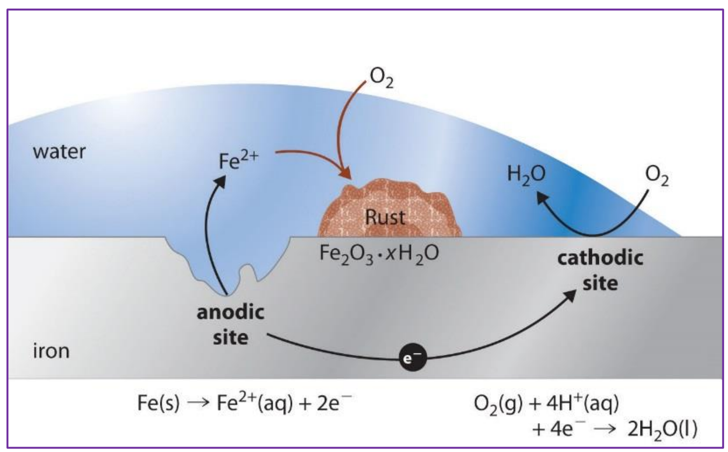
- What are we modeling / simulating?

- Reliability (t > 0) = Material Change / Movement

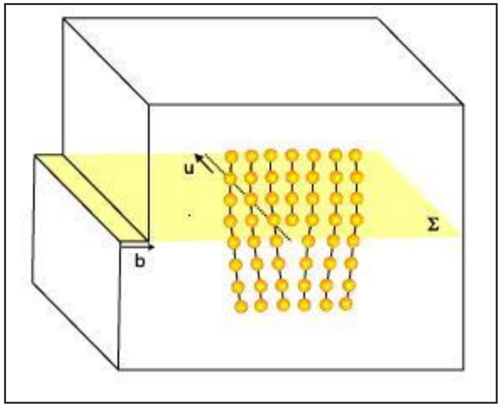
Diffusion



Corrosion



Plasticity



MATERIAL MOVEMENT AND PHYSICS OF FAILURE

- How large is the stress?
- At what rate is this stress driving material movement?
- At what time will this material movement induce failure?

PHYSICS OF FAILURE (POF) ALGORITHMS

$$\tau_{HCI} \propto \exp[\frac{b_{HCI}}{V_D}] \cdot \exp[\frac{E_{aHCI}}{kT}]$$

$$L = L_r \left(\frac{V_r}{V_0}\right) \times 2^{\left(\frac{T_r - T_A}{10}\right)}$$

$$T_f \propto \exp\left(\frac{\sim 0.51eV}{kT}\right) \times \exp(\sim -0.063\% RH)$$

$$\tau_{TDDB} \propto \exp[-b_{TDDB} \cdot V_G] \cdot \exp[\frac{E_{aTDDB}}{kT}]$$

$$N_f^{-0.6} D_f^{0.75} + 0.9 \frac{S_u}{E} \left[\frac{\exp(D_f)}{0.36}\right]^{0.1785 \log \frac{10^5}{N_f}} - \Delta\varepsilon = 0$$

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp \frac{E_a}{K_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

$$\tau_{EM} \propto (J)^{-n} \cdot \exp[\frac{E_{aEM}}{kT}]$$

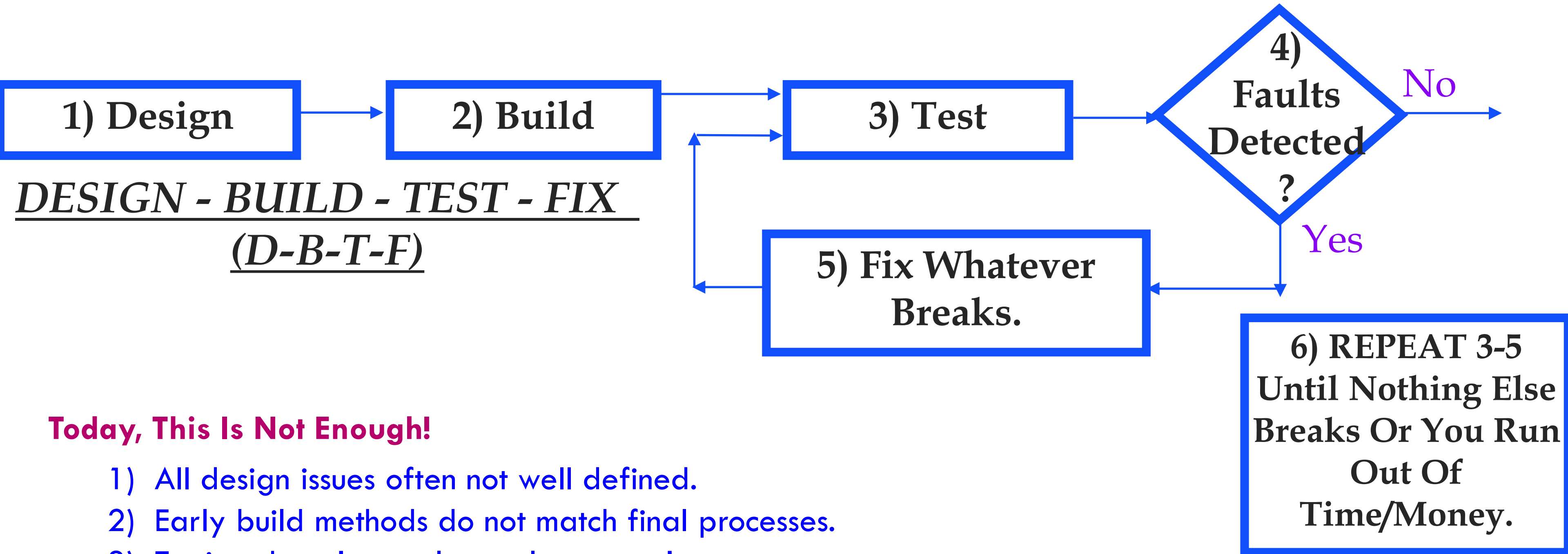
$$\tau_{NBTI} \propto \exp[-b_{NBTI} \cdot V_G] \cdot \exp[\frac{E_{aNBTI}}{kT}]$$

$$(\alpha_2 - \alpha_1) \cdot \Delta T \cdot L = F \cdot \left(\frac{L}{E_1 A_1} + \frac{L}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left(\frac{2 - \nu}{9 \cdot G_b a}\right)\right)$$

Can be mind-numbing! What to do?

WHY PoF?

Before Physics of Failure: Traditional Reliability Growth



<u>DESIGN - BUILD - TEST - FIX</u>
<u>(D-B-T-F)</u>

Today, This Is Not Enough!

1) All design issues often not well defined.
2) Early build methods do not match final processes.
3) Testing doesn't equal actual customer's usage.
4) Improving fault detection catches more problems, but causes more rework.
5) Problems found too late for effective corrective action, fixes often used.
6) **<u>Testing more parts & more/longer tests "seen as only way" to increase reliability</u>.**
7) Can not afford the time or money to test to high reliability.
8) Incremental improvements from faster more, capable tests still not enough.

It Is Time for a Change

WHY PHYSICS OF FAILURE: SAVE LOTS OF MONEY

Global Storage Manufacturer reduces time-to-market by six (6) months

- Global Storage Manufacturer is using PoF software (Sherlock) to eliminate one (1) to two (2) physical tests for EACH PCBA Design

- Ten (10) PCBAs are designed annually
  - Engineering labor and hard test costs (Chambers, Samples) are approximately $750,000 per test
  - Results in an **Annual Savings of $7,500,000**

- Sherlock also eliminates two (2) design revs for EACH PCBA
  - Time-to-Market **Reduced by Six (6) Months**

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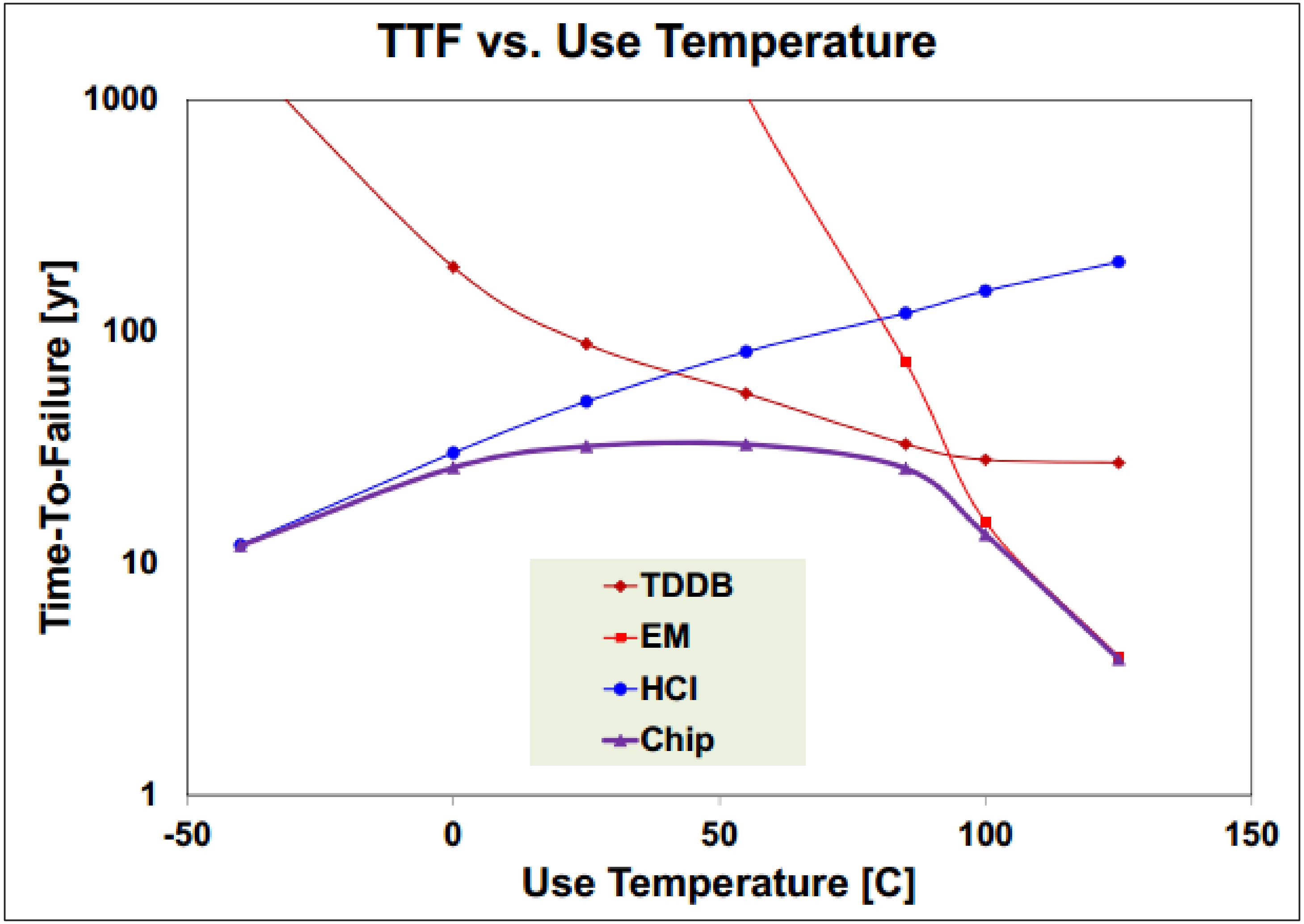
WHY PHYSICS OF FAILURE: LESS ROBUST TECHNOLOGY



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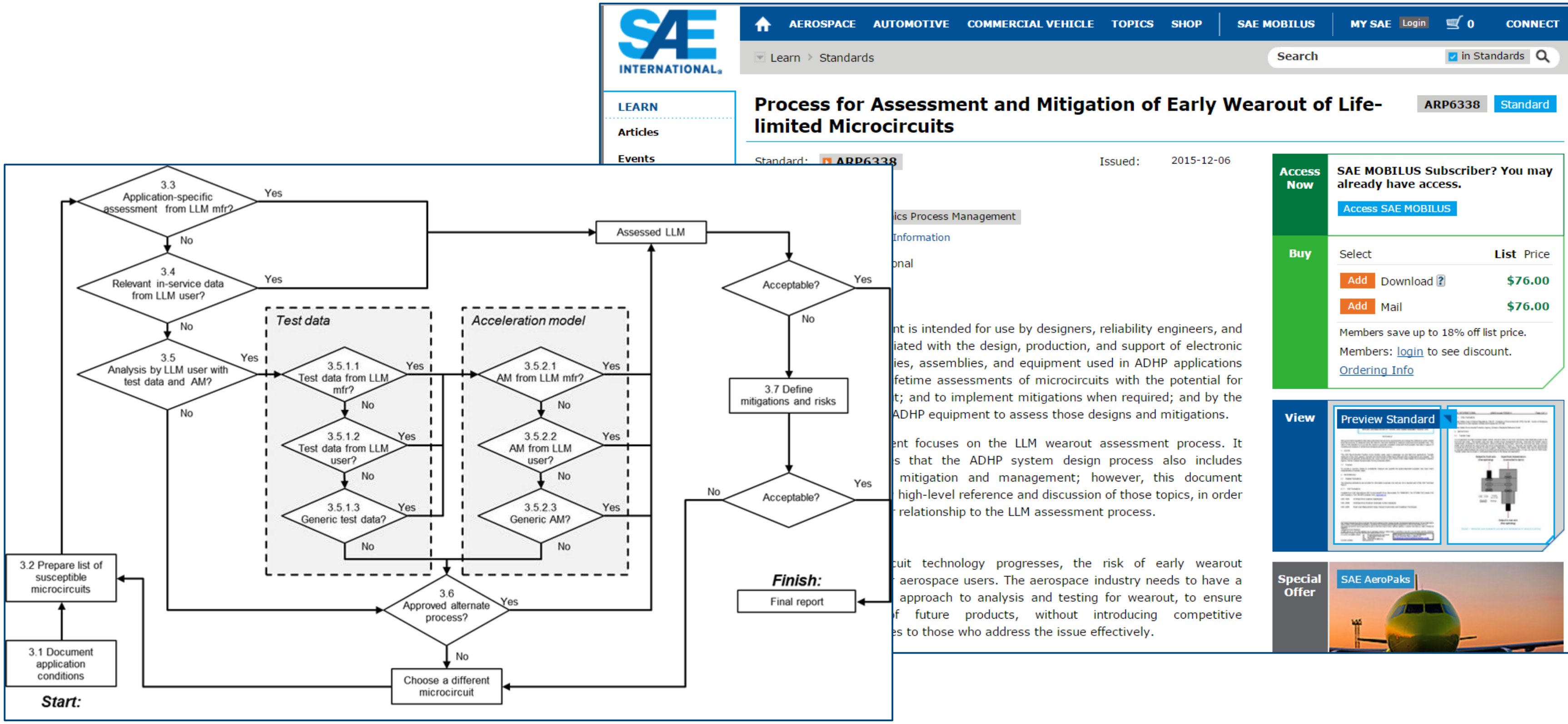
WHY PHYSICS OF FAILURE: IT IS REQUIRED



- Numerous aviation and automotive system integrators (OEMs) are implementing PoF requirements for their Tier 1 suppliers

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WHEN PoF?

WHEN PoF: PART OF A ROBUST DFR PROCESS

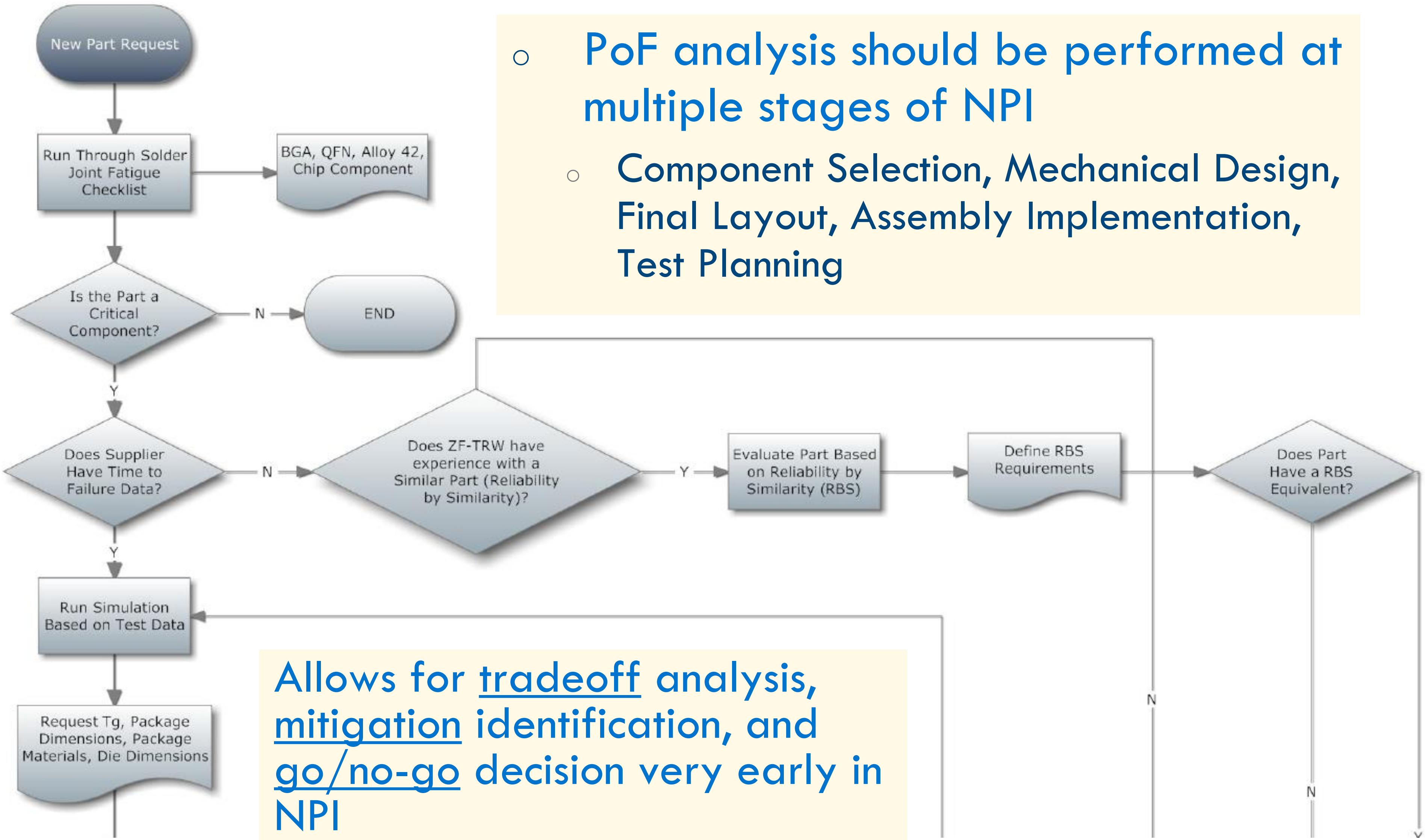
- Failure Mode Analysis
  - Failure Mode Effect Analysis (FMEA), Fault Tree/Tolerance Analysis (FTA), Design Review by Failure Mode (DRBFM), Sneak Circuit Analysis (SCA)
- Reliability Prediction - Empirical
- Design Rules
- Design for Excellence
  - Design for Manufacturability (DfM), Design for Testability (DfT)
- Tolerancing (Mechanical, Electrical)
- Simulation and Modeling (Stress)
  - Thermal, Mechanical, Electrical/Circuit
- Simulation and Modeling (Damage)
  - EMI/EMC, EOS/ESD, Physics of Failure, Derating

WHEN PoF: CRITICAL COMPONENTS

- Integrated Circuits (EM, TDDB, HCI, NBTI)
- Interconnects (Die Attach, Wire Bonds, Solder Joints, Vias)
- Ceramic Capacitors (oxygen vacancy migration)
- Electrolytic Capacitors (electrolyte evaporation, dielectric dissolution)
- Film Capacitors
- Memory Devices (limited write cycles, read times)
- Light Emitting Diodes (LEDs) and Laser Diodes
- Resistors (if improperly derated)
- Silver-Based Platings (if exposed to corrosive environments)
- Relays and other Electromechanical Components
- Connectors (if improperly specified and designed)
- Tin Whiskers

WHEN PoF: PROCESS

- PoF analysis should be performed at multiple stages of NPI
  - Component Selection, Mechanical Design, Final Layout, Assembly Implementation, Test Planning



Allows for tradeoff analysis, mitigation identification, and go/no-go decision very early in NPI

PoF EXAMPLE:
SOLDER FATIGUE

STRAIN RANGE + CLOSED FORM EQUATIONS

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon_f}\right)^c$$

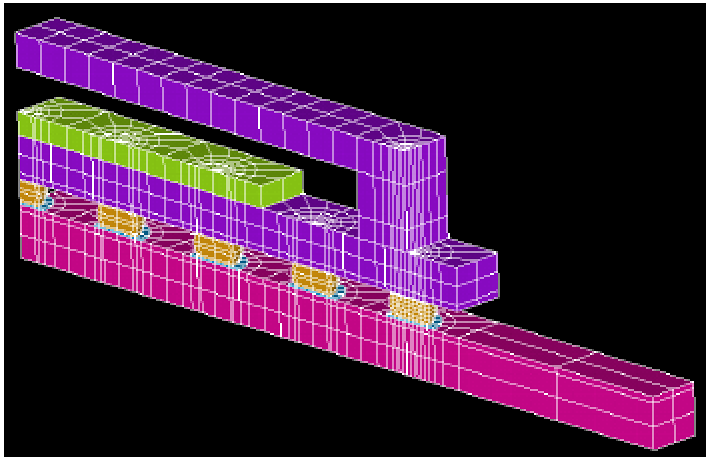
$$\Delta\gamma = C\frac{L_D}{h_s}\Delta\alpha\Delta T$$

$$\varepsilon_f = 0.325$$

$$c = (-0.442) - (6x10^{-4}T_s) + (1.74x10^{-4})[\ln(1 + f)]$$

Engelmaier, W.; , "Fatigue Life of Leadless Chip Carrier Solder Joints During Power Cycling," Components, Hybrids, and Manufacturing Technology, IEEE Transactions on , vol.6, no.3, pp. 232-237, Sep 1983

STRAIN ENERGY + FINITE ELEMENT ANALYSIS (FEA)



Strain energy (work) used to predict crack initiation and crack propagation

$$N_0 = K1\left(\Delta W_{avg}\right)^{K2}$$

$$\frac{da}{dN} = K3\left(\Delta W_{avg}\right)^{K4}$$

$$N_f = N_0 + \frac{D}{da/dN}$$

Darveaux, R., "Solder Joint Fatigue Life Model," Proceedings of TMS Annual Meeting, Orlando FL, February 1997, pp. 213-218

STRAIN ENERGY + CLOSED FORM EQUATIONS

$$(\alpha_2 - \alpha_1) \cdot \Delta T \cdot L = F \cdot \left(\frac{L}{E_1 A_1} + \frac{L}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left(\frac{2 - \nu}{9 \cdot G_b a} \right) \right)$$

$$\Delta W = 0.5 \cdot \Delta \gamma \cdot \frac{F}{A_s}$$

$$N_f = (0.001 \cdot \Delta W)^{-1}$$

Closed Form, PCB Stiffness, Strain Energy, E (T), Tg, Die Shadow

N. Blattau and C. Hillman, "An Engelmaier Model for Leadless Ceramic Chip Devices with Pb-Free Solder," Journal of the Reliability Information Analysis Center, First Quarter 2007, 6-11

UNEXPECTED SOLDER FAILURES

Increasing number of companies reporting early life failures during thermal cycle testing or in the field

Classic solder fatigue approaches do not seem to be capturing these risks

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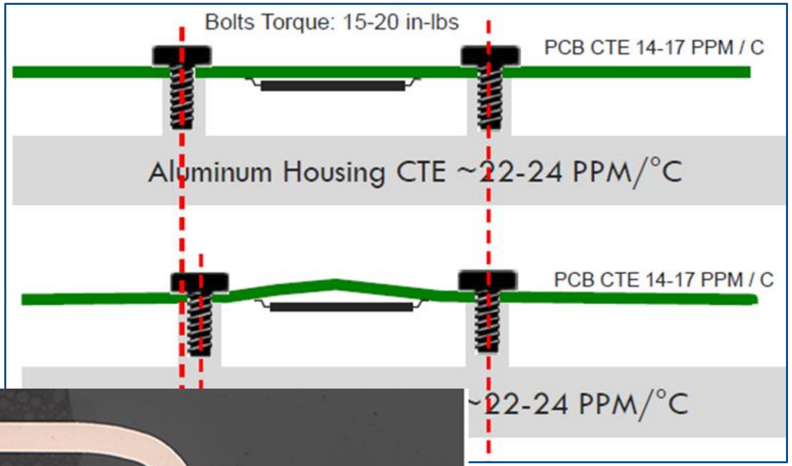
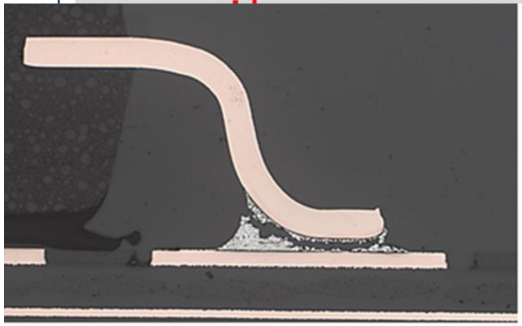
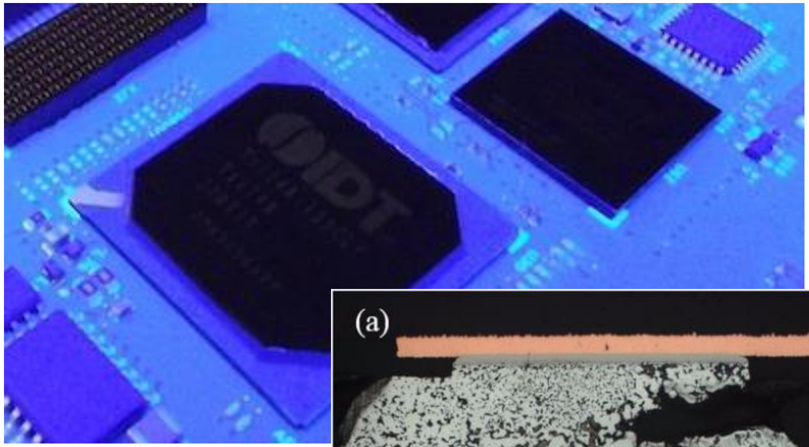
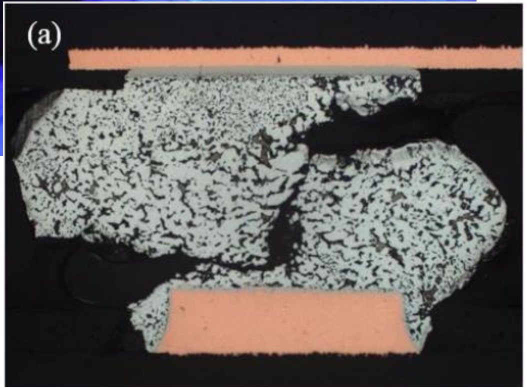
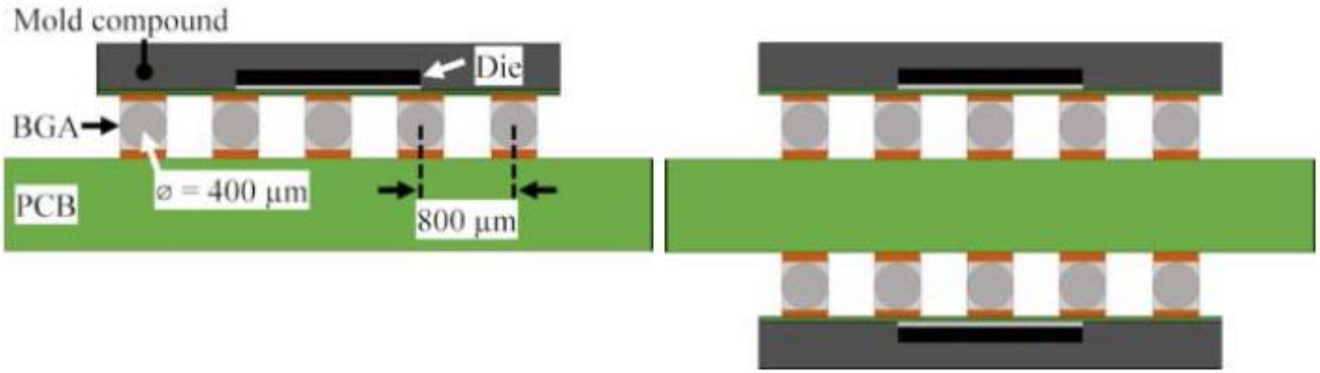
SYSTEM-LEVEL EFFECTS / MIXED-MODE / TRIAXIALITY











VECTORIZED ENERGY PARTITIONING (VEP)

$$\frac{1}{N_f} = \left(\frac{1}{N_f}\right)_{Tensile} + \left(\frac{1}{N_f}\right)_{Compressive} + \left(\frac{1}{N_f}\right)_{Shear}$$

$$(N_f)_{Axial,plastic} \Rightarrow \frac{\Delta\varepsilon}{2} = \varepsilon'_f (2N_f)^{C_1} \qquad (N_f)_{Axial,Creep} \Rightarrow N_f = \frac{1}{2}\left[\frac{\Delta\varepsilon}{\varepsilon_f}\right]^{-1/C_3}$$

$$(N_f)_{shear,plastic} \Rightarrow \frac{\Delta\gamma}{2} = \gamma'_f (2N_f)^{C_2} \qquad (N_f)_{shear,Creep} \Rightarrow N_f = \frac{1}{2}\left[\frac{\Delta\gamma}{\gamma_f}\right]^{-1/C_4}$$

$\varepsilon'_f \ \gamma'_f \ C_1 \ C_2$ $\qquad$ $\varepsilon_f \ \gamma_f \ C_3 \ C_4$

VEP approach will combine FEA and closed form equation to optimize diligence and simulation time

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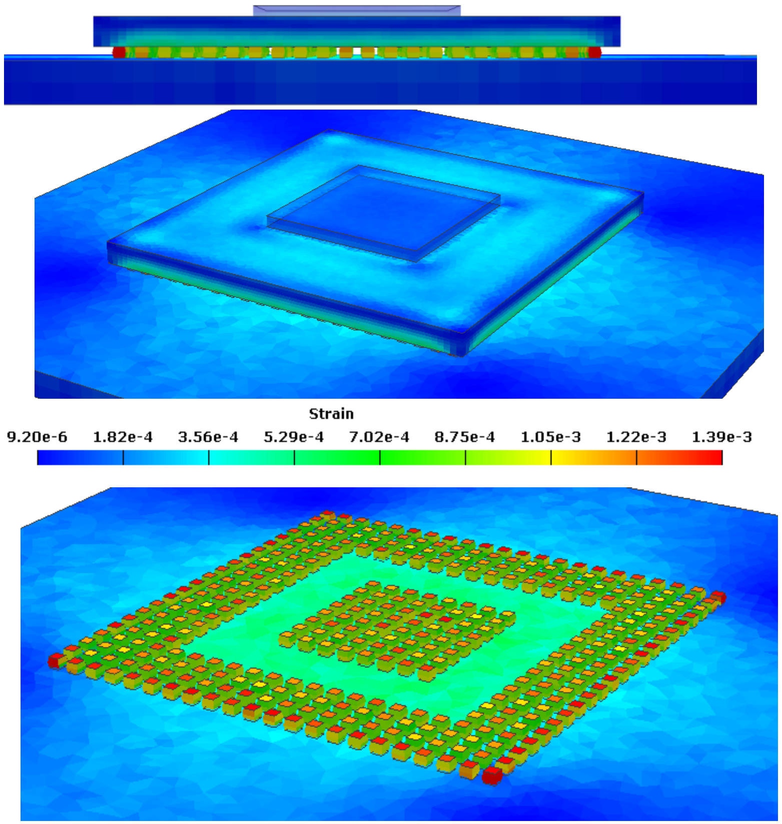
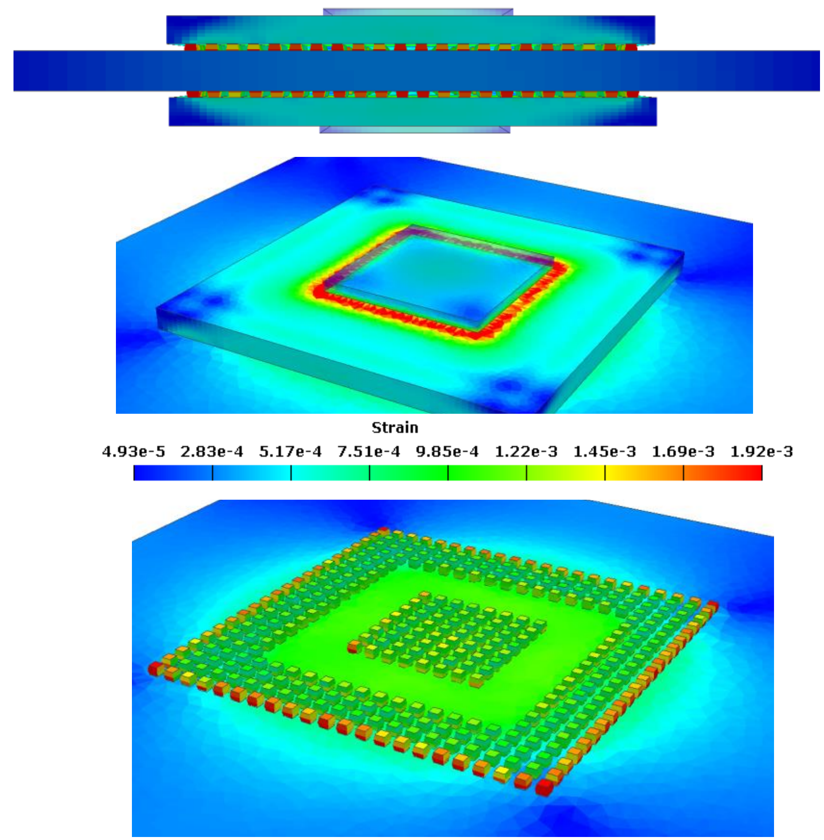
VEP AND FLIP CHIP CSP (FC-CSP) – SHERLOCK

- First and second level interconnect strains in single sided and mirrored configurations.

Single Sided



Mirrored



PoF EXAMPLE:
INTEGRATED CIRCUITS

FUNDAMENTAL CHALLENGES

- What integrated circuit (IC) manufacturers are using

$$\vec{J}_v = -D_v\left(\nabla C_v - \frac{|Z^*|e}{kT} C_v \vec{E} - \frac{Q^*}{kT^2} C_v \nabla T + \frac{f\Omega}{kT} C_v \nabla \sigma\right)$$

- What they want you to use

$$\lambda \propto \frac{1}{TDH} \times exp\left(\frac{0.7eV}{k}\left[\frac{1}{T_{field}} - \frac{1}{398}\right]\right)$$

- What you should be using

$$t_f = -\frac{Test\ Time}{\left(\frac{\ln(1-CL)}{n}\right)^{1/\beta}} \times A(J^{-n})exp\left(\frac{E_a}{kT}\right)\ [\beta > 1]$$

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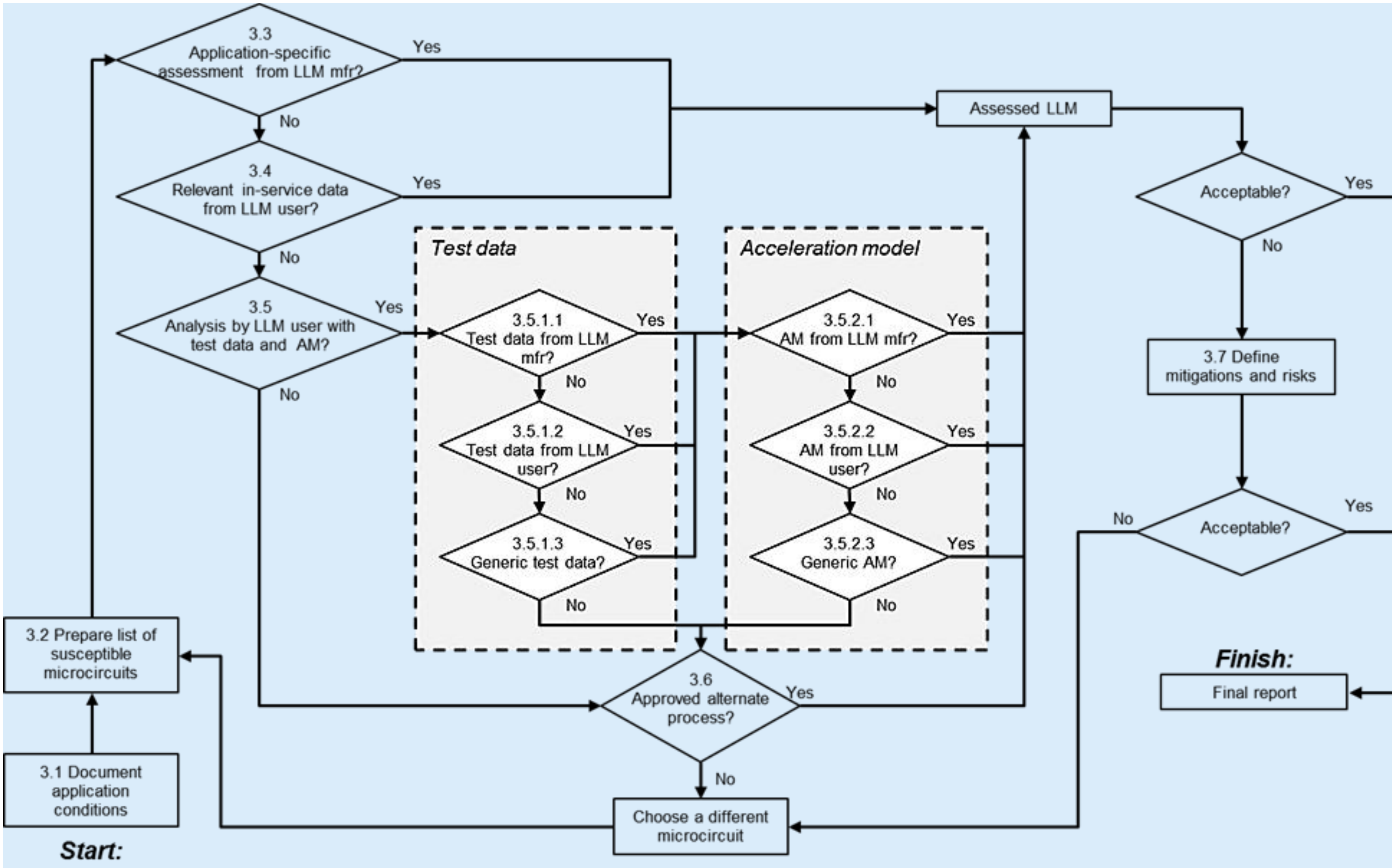
OPTIONS 4 AND 5 (PARAMETERS NODE-DEPENDENT)

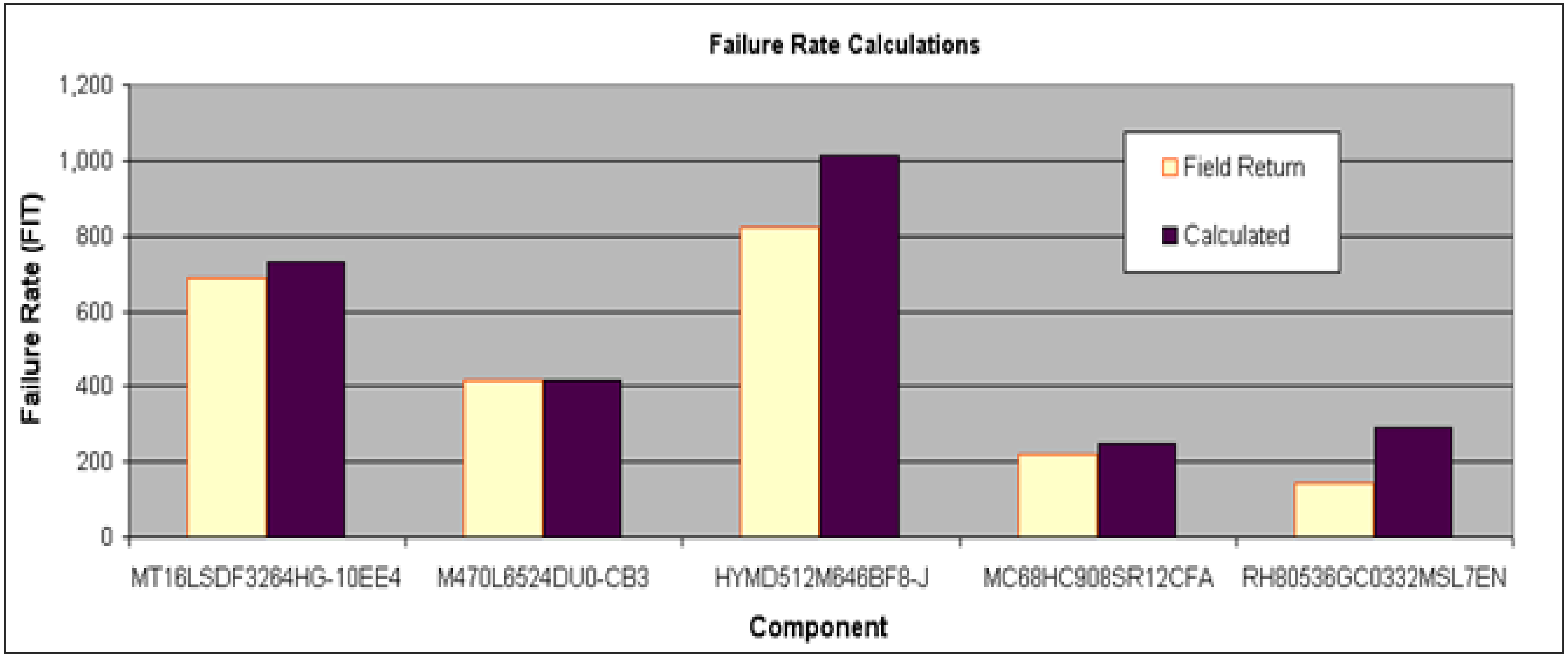
	10nm Planar	14nm FinFET	16nm FinFET	20nm Planar	22nm FinFET	28nm Planar	35nm Planar	45nm Planar	65nm Planar	90nm Planar	130nm Planar	180nm Planar	250nm Planar	350nm Planar
Name	10nm	14nm	16nm	20nm	22nm	28nm	35nm	45nm	65nm	90nm	130nm	180nm	250nm	350nm
Type	Planar	FinFET	FinFET	Planar	FinFET	Planar	Planar	Planar	Planar	Planar	Planar	Planar	Planar	Planar
gateOxideThickness	3.10E-10	7.70E-10	8.00E-10	9.40E-10	8.20E-10	6.60E-10	9.50E-10	9.50E-10	1.10E-09	2E-09	2.30E-09	4.00E-09	5.00E-09	7.50E-09
channelRegionLength	9.00E-09	1.70E-08	2.00E-08	1.70E-08	2.00E-08	2.00E-08	2.20E-08	2.70E-08	2.50E-08	1.00E-07	1.30E-07	1.80E-07	2.50E-07	3.50E-07
channelRegionWidth	1.35E-07	2.55E-07	3.00E-07	2.55E-07	3.00E-07	3.00E-07	1.62E-07	1.62E-07	1.50E-07	1.50E-06	1.95E-06	2.70E-06	3.75E-06	5.25E-06
transconductance	8.63E-04	8.63E-04	8.63E-04	8.63E-04	8.63E-04	8.63E-04	8.63E-04	8.63E-04	3.21E-04	4.83E-04	4.80E-04	3.36E-04	3.24E-04	3.00E-04
nominalSupplyVoltage	0.8	0.85	0.86	0.8	0.9	0.8	0.8	0.8	1.1	1	1.2	1.8	2.5	3.3
nominalDriveCurrent	0.002	0.001355	0.001348	0.00159	0.00136	0.00148	0.0012	0.0012	0.0009	0.0009	0.0009	0.00062	0.0006	0.00056
nominalCoreVoltage	0.83	0.85	0.86	0.8	0.9	0.8	0.8	0.8	1.1	1	1.2	1.8	2.5	3.3
ThresholdVoltage	0.274	0.392	0.404	0.304	0.441	0.322	0.185	0.119	0.134	0.702	0.7	0.704	0.703	0.701
activationEnergyTDDB	0.7	0.3	0.3	0.7	0.3	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
activationEnergyNBTI	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6
activationEnergyHCI	-0.15	0.3	0.3	-0.15	0.3	-0.15	-0.15	-0.15	-0.15	-0.15	-0.15	-0.15	-0.15	-0.15
activationEnergyEM	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.75	0.7	0.65
TDDBgamma	0.9	3.8	3.8	0.9	3.8	0.9	0.9	0.9	0.9	1	1	1.1	1.2	1
NBTIgamma	6	6	6	6	6	6	6	6	6	6	6	6	6	6
HCIgamma	42	17	17	42	17	42	42	42	42	42	45	50	55	60
Emgamma	2	2	2	2	2	2	2	2	2	2	2	2	2	2
weibullBetaTDDB	1	1.5	1.5	1	1.5	1	1	1	1	1.3	1.5	2.8	3	4
weibullBetaNBTI	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.5	2	3	4
weibullBetaHCI	1.2	4	4	1.2	4	1.2	1.2	1.2	1.2	1.2	1.5	2	3	4
weibullBetaEM	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Scaling Factor	0.2401	0.49	0.7	0.343	1	0.49	0.7	1	1	1	1	1	1	1

SAE ARP 6338 LIFE LIMITED MICROCIRCUITS



MULTI-MECHANISM THEORY: VALIDATION STUDY (cont.)

- Results demonstrate the accuracy and repeatability of the multi-mechanism model to predict the field performance of complex integrated circuits



CONCLUSION

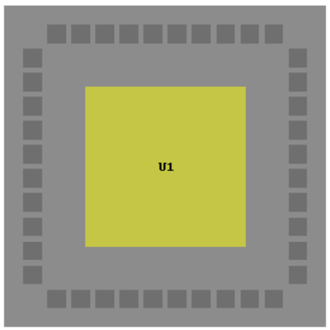
- Physics of Failure is part of a larger trend towards modeling and simulation
  - Testing is too late, takes too long
  - Design rules are too conservative, not pliable to new technology

- Several new organizations and tools are coming online to help companies incorporate PoF-based analysis into the design process

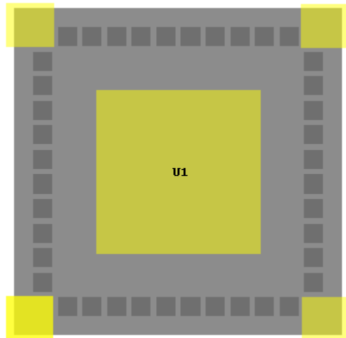
STAGE 1: EFFECT OF CORNER STAKING

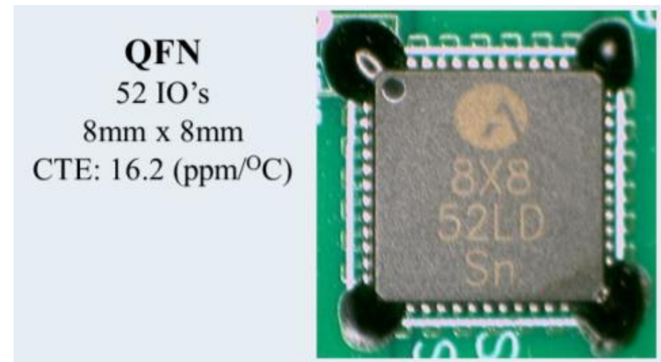
Sherlock predicts effect of staking on lead strain in QFN packages. Experimental data shows almost 40% improvements in fatigue life.

No Staking

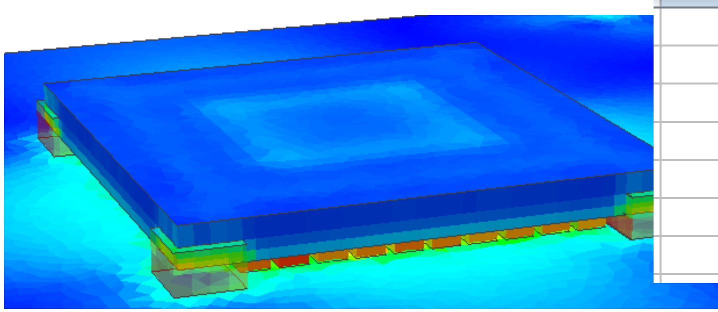


Staking – Namics UF



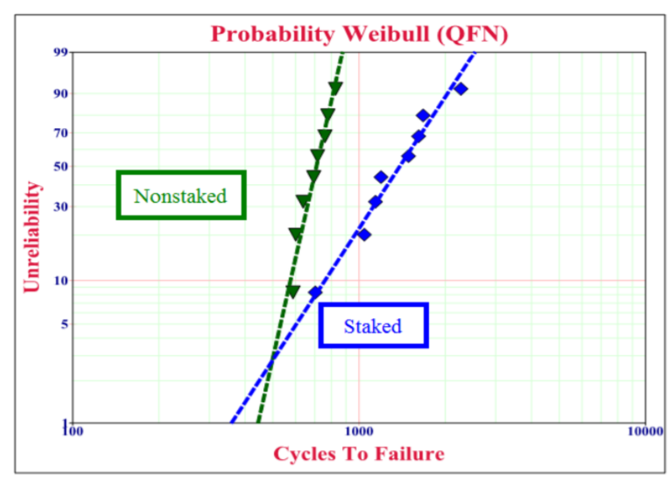


- Reduction in maximum lead strain



Max Lead Strain
2.2E-3
2.1E-3
2.1E-3
2.1E-3
2.1E-3
2.1E-3
2.0E-3

Max Lead Strain
2.7E-3
2.6E-3
2.6E-3
2.6E-3
2.6E-3
2.5E-3
2.5E-3



PoF and Electrolytic Capacitors

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ELECTROLYTIC CAPACITORS (cont.)

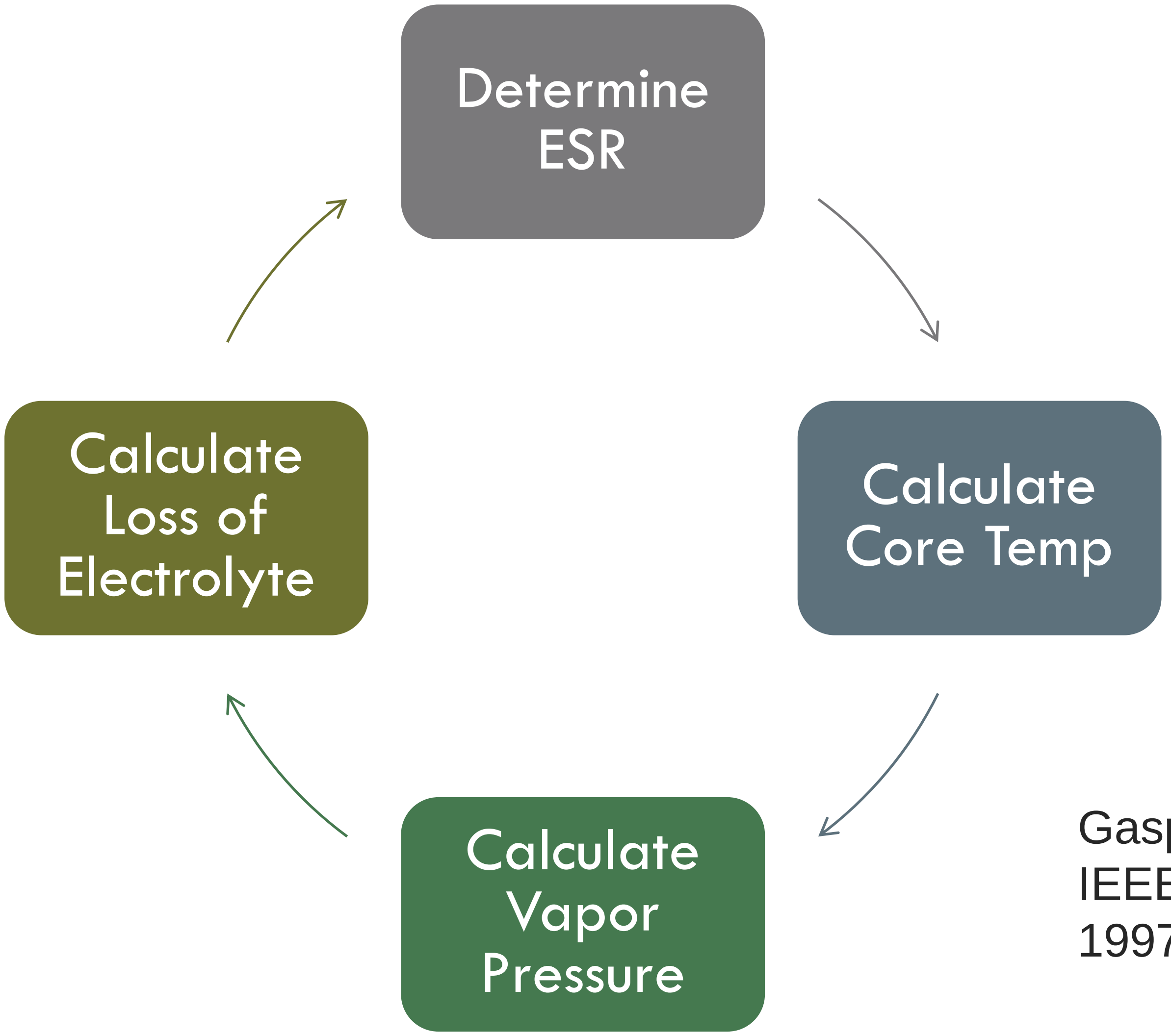
- Evaporation prediction has been based on a widely held standard aging relationship

- Doubling of lifetime with every 10C drop in temp (note: This is not Arrhenius!)

$$L_x = L_o \times 2^{(To-Tx)/10}$$

- However, there are variations from manufacturer to manufacturer

PHYSICS OF FAILURE FOR ELECTROLYTIC CAPACITORS

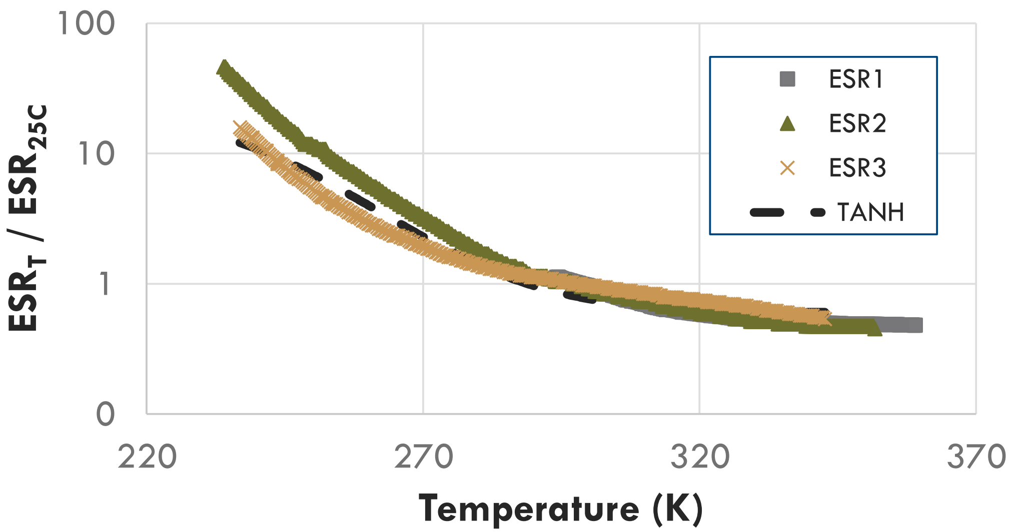


Gasperi
IEEE IAS
1997

PHYSICS OF FAILURE FOR ELECTROLYTIC CAPACITORS

- Increase in ESR is the most common driver for failures

- Determine ESR at test/application temperature
  - Typically $ESR_T/ESR_{25C} = A \times (B - (C \times TANH((T-T_0)/D)))$
  - Empirically determined by DfR
    - A = 6
    - B = 1.8
    - C = 1.7
    - $T_0 = 240$
    - D = 25



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POF FOR ELECTROLYTIC CAPACITORS

- Calculate Core Temperature
  - $\Delta T = \frac{ESR_T \times I^2}{H \times (2\pi rh + 2\pi r^2)}$ (H is heat transfer per surface area)
  - Add to ambient temperature to determine core temperature

- Calculate Vapor Pressure $[\log P = A - \frac{B}{C + T}]$ (Antoine Equation, mmHg)
  - Ethylene Gylcol (EG) / 99%H2O:
    A = 9.19 / B = 3103 / C = 309.7
  - Dimethyl Formamide (DMF) and γ-Butyrolactone (GBL)

PHYSICS OF FAILURE FOR ELECTROLYTIC CAPACITORS

- ## Calculate Loss of Electrolyte
  - $V_{t0+\Delta t} = V_{t0} - (k \times P \times \Delta t)$
  - k is leak rate based on vapor pressure (empirically determined, ml/mmHg/hr)
  - Δt is the time step

- ## ESR is dependent on electrolyte volume
  - $ESR_{t0+\Delta t}/ESR_{t0} = (V_{t0+\Delta t}/V_{t0})^2$

9000 Virginia Manor Rd Ste 290, Beltsville MD 20705 | 301-474-0607 | www.dfrsolutions.com