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JTAG TECHNOLOGIES

Subjects

- JTAG Technologies (Rik Doorneweert, Area Manager)
  - JTAG Technologies B.V. activities
  - Introduction to (classic) Boundary Scan

- Grass Valley Breda(Camera division) (Khaled Sarsam, Test Automation Architect)
  - About Grass Valley and it's products
  - **Embedded at-speed testing without the functional Firmware**
  - **Embedded testing examples using JTAG interface**

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JTAG TECHNOLOGIES®

JTAG Technologies B.V.

- Worldwide active since 1994, HQ in Eindhoven, 55 employees
- JTAG based tools for:
  - HW Engineers:

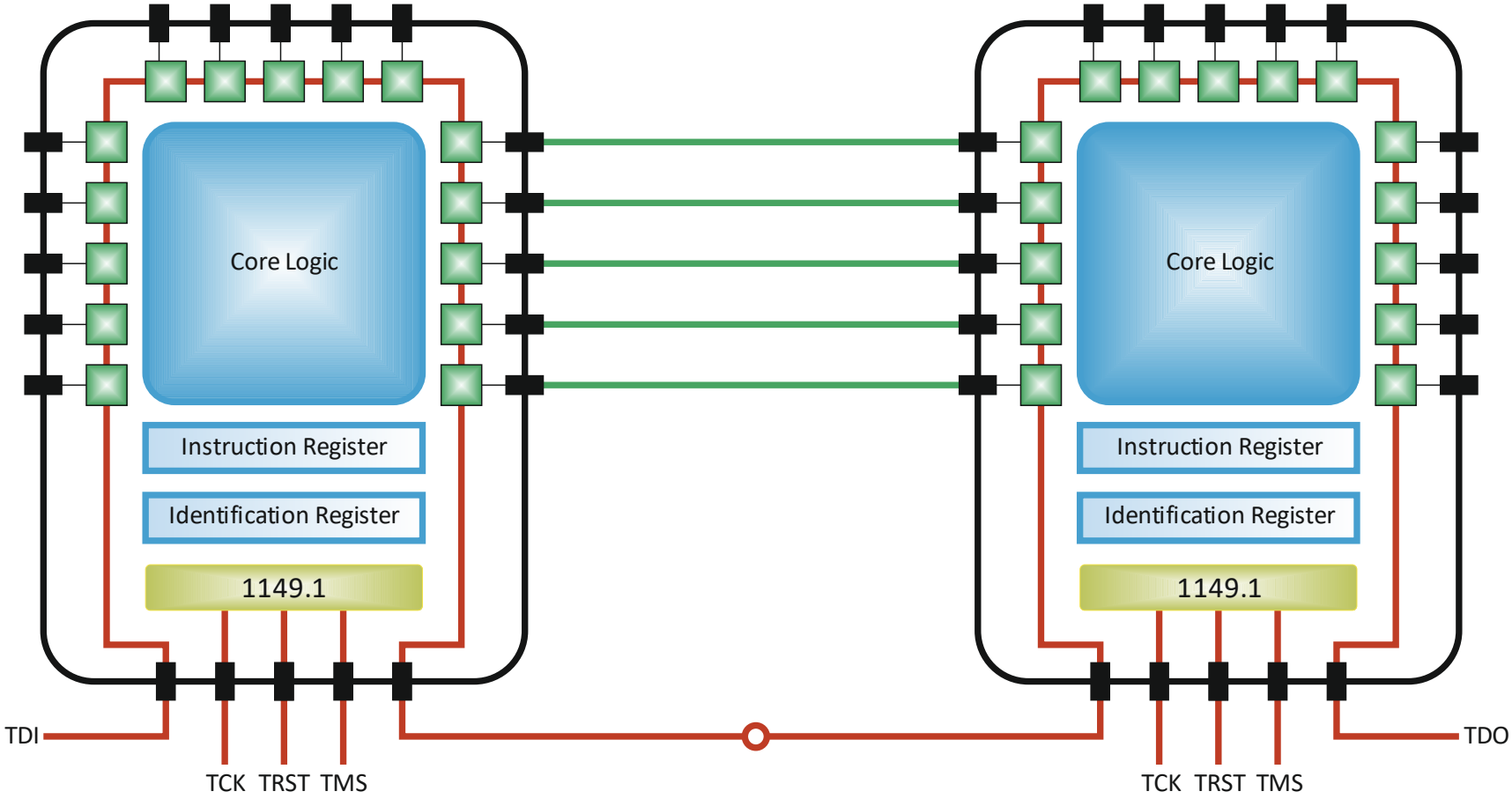
BSDL files → JTAG Live → Measure

Altium Designer JTAGmaps accesibilty

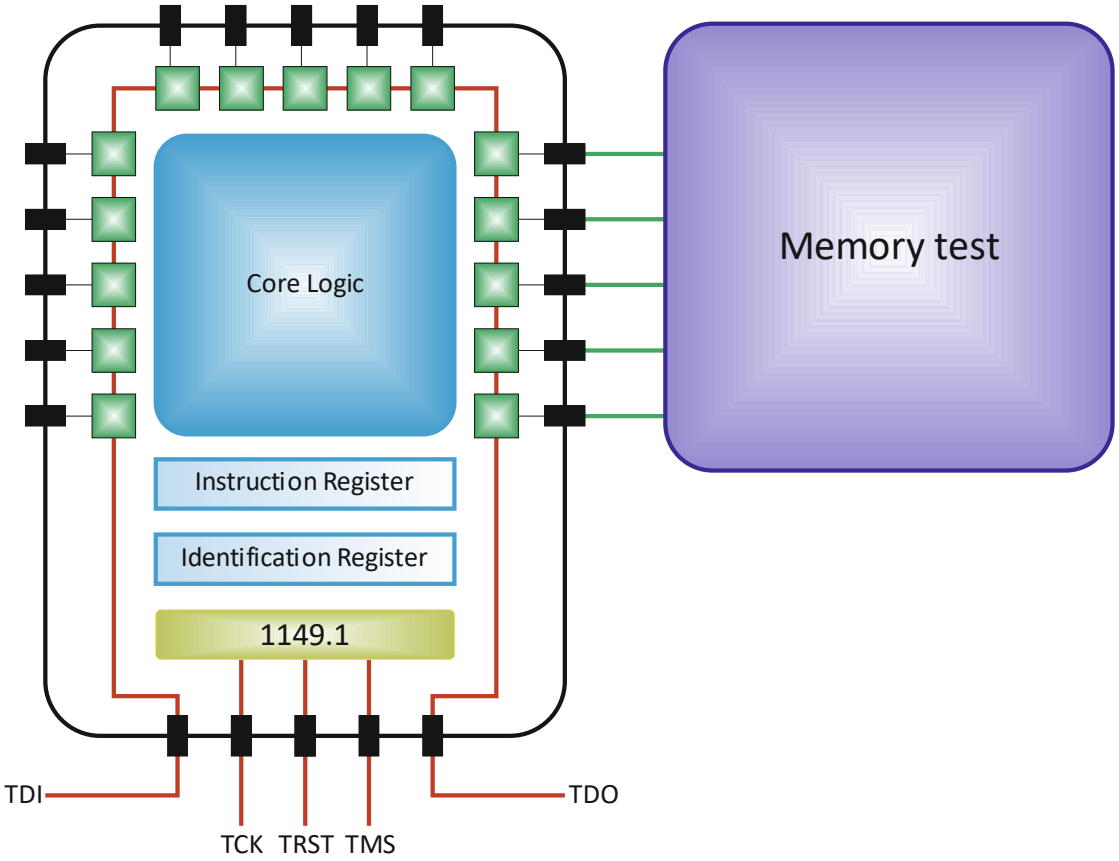
  - Test Engineers:

BSDL files →
Schematics →
BOM file →
ProVision → ISP & Test programs
JTAG TECHNOLOGIES → Testability reports

Extest Interconnection test



Extest Memory connection test



Requires access to:

- Address bus
- Data bus
- Control signals

Examples:

- SRAM
- DRAM
- SDRAM
- DDR2
- DDR3
- DDR4…

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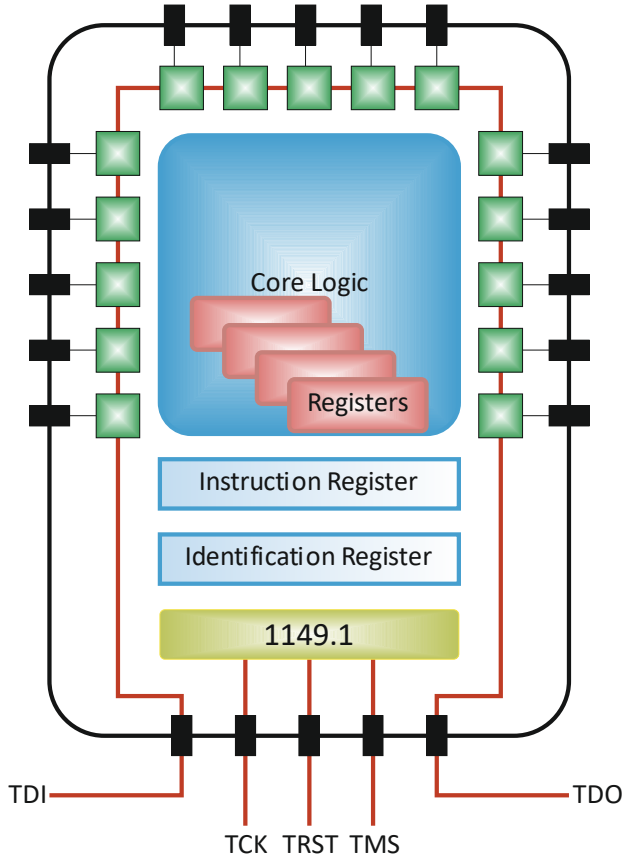
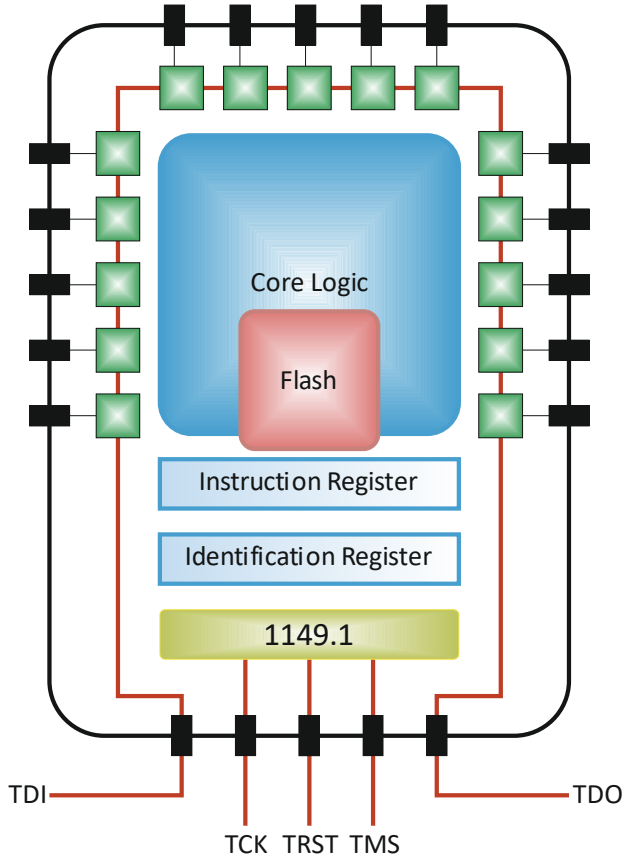
Intest



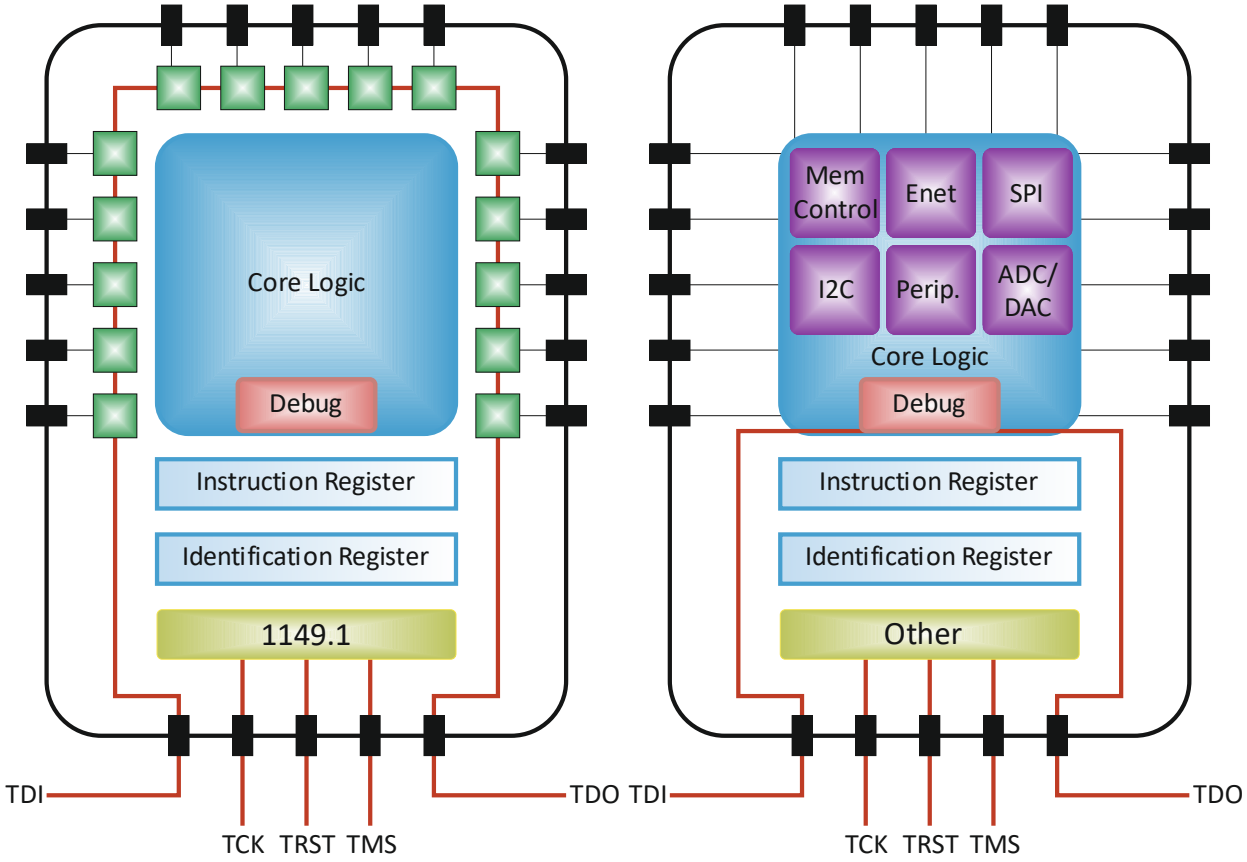
- BIST (Built In Self Test)
- Measure voltages (Zynq/XADC)
- Everything what is supported by the 1149.1 Device

Programming Embedded Flash



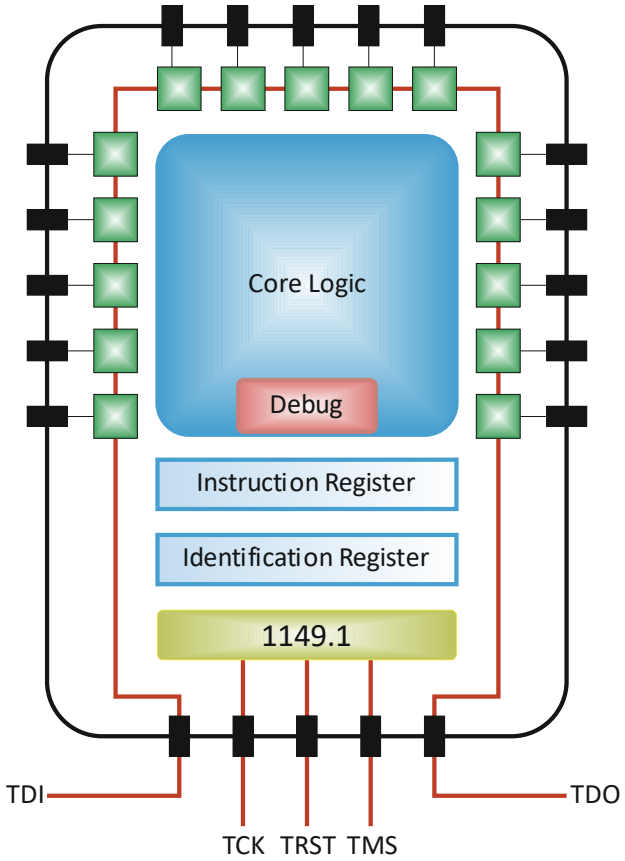
- Analog Devices
- Atmel
- Cypress
- Freescale
- Infineon
- Microchip
- Nordic
- NXP
- Philips
- Renesas
- ST
- Silicon Labs
- TI

Emulative accessible uC's



- ARM
- Analog Devices
- Freescale
- Infineon
- Microchip
- Texas Instruments
- Xscale
- NXP
- ST

Emulative accessible FPGA's



- Altera, JTAG Translator
- Xilinx, JTAG Translator

Grass Valley a Belden brand

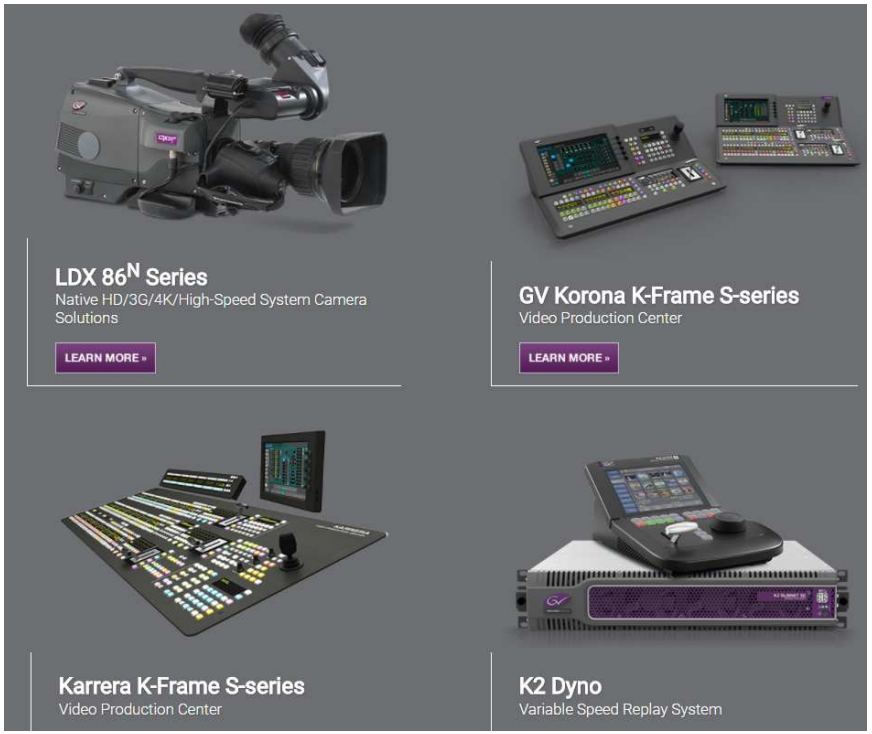
Number of employees:

- Grass Valley 1200+
- Belden 8500+ (GV Included)

Products:

Grass Valley

- Live Production Equipment



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Test Automation

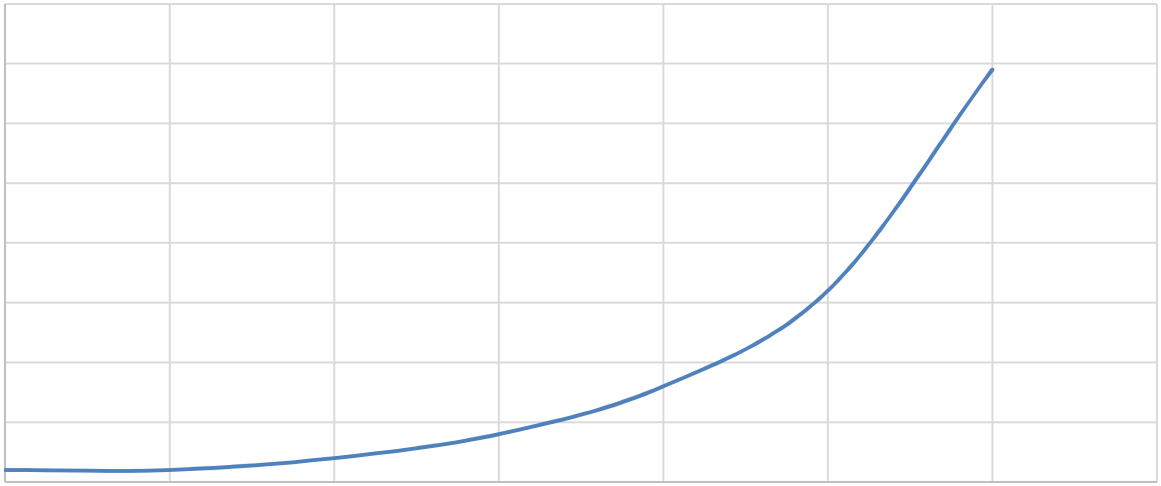
Various interfaces at our disposal

- JTAG
- I2C
- SPI
- etc

Why test @ speed

- Almost reflecting the functional stage
- Cover production faults which might only occur at functional speeds
- Find faults at an early stage of the process (both development - and production process)

Costs of resources at different test-phases in case fault is detected



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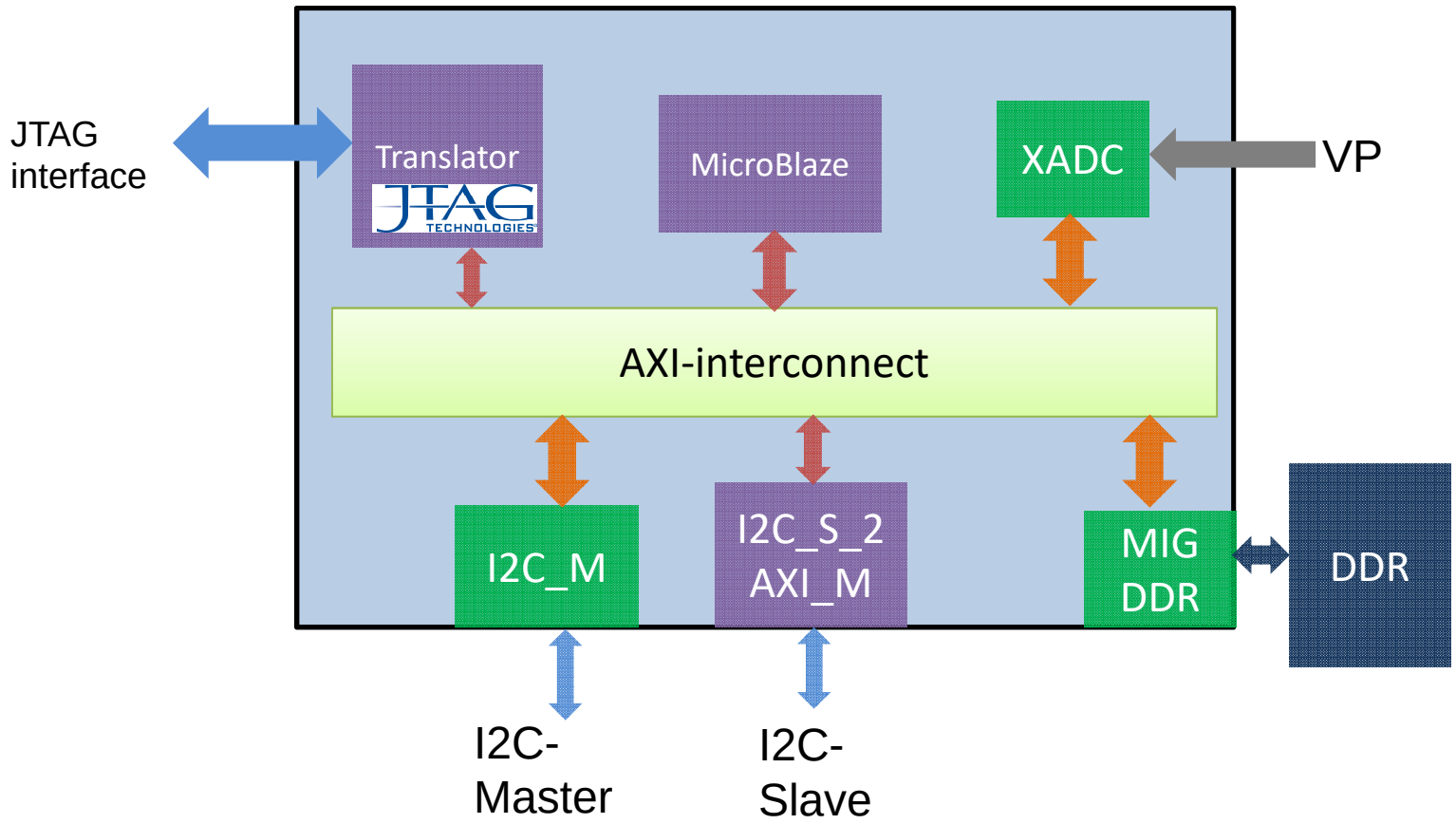
The JTAG interface @ Grass valley Breda

- Used for board-level testing part of our LabView based tests
- Automatic test-pattern generation using ATE tools
- Automatic flash-programming using bus-emulation
- Now also used for Embedded testing (At-speed)
- Test Automation using Python scripting

Example 1: FPGA based @Speed DDR3-interconnection test



Generation sequence

- AXI-interconnect based FPGA design with JTAG Translator as bus-master
- Compile & generate an SVF-file
- Generate At-speed test using CTPG_M (JTAG Technologies)

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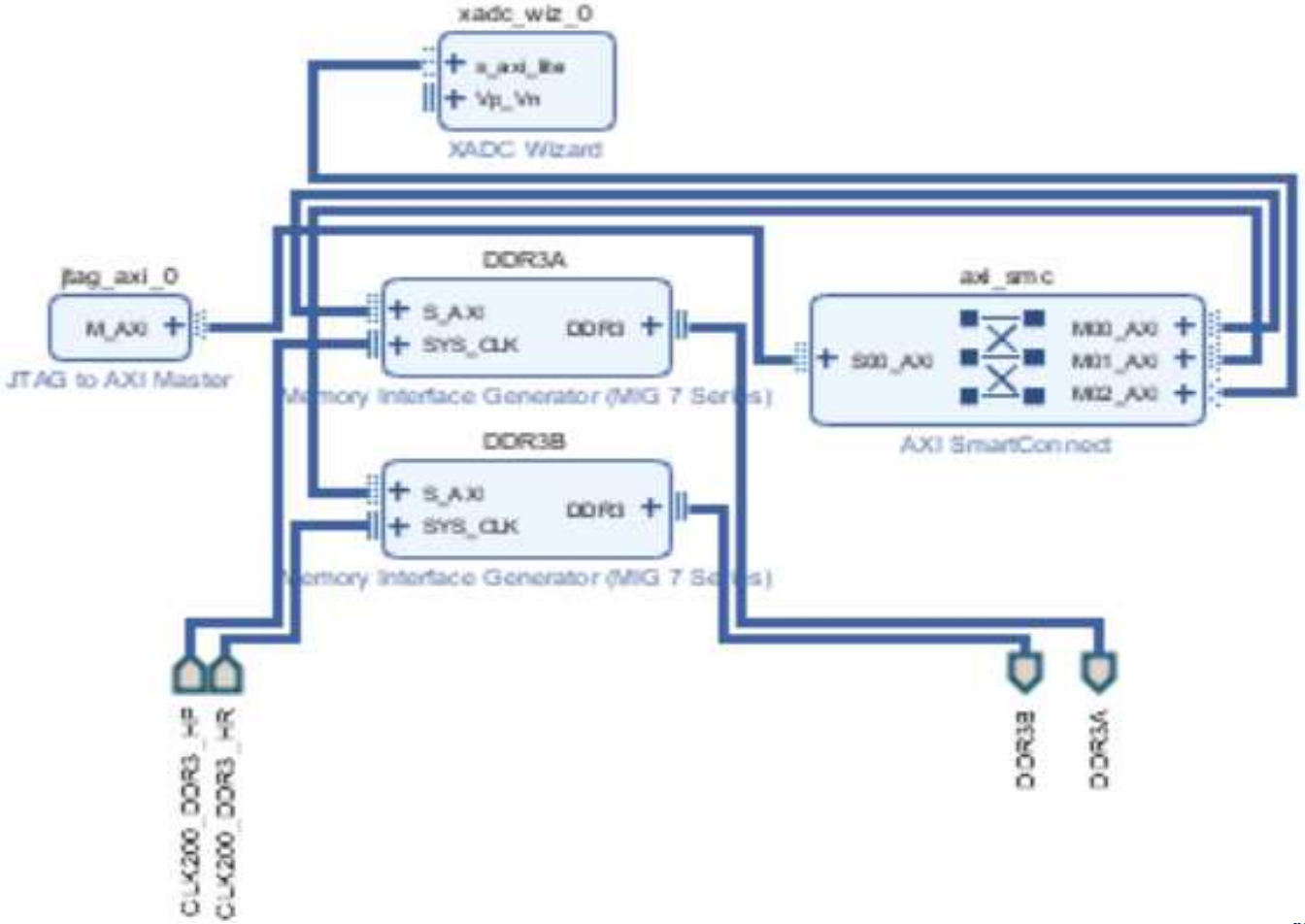
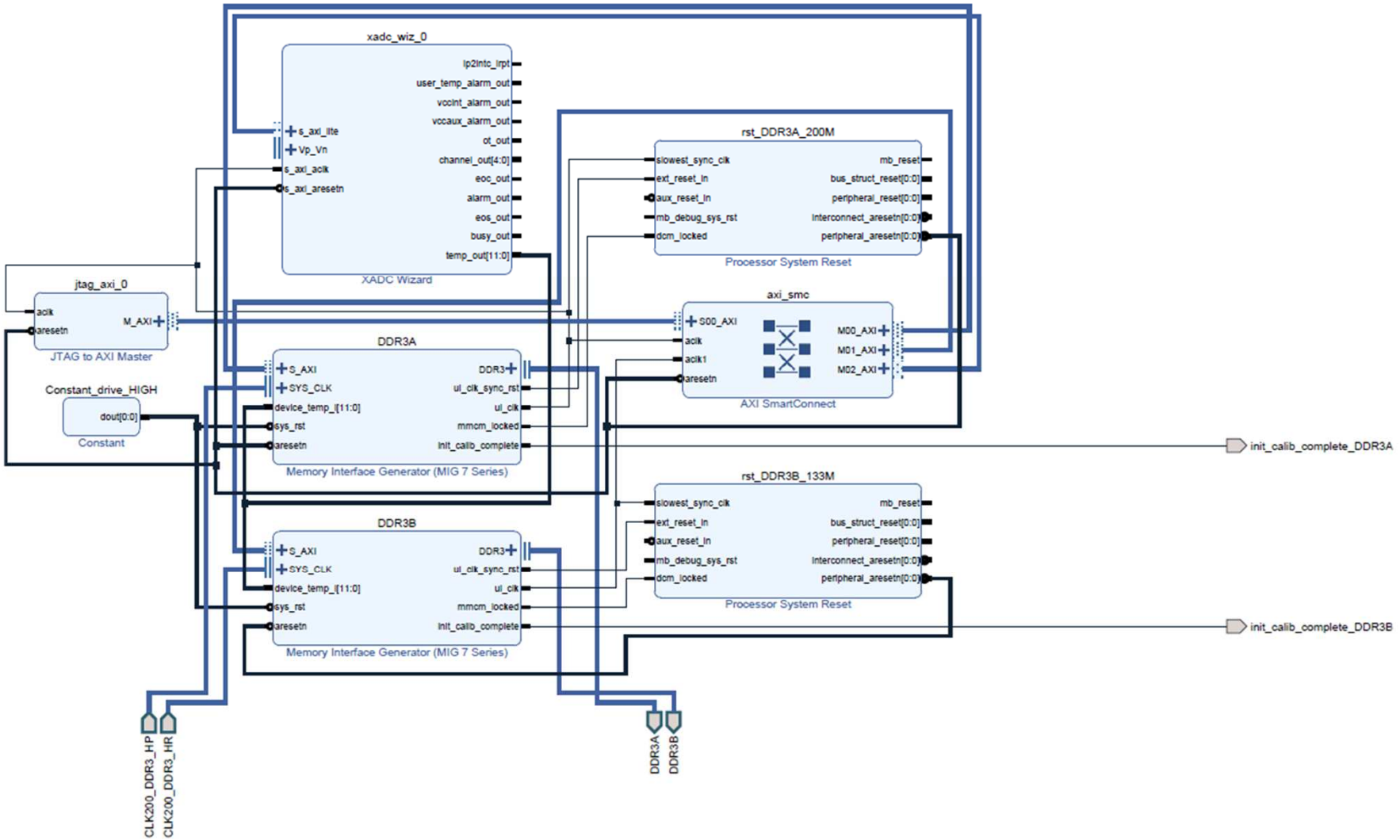
Vivado FPGA design DDR-memory




xadc_wiz_0
ip2intc_irpt
user_temp_alarm_out
vcint_alarm_out
vccaux_alarm_out
ot_out
channel_out[4:0]
eoc_out
alarm_out
eos_out
busy_out
temp_out[11:0]
s_axi_lite
Vp_Vn
s_axi_aclk
s_axi_aresetn
XADC Wizard
rst_DDR3A_200M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
jtag_axi_0
aclk
aresetn
M_AXI
JTAG to AXI Master
axi_smc
S00_AXI
aclk
aclk1
aresetn
M00_AXI
M01_AXI
M02_AXI
AXI SmartConnect
DDR3A
S_AXI
SYS_CLK
device_temp_i[11:0]
sys_rst
aresetn
DDR3
ui_clk_sync_rst
ui_clk
mmcm_locked
init_calib_complete
Memory Interface Generator (MIG 7 Series)
Constant_drive_HIGH
dout[0:0]
Constant
init_calib_complete_DDR3A
rst_DDR3B_133M
Processor System Reset
DDR3B
Memory Interface Generator (MIG 7 Series)
init_calib_complete_DDR3B
CLK200_DDR3_HP
CLK200_DDR3_HR
DDR3A
DDR3B

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FPGA Design System Memory-map

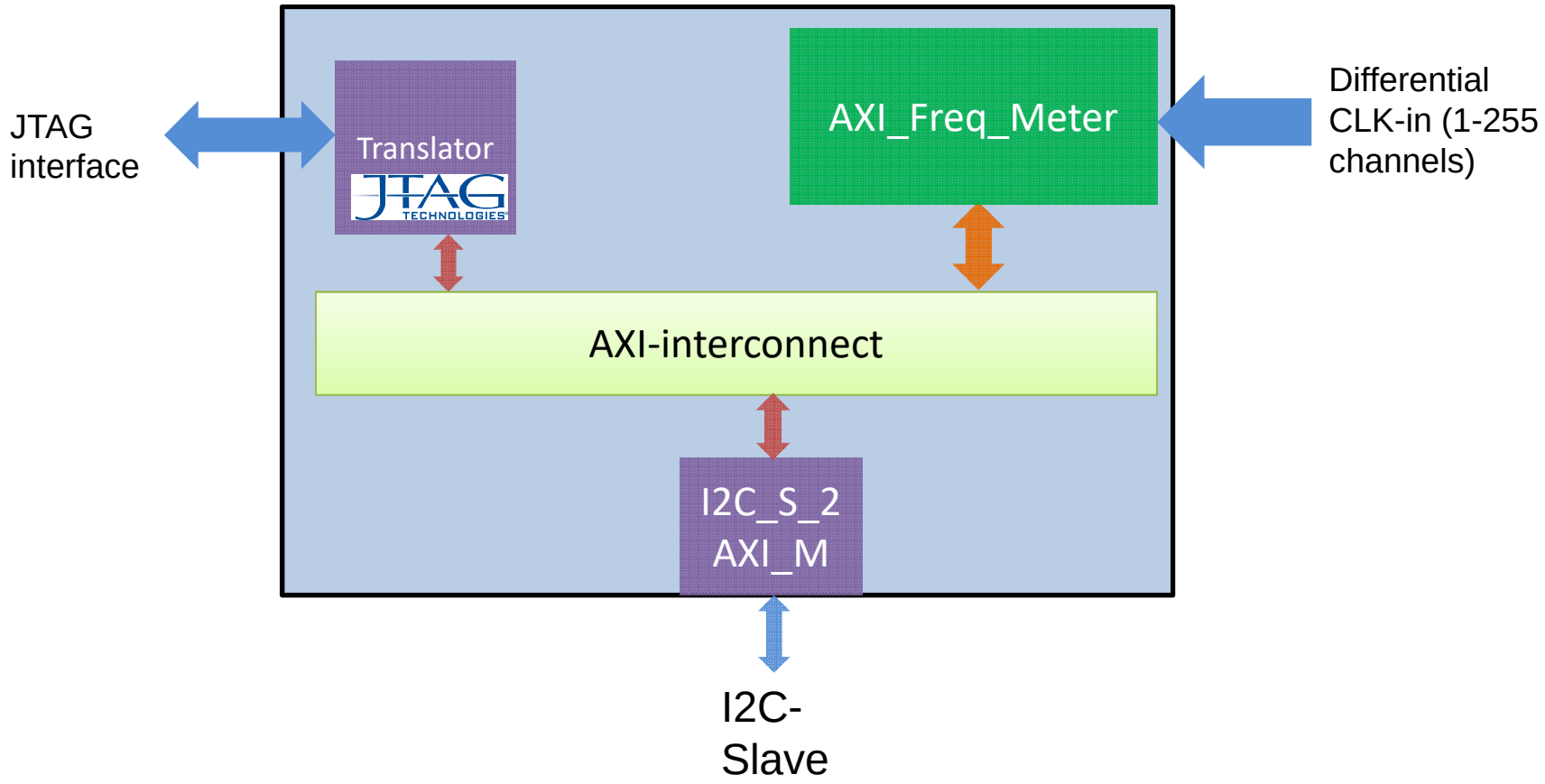
Diagram | Address Editor

Cell	Slave Interface	Base Name	Offset Addre...	Range	High Address
jtag_axi_0					
Data (32 address bits : 4G)					
DDR3A	S_AXI	memaddr	0x8000_0000	1G	0xBFFF_FFFF
DDR3B	S_AXI	memaddr	0xC000_0000	1G	0xFFFF_FFFF
xadc_wiz_0	s_axi_lite	Reg	0x44A0_0000	64K	0x44A0_FFFF

Test sequence

- Load the FPGA-design on-the-fly using JTAG Interface (SVF)
- Wait for Config_done = 1
- Wait for ddr_calib_done=1
- Execute AT-speed test (ProVision, JTAG Technologies)
- If fail: execute boundary-scan diagnostics (BSD, JTAG Technologies)

Example 2: Embedded Frequency-measurement



Again system memory-map

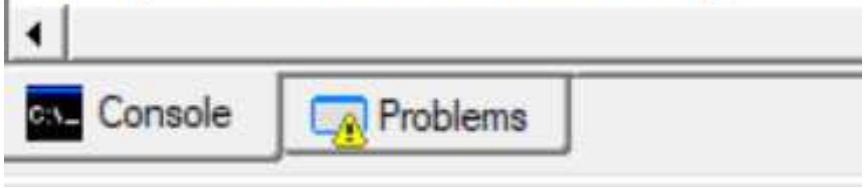
AXI (32 address bits : 4G)					
Frequency	S_AXI	Reg	0x4000_0000	64K	0x4000_FFFF
SelectCh...	S_AXI	Reg	0x4001_0000	64K	0x4001_FFFF

Python script

```
import jft
import jftuproc
import time

jftuproc.Init("Kintex7","","IC7")
jftuproc.EnterDebug()

freq_sel_address =       0x40010000
measure_address =       0x40000000
jftuproc.WriteMemory(0x40010000,0x01)
jftuproc.WriteMemory(0x40010000,0x00)

def MeasureChannel(channel):
    jftuproc.WriteMemory(freq_sel_address,channel)
    val = jftuproc.ReadMemory(measure_address)
    return val

for channel in range(0,8):


    measuredfreq = MeasureChannel(channel)
    print("channel",channel,":",measuredfreq)
```

Executed python-script's output

```
Initializing Jft...
channel 0 : 74187415
channel 1 : 222562247
channel 2 : 148374831
channel 3 : 148374831
channel 4 : 200032982
channel 5 : 200032983
channel 6 : 24579839
channel 7 : 0
Closing Jft...
Script ended successfully.
```



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Benefits

- Easy test integration using our the JTAG Technologies controllers which we already have for years
- Easy test automation using scripting (Python, TCL)
- Faster time-2-market

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Questions?