# *Design Challenges for Testing High Speed Serial Communications*

Design Automation & Embedded Systems 2018
John Marrinan, Director Application Engineers
7th and 8th of November, 2018

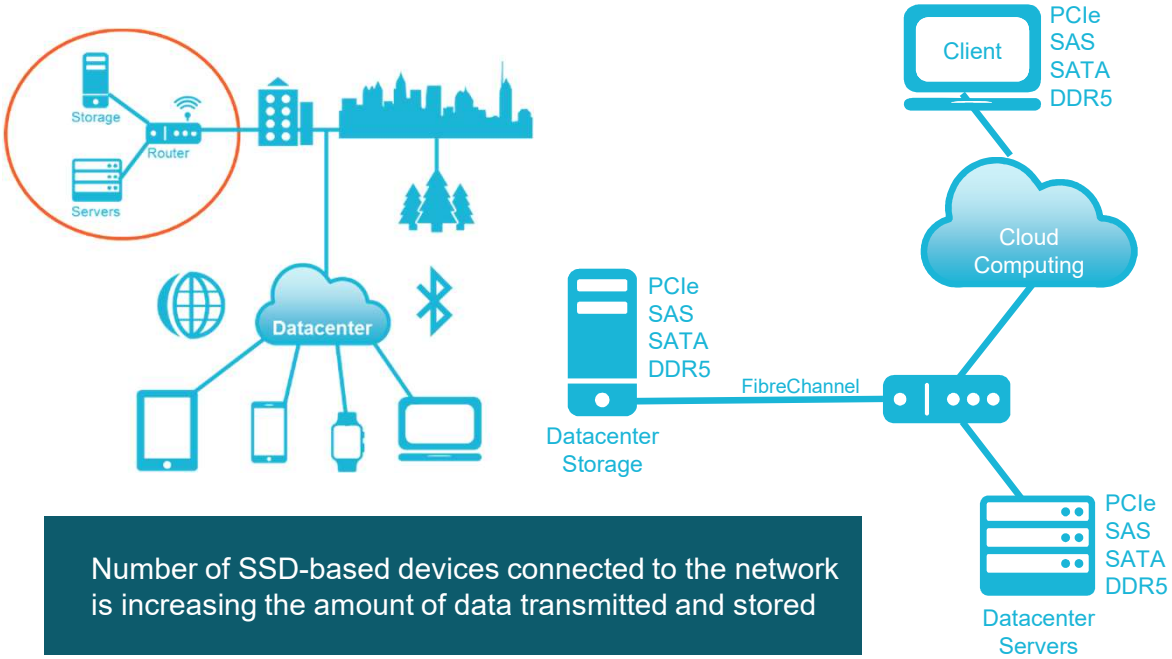
# AGENDA

- Serial Data Link Challenges
- Fundamentals of Serial Data Link Analysis
- Measurement System De-embedding
- Practical Channel Emulation – PCIe Gen3
- Practical Receiver Equalization

# Next Generation Serial Standards

BIG DATA, AUTOMOTIVE, IOT AND ANALYTICS DRIVING NEED FOR

COMPUTE POWER, STORAGE CAPACITY, AND NETWORK BANDWIDTH



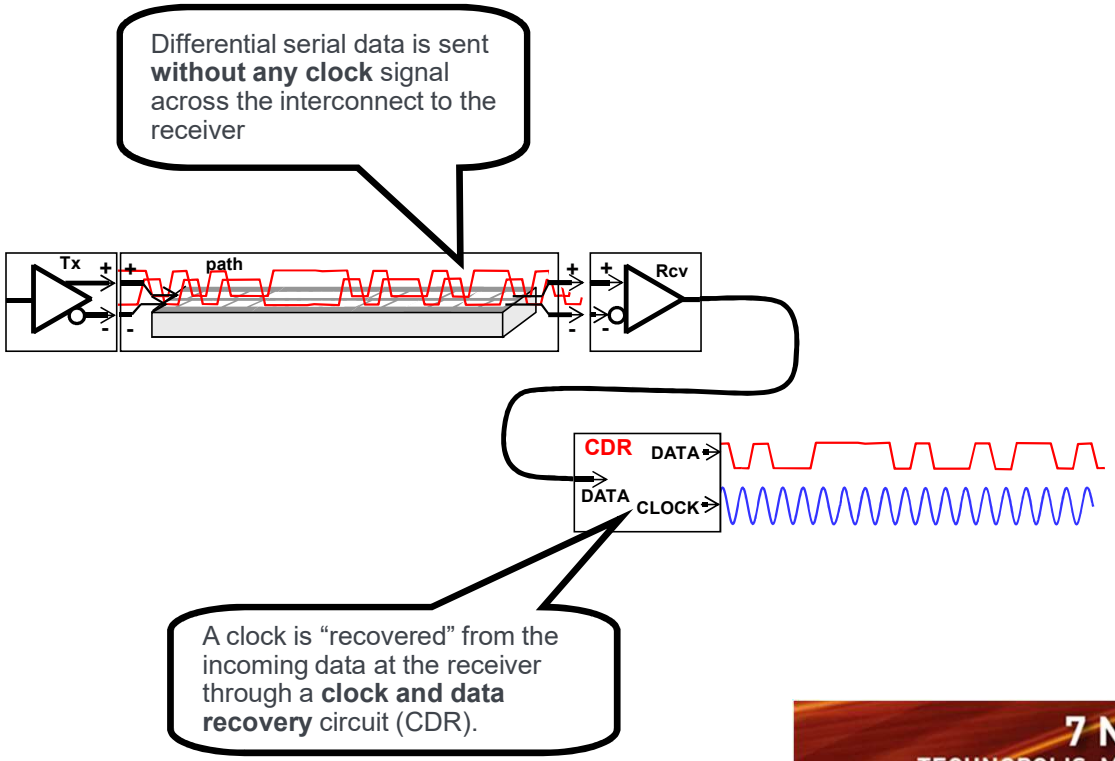

Number of SSD-based devices connected to the network is increasing the amount of data transmitted and stored

| Standard | Data Throughput |
|---|---|
| PCIe Gen3 -> Gen4 | 8GT/s -> 16GT/s |
| SAS3 -> SAS4 | 12Gb/s -> 22GB/s |
| USB3.0 -> USB3.1 | 5Gb/s -> 10Gb/s |
| DDR4 -> DDR5 | 3.2GT/s -> 6.4GT/s |
| 100G -> 400G | 25Gbd -> 56Gbd |

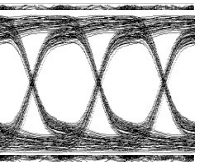
- **Cloud, Connectivity, Computing, Auto**
- **Doubling of Data Rates from One Generation to The next**

# Design and Test Challenges
# Transmission Path of a High Speed Serial

**Ideal State**

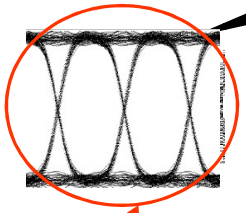


# Design and Test Challenges
# Transmission Path of a High Speed Serial

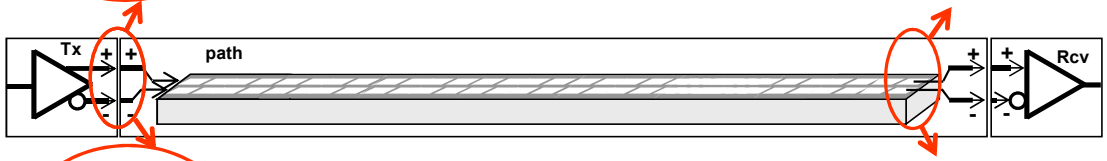


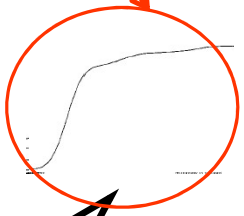
**The Reality**

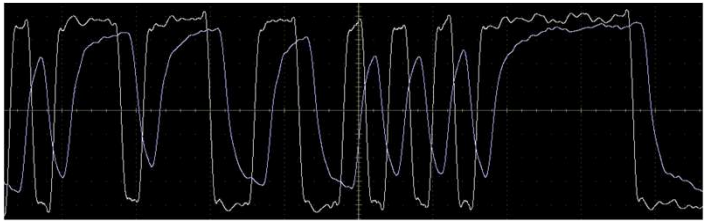
Clean, open, logical 1 & 0 at launch from transmitter



Logical 1 & 0 can be hard to distinguish at end of long interconnects; (this is often called a "closed eye")



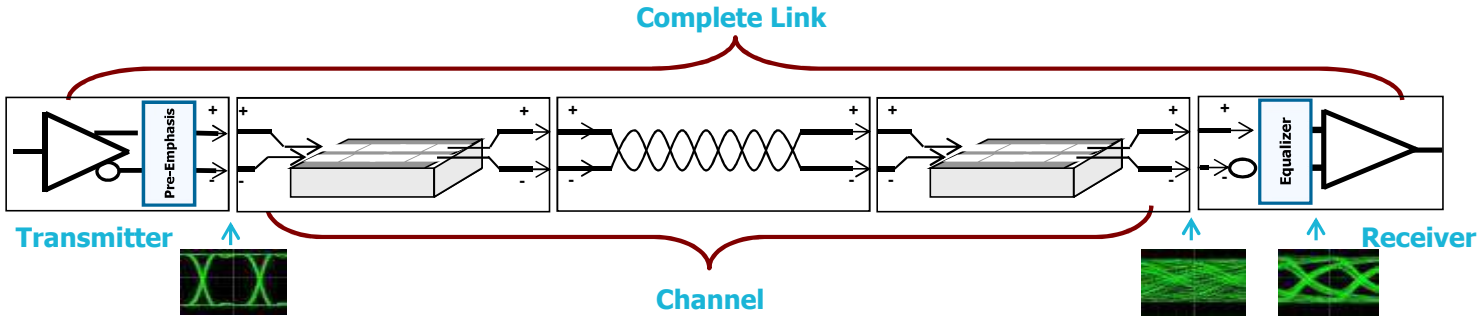


Fast, sharp, edges at transmitter launch

Smeared edges at end of long interconnect.

Reference Maxim Note HFDN-27.0 (Rev. 0, 09/03)

# Anatomy of a Serial Data Link




**Aspirational goal: 0 errors**
**Practical Goal: Bit Error Rate < Target BER**

**Since BER is the ultimate goal, why not measure it directly?**

# Serial Data Link Integrity = Bit Error Ratio

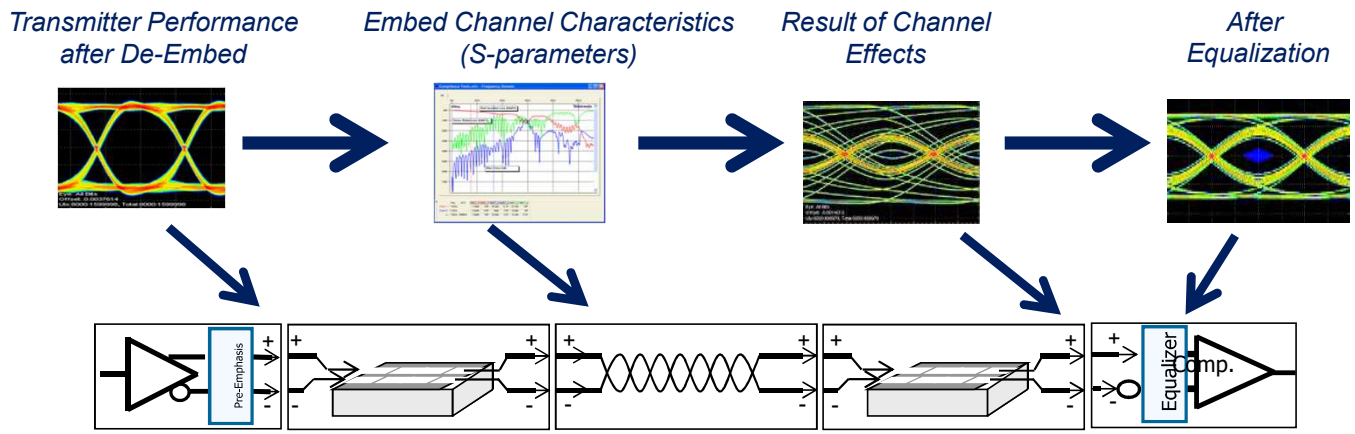
- **Bit Error Ratio Testers (BERTs) are the tools for measuring BER directly**
- **Why not use ONLY BERTs for Serial Data Link Analysis?**
  - ❑ **Difficult to model/emulate the equalizer**
  - ❑ **Measurements can take a very long time**
  - ❑ **Instruments are very expensive and not all that flexible**
  - ❑ **Does not analyze the root causes of the impairments of the links**
- **Alternative approach: use a scope and advanced jitter and noise analysis tools**
  - ❑ **Easily move from Compliance to Debug**
  - ❑ **Better equipped to identify root causes of eye closure**
  - ❑ **Equalizer can easily be modeled**
  - ❑ **More cost effective**
  - ❑ **Greater throughput**

**BER requirements have been translated to Jitter (and more recently, Noise) budgets**

| Characteristic | Units | Minimum | Nominal | Maximum | Reference |
|---|---|---|---|---|---|
| Tx RJ [b c d] | UI | 0.135 [e] | 0.150 [f] | 0.165 [g] | 5.8.4.6.1 |
| Tx SJ [c] | UI | See figure 129 and figure 130 | | | 5.8.5.7.4.5 |
| WDP at 6 Gbps [b h] | dB | 13 | | 14.5 | |
| NEXT offset frequency [i j k] | ppm | 2 500 | | | |
| Total crosstalk amplitude [i k] | $mV_{rms}$ | 4 | | | |
| Receiver device configuration [l] | | | | | |

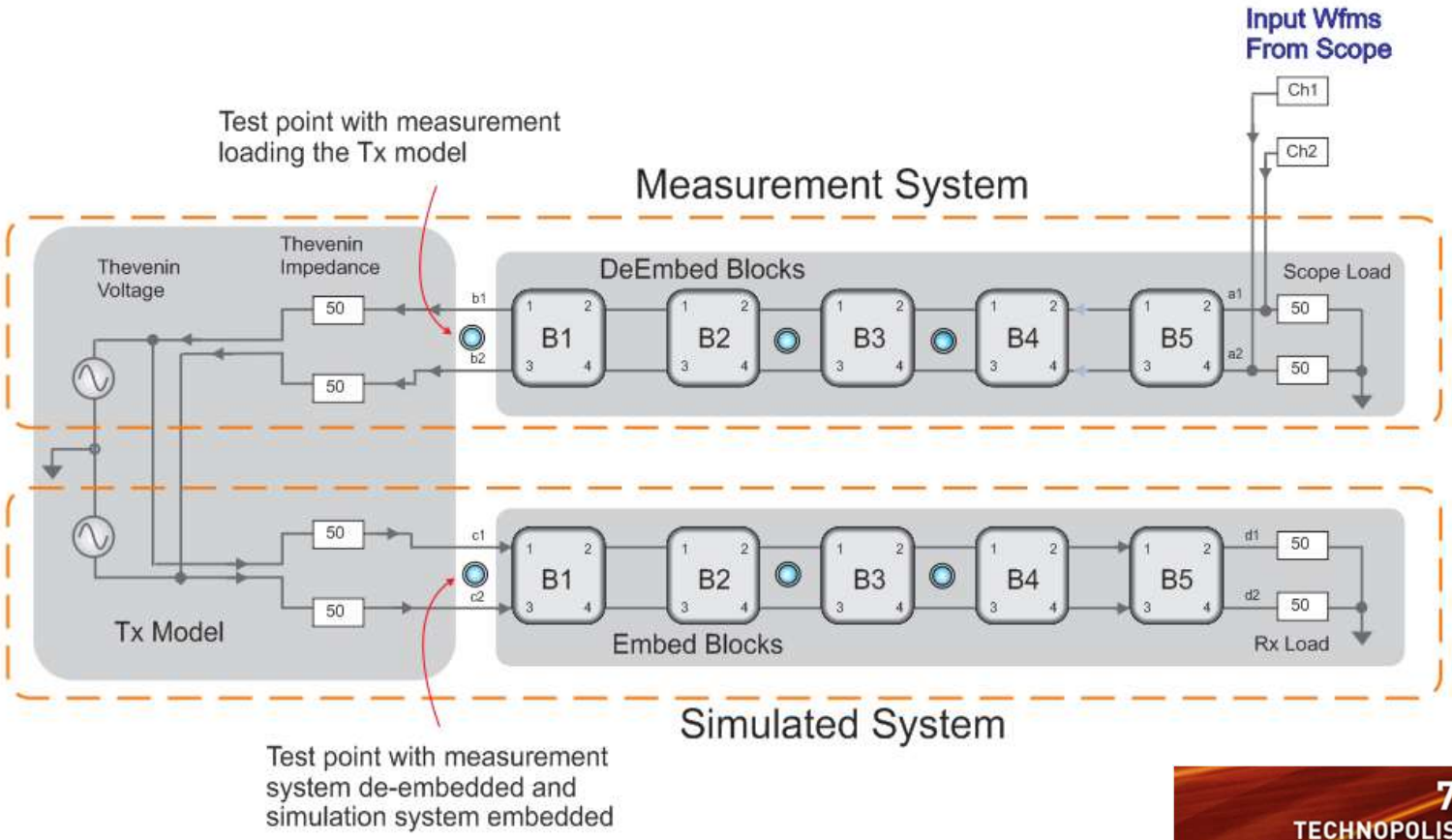
[a] For a characteristic with only a nominal value, the test setup shall be configured to be as close to that value as possible while still complying with other characteristics in this table.
[b] For characteristics with minimum and maximum values, the test setup shall be configured to be within the range specified by the minimum and maximum values. The range shall not be used to define corner test conditions required for compliance.

# Fundamentals of Serial Data Link Analysis

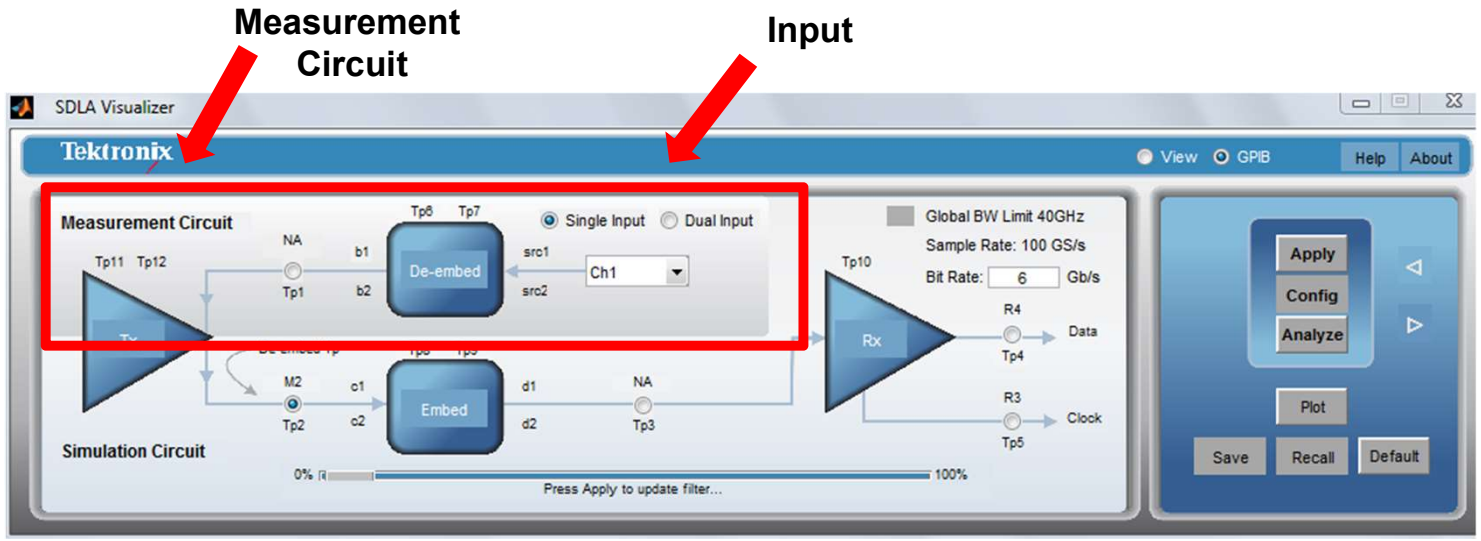


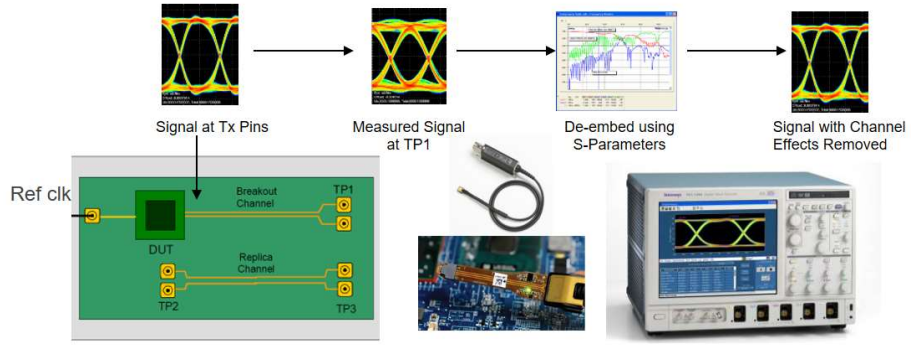

- ***De-embed*** measured circuit as needed, to remove the effects of the test fixture, cables and/or the channel to characterize the Transmitter
- ***Embed*** the simulation circuit: observe the waveform at the receiver pins
- Emulate the ***Equalization*** *inside the Rx*: observe the waveform at the comparator

# SDLA Tool Set Have Two Components



# De-embedding Test Equipment Effects

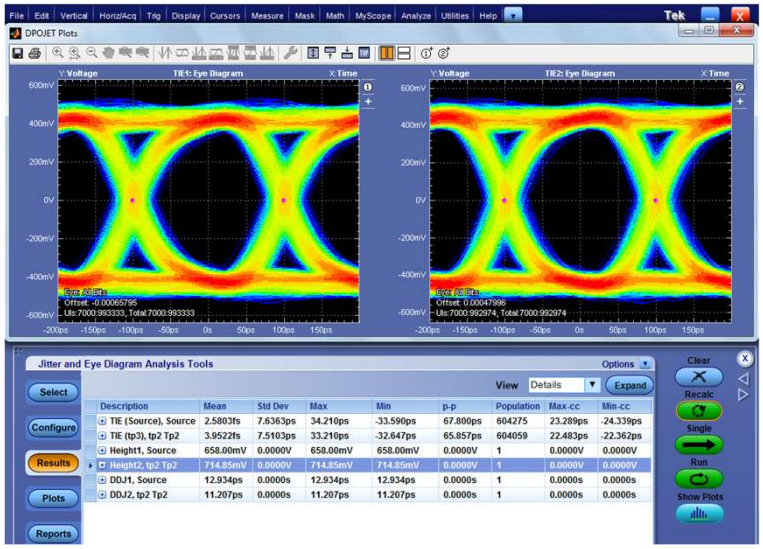


# *De-Embed* the Measurement Circuit – Coax Cables

- Removal of the effects of measurement equipment is required and necessary for many next generation standards
- Compensating for loss and reflections due to the measurement circuit is required
- The example below shows an 8Gb/s signal before and after the removal of SMA cables

Before De-Embedding
Eye Height
~660mV

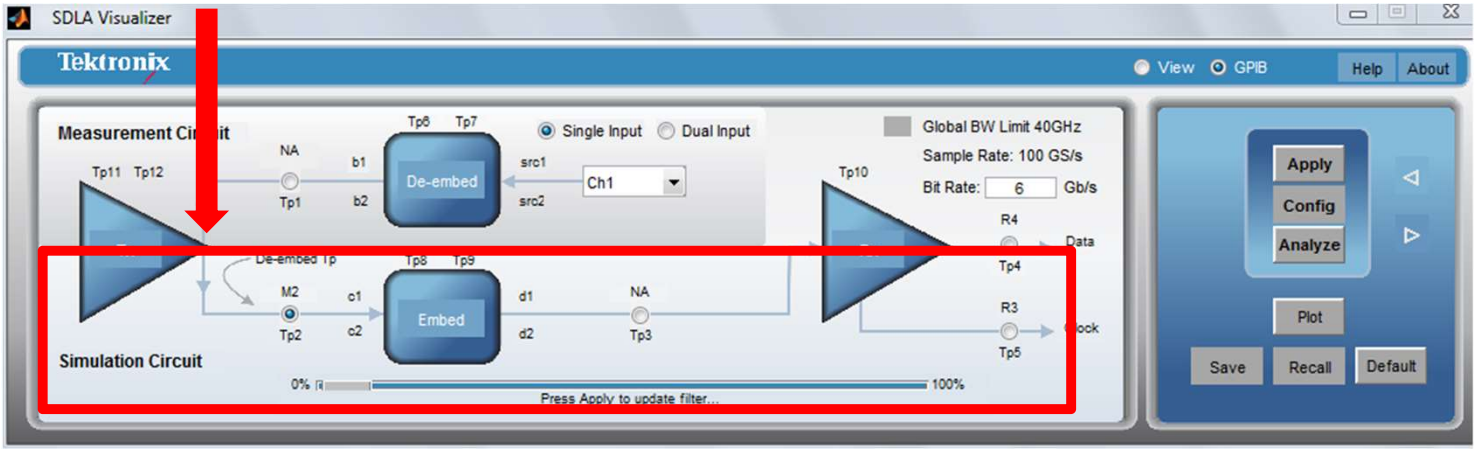


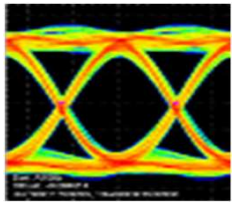

After De-Embedding
Eye Height
~715mV

+ 9%

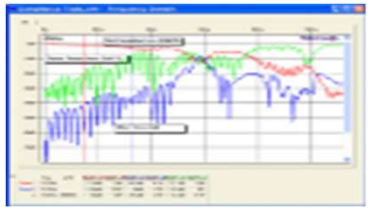
# Embedding Channel Effects

**Simulation Circuit**

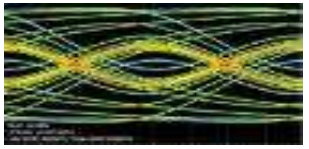


**Signal Acquired or after de-embedding**



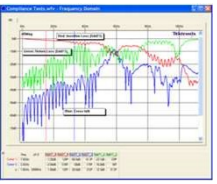
**Embed Compliance Channel and Package**

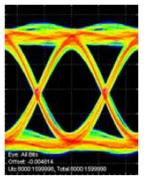


**Closed Eye due to the Channel**

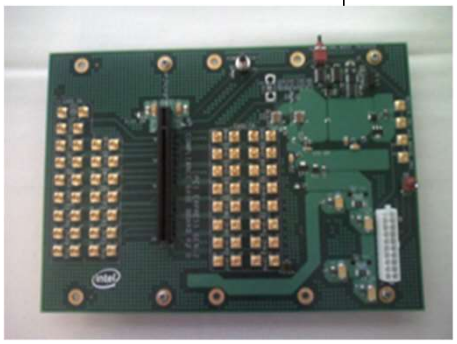
# Fundamentals of Serial Data Link Analysis

## *Example using PCI Express 3.0*

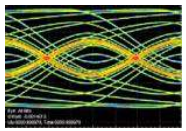




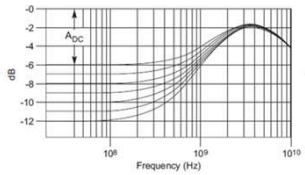
Signal Acquired from Compliance Board



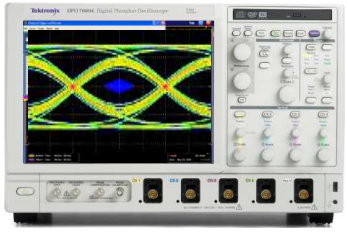
Embed the Add-In Card Compliance Channel



Closed Eye due to the Channel




Apply the Base Specification CTLE + Dfe for Long Channel



Open Eye for Measurements

System Board Eye Limits

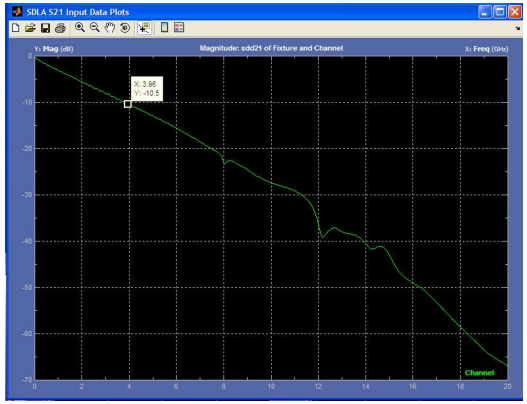
| Parameter | Min | Max | Units |
|---|---|---|---|
| $V_{TXS}$<br>$V_{TXS\_d}$ | 34<br>34 | 1200<br>1200 | mV<br>mV |
| $T_{TXS}$ | | 41.25 | ps |

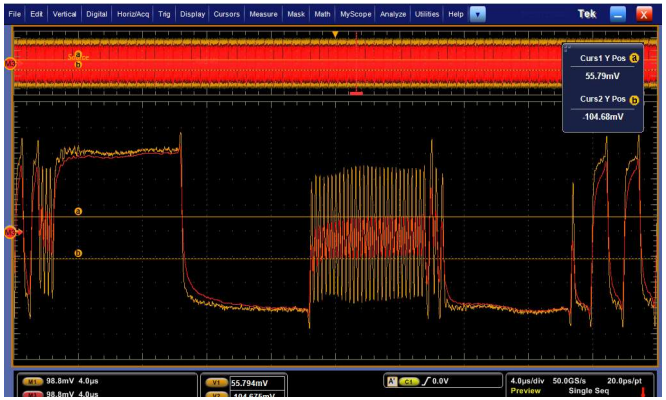
Add-In Card Eye Limits [1]

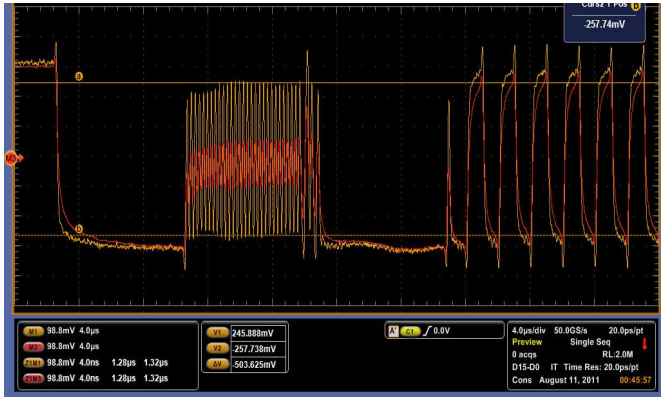
| Parameter | Min | Max | Units |
|---|---|---|---|
| $V_{TXA}$<br>$V_{TXA\_d}$ | 50<br>50 | 1200<br>1200 | mV<br>mV |
| $T_{TXA}$ | | 41.25 | ps |

# Embed Simulation Circuit (Compliance Channel)

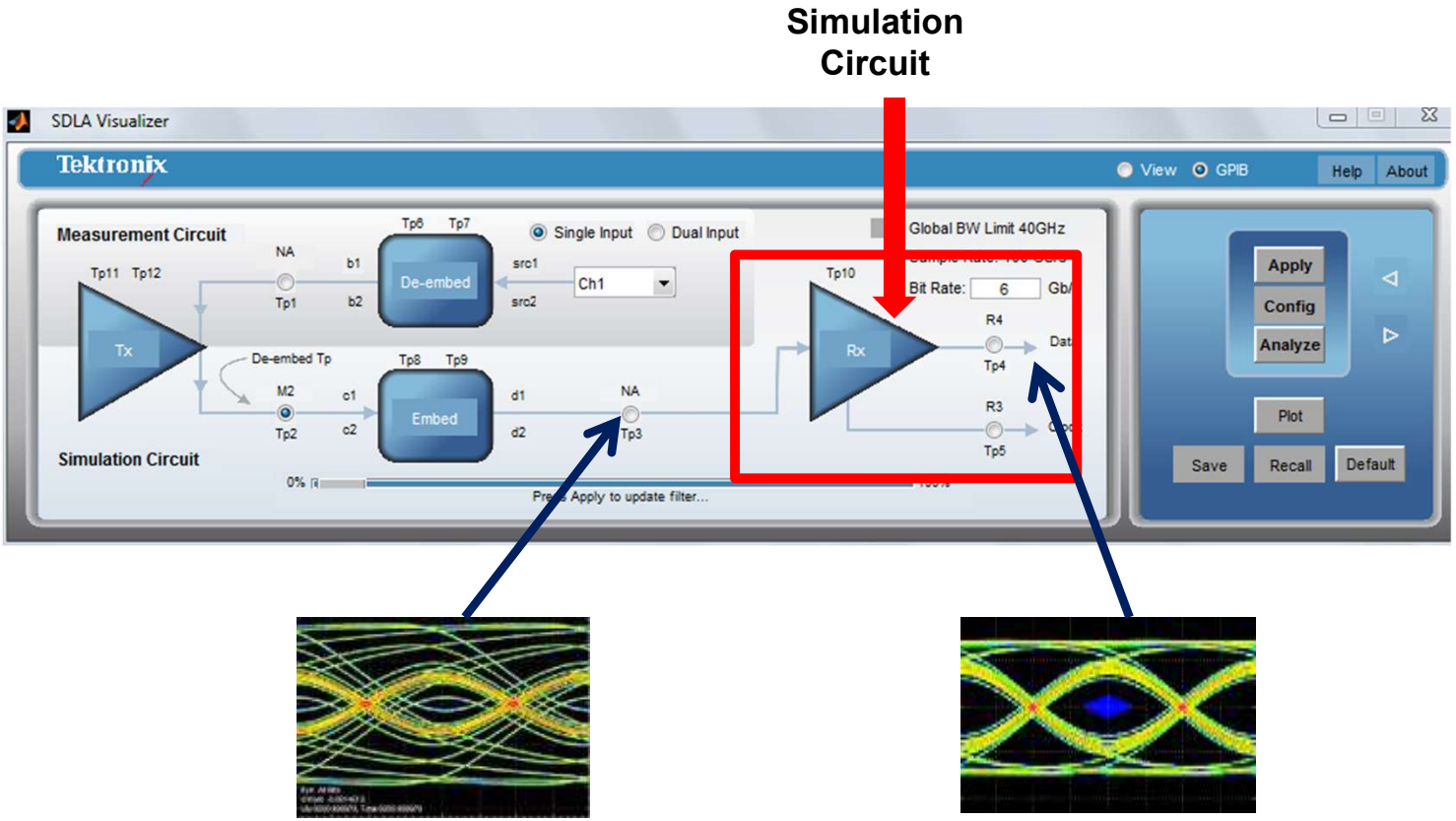
- Verifying the effects on the waveform are correct can be done by looking at the S-parameters of the channel model
  - Based on the PCIe 3.0 Add-In Card Compliance Channel, 10dB (0.3 voltage) attenuation is expected on high frequency bits (4GHz for PCIe Gen 3)



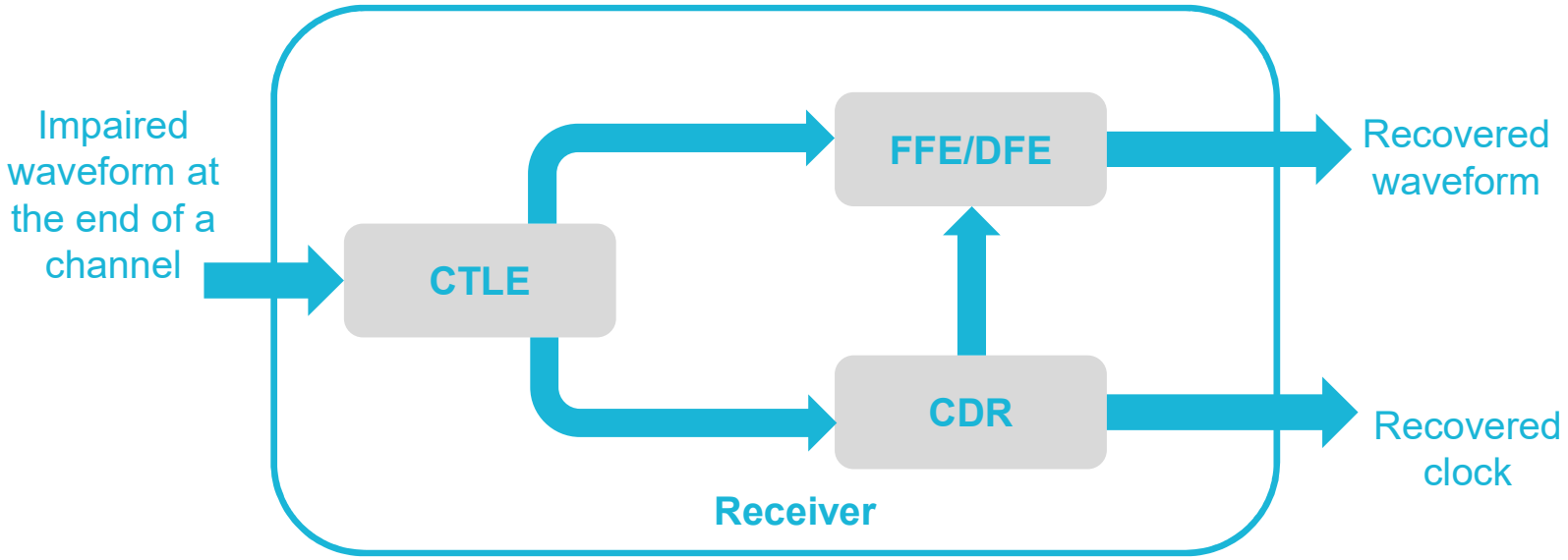



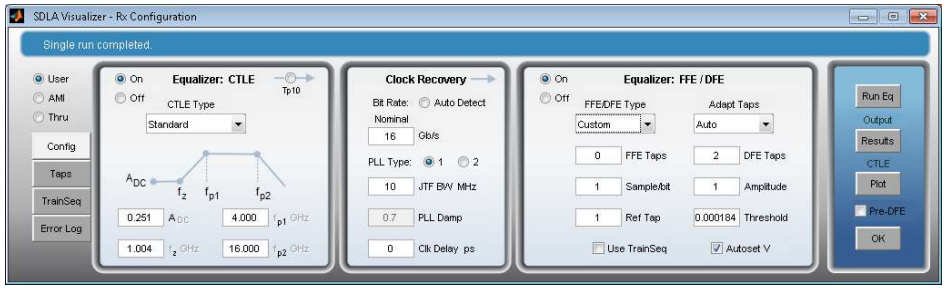



# Rx Equalization Create TP2’ Eye



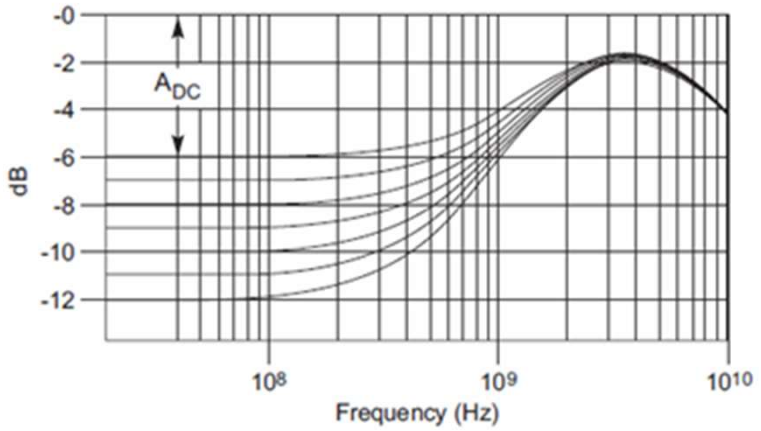
# Generic Rx Equalizer



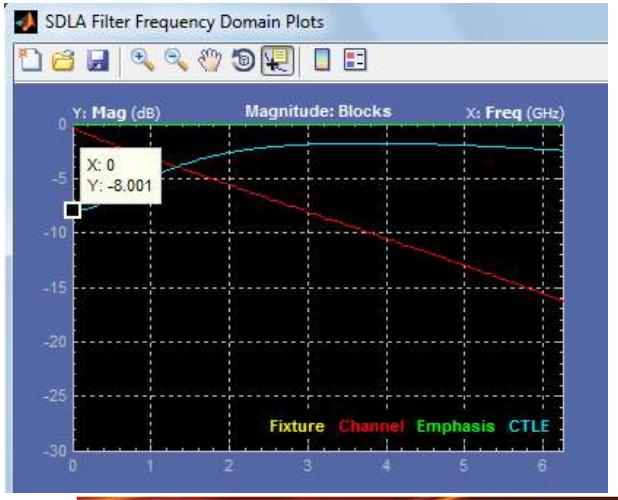



# Apply *Receiver Equalization*

- Equalizer is optimized on the CTLE + DFE tap value that results in the best eye area
  - 8dB (~60% attenuation) Adc settings are shown in the example below
- PCIe reference equalizer is CTLE and 1 Tap DFE
  - CTLE – one Zero and Two Poles
  - DFE – 1 Tap (-20/20mV tap value)







# Validate CTLE EQ

*Analyze Raw and CTLE EQ Waveform*

- Measure the low frequency content of the signal on the acquired waveform (Orange) 615mV approx.
- Based on the CTLE that was applied, we expect a 60% attenuation in the low frequency content after the CTLE 240mV


# Apply *Receiver Equalization*

## *Validate Equalizer: Analyze DFE*

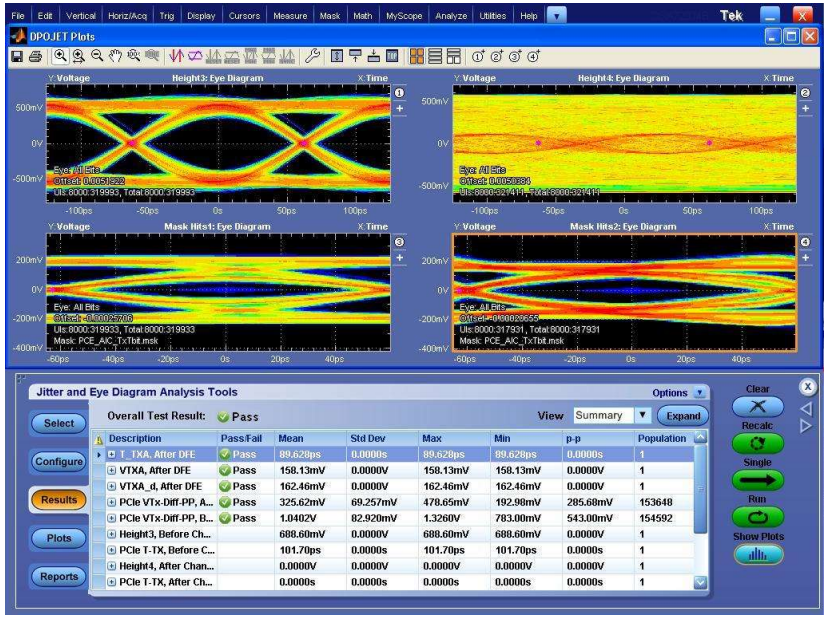
- The DFE will open the eye by twice the tap value
- PCIe uses a 1 tap DFE, meaning that the previous bit will determine if change of the current bit.
- The table below outlines the change based on the 20mV Tap
- High frequency signal before DFE is 126mV and after 166mV, which is 2 times the tap value of 20mV

| Previous Bit | Current Bit | Change |
|---|---|---|
| 0 | 1 | 20mV |
| 1 | 0 | -20mV |
| 0 | 0 | No Change |
| 1 | 1 | No Change |

# Final Results

*PCI Express Compliance Measurements*

- PCIe CEM compliance measurements can now be made on the TP2' waveform (after the EQ and CDR stages). Better correlation with BER
- Simultaneous assessment of the signal at each point during the post processing stage



# Summary

- Traffic Demands in Datacentres and Automotive Industries driving doubling in data rates.
- High Speed Serial Data Links Suffer Frequency Related Losses In Channels
- Test Equipment Utilising New Emulation Technics To address This
- DSP Technics In Oscilloscopes Are Used To Remove Non-Ideal Effects of Measurement Equipment Improving Margin
- Similar Techniques Are Used to Emulate The Effect of Channel Losses and Receiver Equalisation
- These Techniques, Plus The Ability To Incorporate Emulation and Models into Scope DSP Processing Allows Better Correlation Between the PHY later and BER performance

# Questions?

## More information?

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