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Multiple-clock Domain in FPGA Designs: Challenges & Solutions

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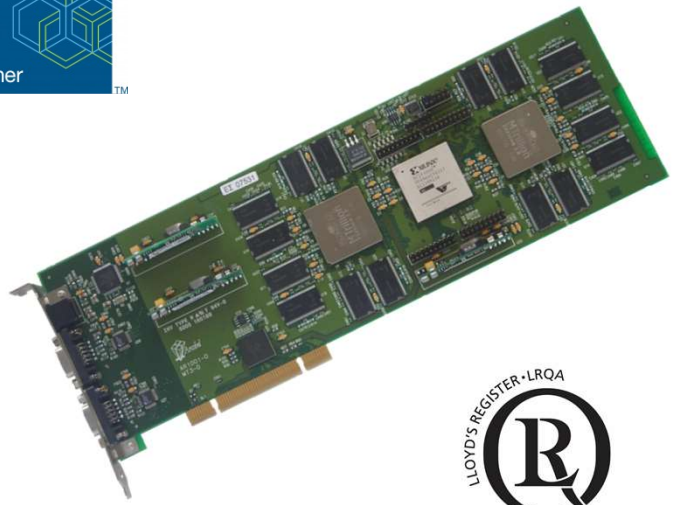
Core|*Vision*

- **Core|Vision has more than 175 man years of design experience in hard- and software development. Our competence areas are:**
  - System Design
  - FPGA Design
  - Consultancy / Training
  - Digital Signal Processing
  - Embedded Real-time Software
  - App development, IOS Android
  - Data Acquisition, digital and analog
  - Modeling & Simulation
  - PCB design & Layout
  - Doulos & Xilinx Training Partner
  - **Clock Domain Crossing Training & support**



vSync Circuits

- **EDA & IP Company**

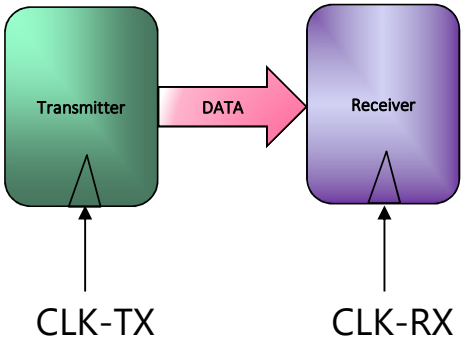
- **Mission:**
  - Develop and provide our customers with ***Integration*** and ***Verification*** solutions for Multiple Clock Domain Designs

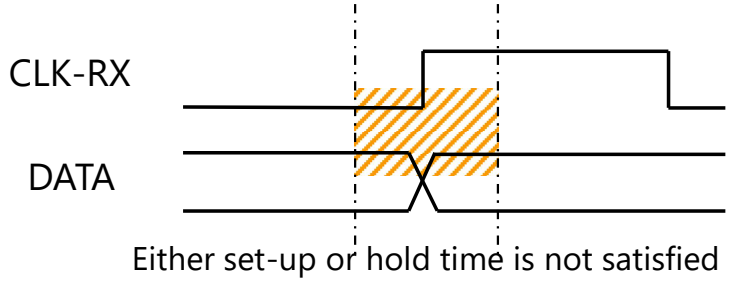
Outline

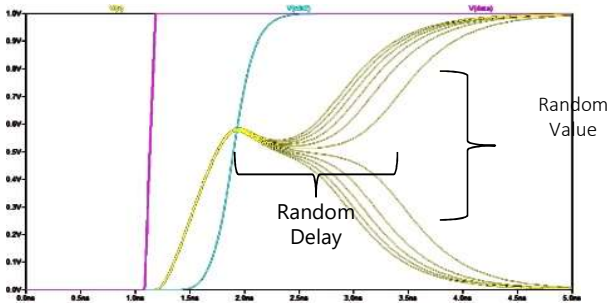
- **Multiple-Clock Domain (MCD) Designs**
  - A Few anecdotes
  - Tips & Tricks
- **3 MCD Challenges**
- **A note on Vincent (on whom?)**

Recall: Inter-Clock Domain Communication

- **Incoming data change near RX clock edge causes *metastability***
  - Leads to functional failure due to
    - Non-deterministic propagation delay
    - Non-deterministic resolution value







Reuven Dobkin,FPGA Kongress, Munich, 2018

Recall: How to … Make it wrong …

- **Make it wrong by …**
  - Avoiding Synchronization
  - One Flop Synchronizer
  - Sneaky Path
  - Greedy Path
  - Flakey Protocol
  - Async Clear
  - DFT Leak
  - Power Optimization Leak
  - Pulse Synchronizer
  - Slow-to-Fast Synchronizer
  - Recovergence Path
  - Conservative Synchronizer
  - Glitching Control Path
  - Bad Constraining

R. Dobkin, R. Ginosar and C. Sotiriou, High Rate Data Synchronization in GALS SoCs, IEEE Trans. on VLSI, 14(10):1063-1074, Oct. 2006
R. Dobkin and R.Ginosar, Two phase synchronization with sub-cycle latency, INTEGRATION, the VLSI journal, 2009.
D. Verbitsky, R. Dobkin, S. Beer and R. Ginosar, StarSync: An Extendable Standard-cell Mesochronous Synchronizer, Integration—the VLSI Journal, 2014
R. Dobkin, Asynchronous Reset Synchronization and Distribution, embedded.com, 2017

Recall: How to … *Make it correct …*

- **Make it correct use …**
  - Universal Synchronizer
  - Handshake event driven Synchronizer
  - **FIFO Gray-code based Synchronizer**
  - Periodic Synchronizer
  - Mesochronous Synchronizer
  - Predictive Synchronizer
  - Adaptive Synchronizer
  - Local-delay latching Synchronizer
  - **Asynchronous reset Synchronizer**
  - Glitch-free gator
  - Glitch-free clock switch
  - Quasi-static Synchronizer
  - Fast h/s Synchronizer with MTFB trade-off

R. Dobkin, R. Ginosar and C. Sotiriou, High Rate Data Synchronization in GALS SoCs, IEEE Trans. on VLSI, 14(10):1063-1074, Oct. 2006
R. Dobkin and R.Ginosar, Two phase synchronization with sub-cycle latency, INTEGRATION, the VLSI journal, 2009.
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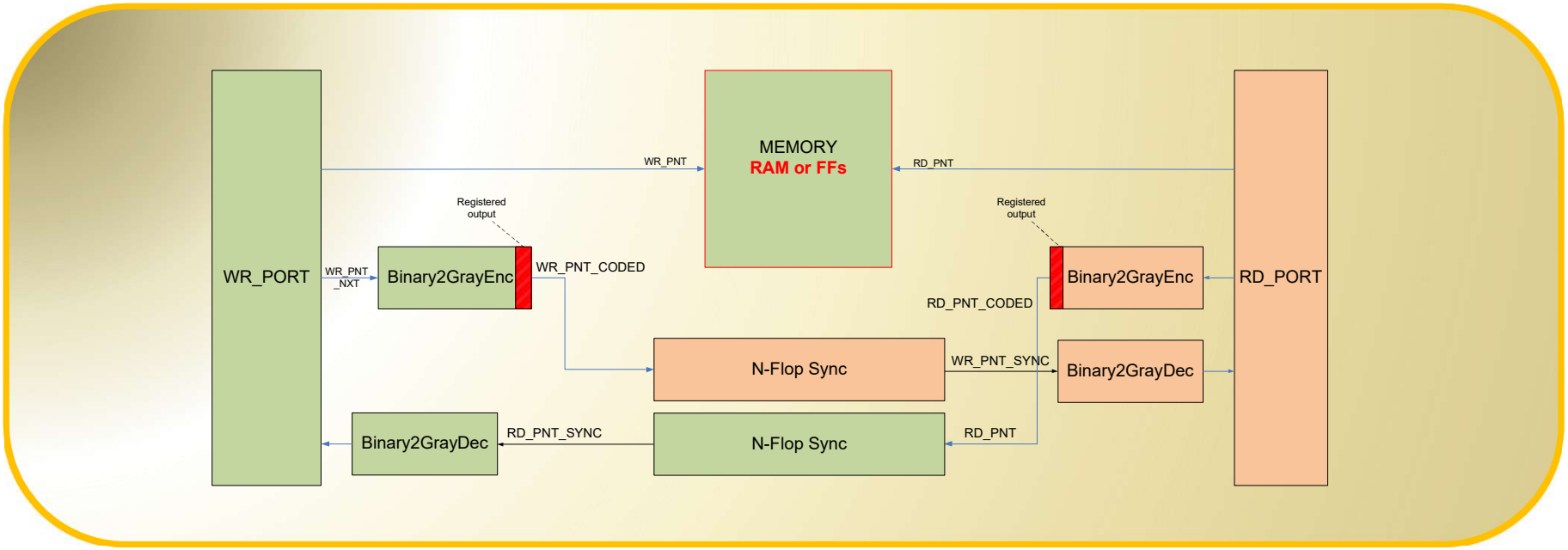
R. Dobkin, Asynchronous Reset Synchronization and Distribution, embedded.com, 2017

A few notes on FIFO design (1)

- **Eliminate glitching into Sync:**
  Gray Encoder output must be sampled

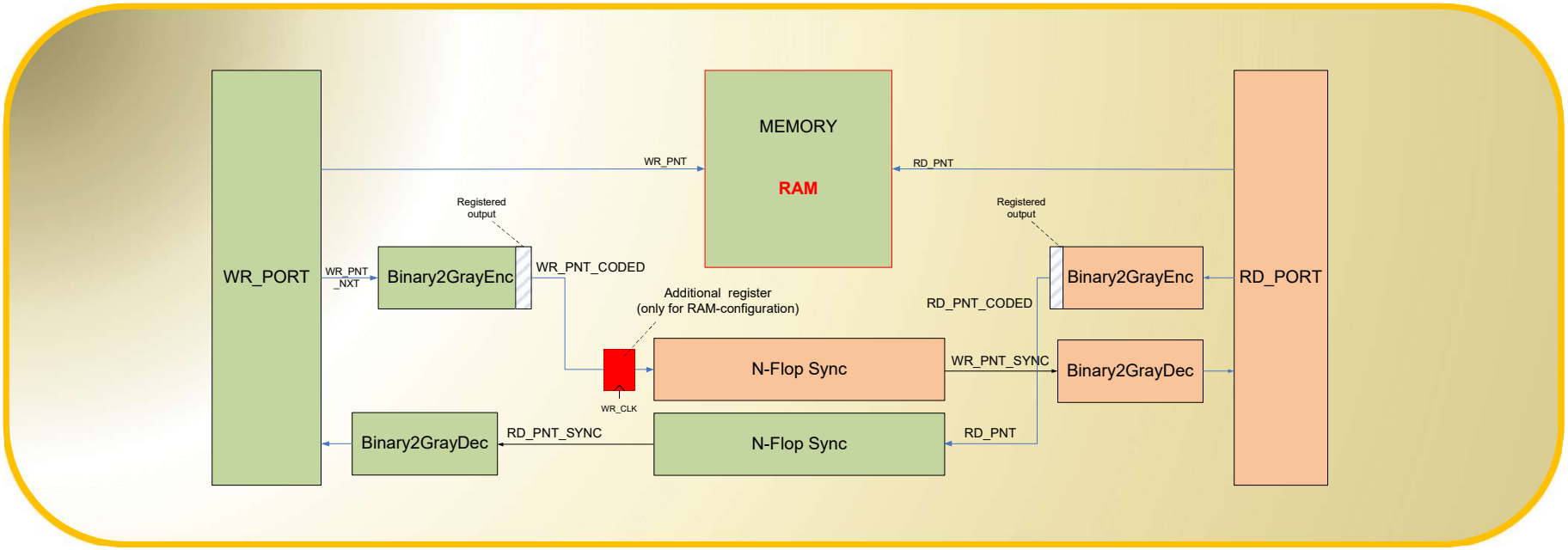


Reuven Dobkin,FPGA Kongress, Munich, 2018

REF: R. Dobkin, Asynchronous two-clock FIFO design key points, Elektronikpraxis, 2018

A few notes on FIFO design (2)

- **RAM write could be "tricky":**
  Check out the RAM specification for write latency

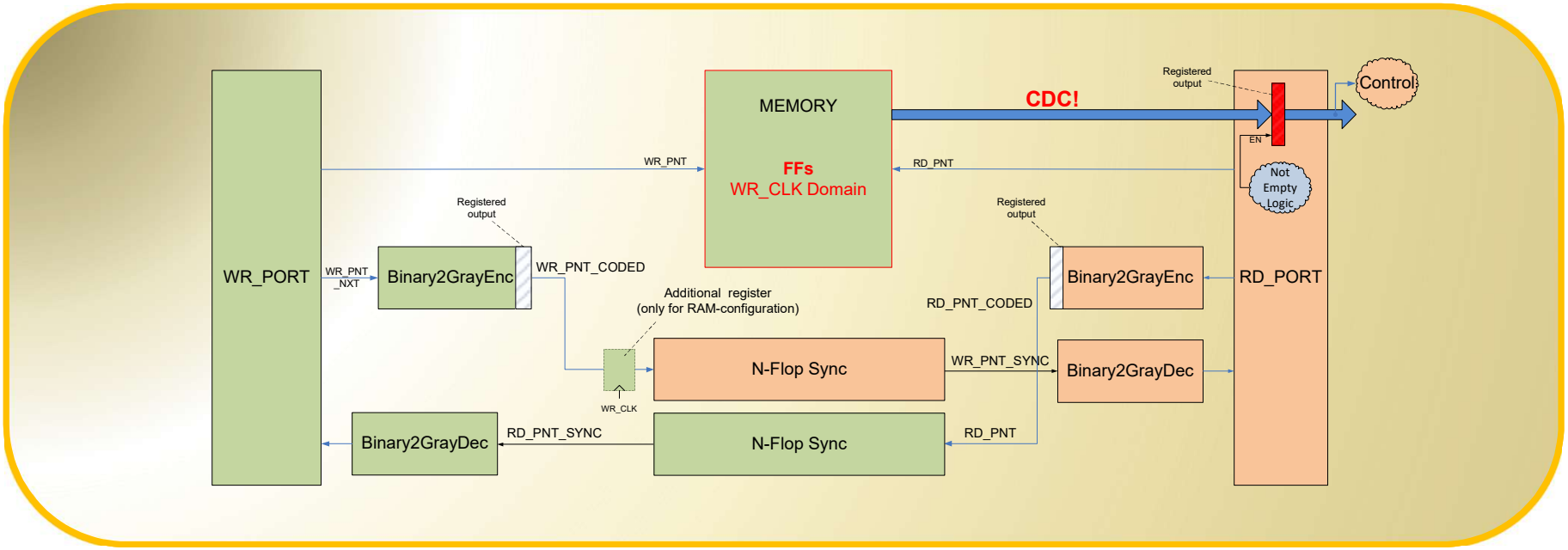


Reuven Dobkin,FPGA Kongress, Munich, 2018

REF: R. Dobkin, Asynchronous two-clock FIFO design key points, Elektronikpraxis, 2018

A few notes on FIFO design (3)

- **Register Read side data output**
  + enable (*who knows how it is used further…*)

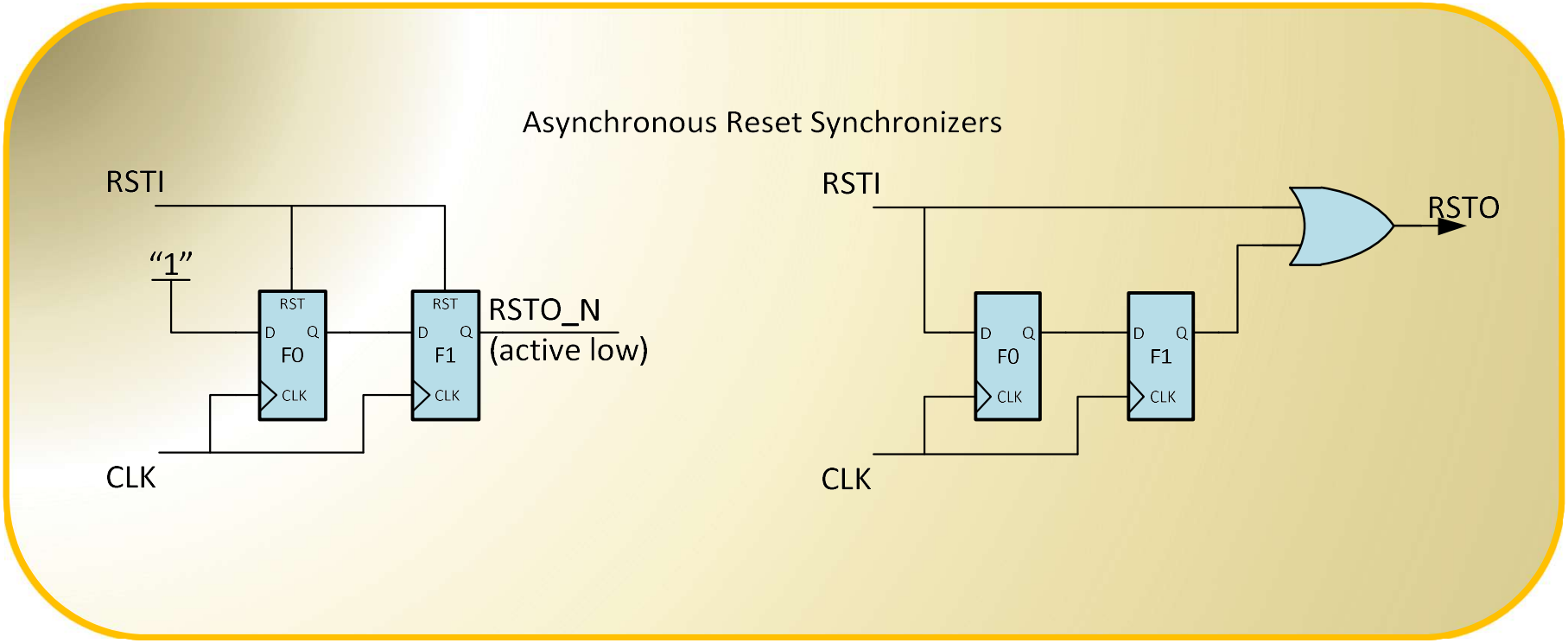


Reuven Dobkin,FPGA Kongress, Munich, 2018

REF: R. Dobkin, Asynchronous two-clock FIFO design key points, Elektronikpraxis, 2018

Asynchronous Reset CDC (1)

- **Reset must meet setup/hold constrains**

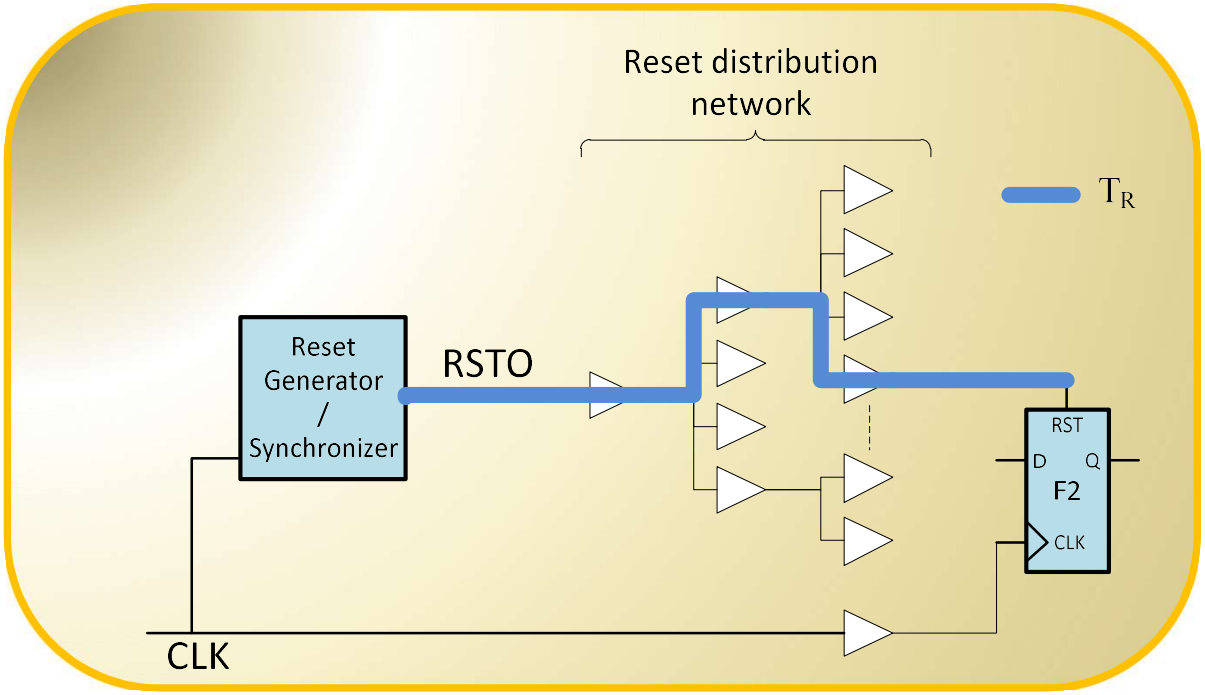


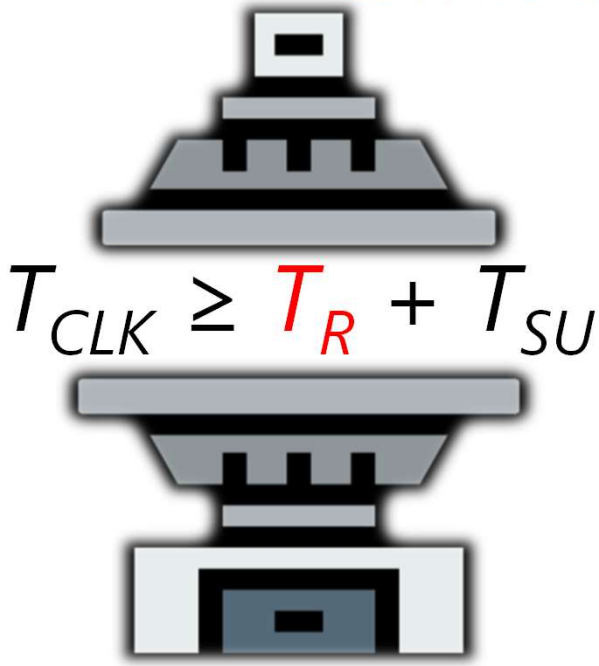
Reuven Dobkin,FPGA Kongress, Munich, 2018

REF: R. Dobkin, Asynchronous Reset Synchronization and Distribution, embedded.com, 2017

Asynchronous Reset CDC (2)

- **Reset must meet setup/hold constrains**





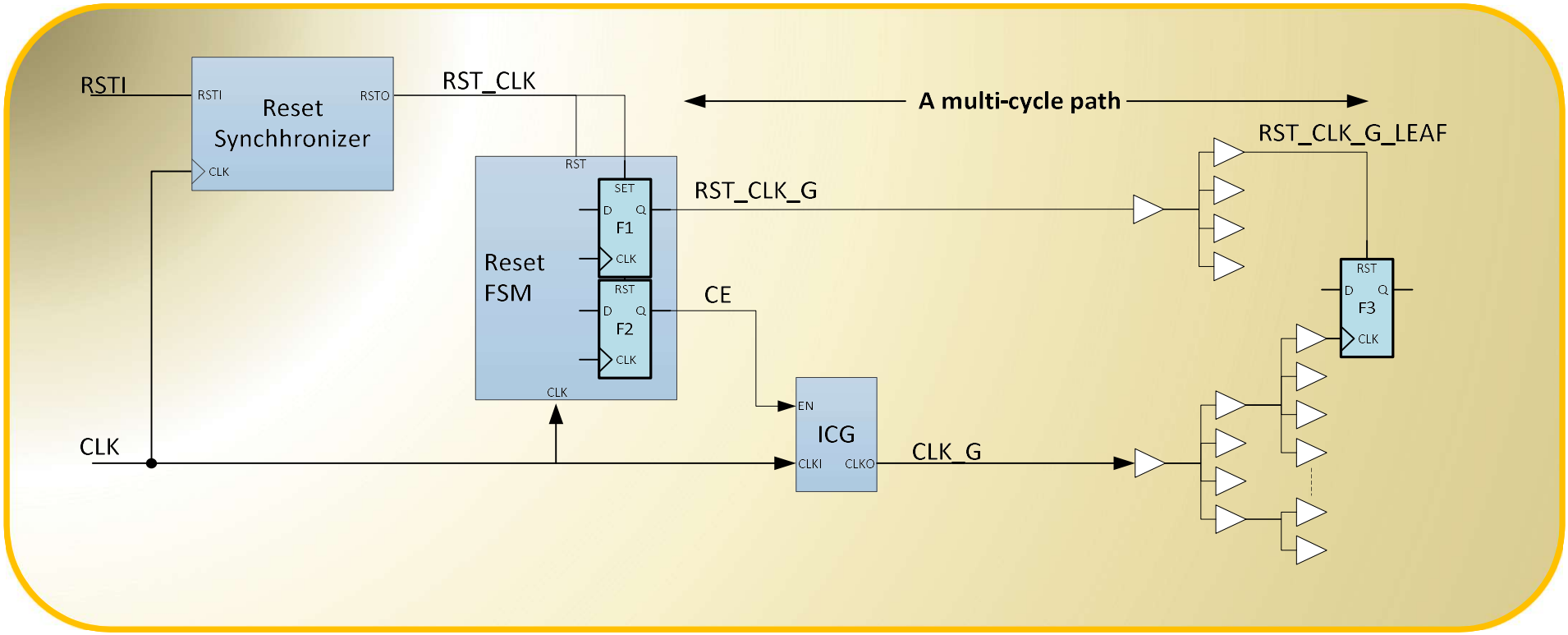
Faster Clocks & Large Designs

T_R gets smaller

Reuven Dobkin,FPGA Kongress, Munich, 2018

REF: R. Dobkin, Asynchronous Reset Synchronization and Distribution, embedded.com, 2017

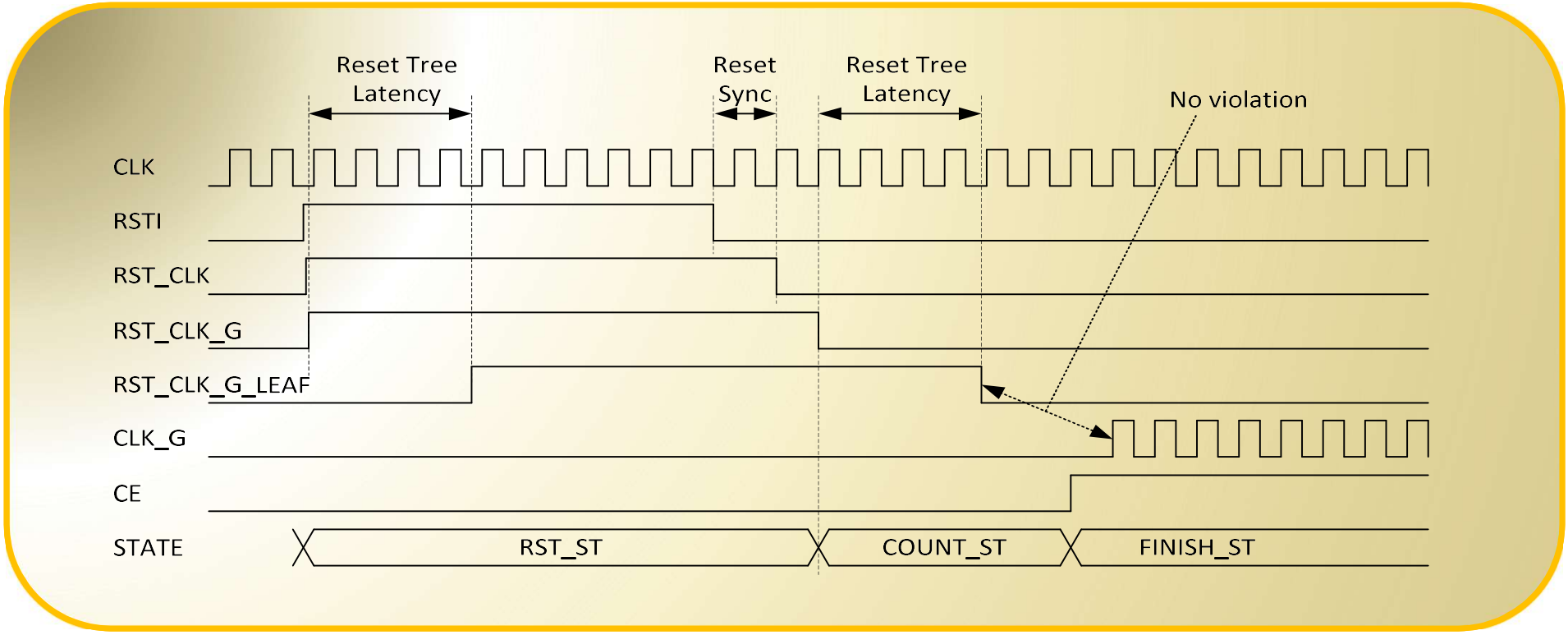
An elegant solution: (1)
The *Clock-Gated* Async Reset Synchronizer



Reuven Dobkin,FPGA Kongress, Munich, 2018

REF: R. Dobkin, Asynchronous Reset Synchronization and Distribution, embedded.com, 2017

An elegant solution: (2)
The *Clock-Gated* Async Reset Synchronizer



Reuven Dobkin,FPGA Kongress, Munich, 2018

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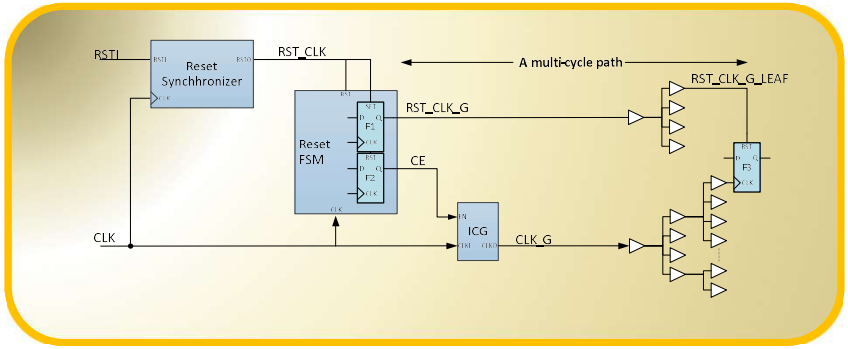

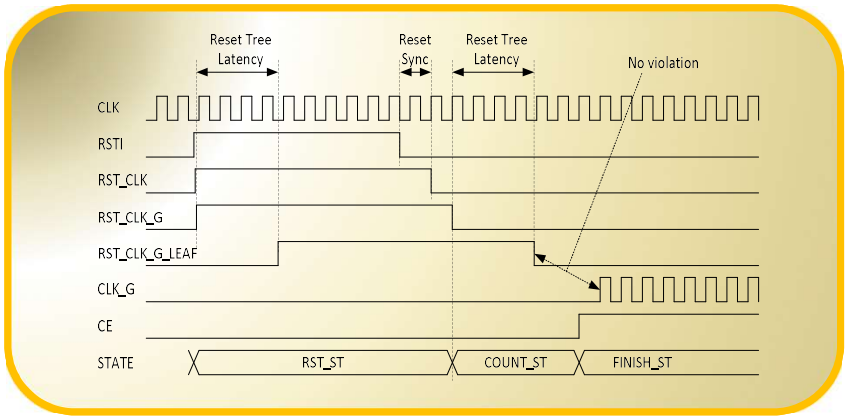

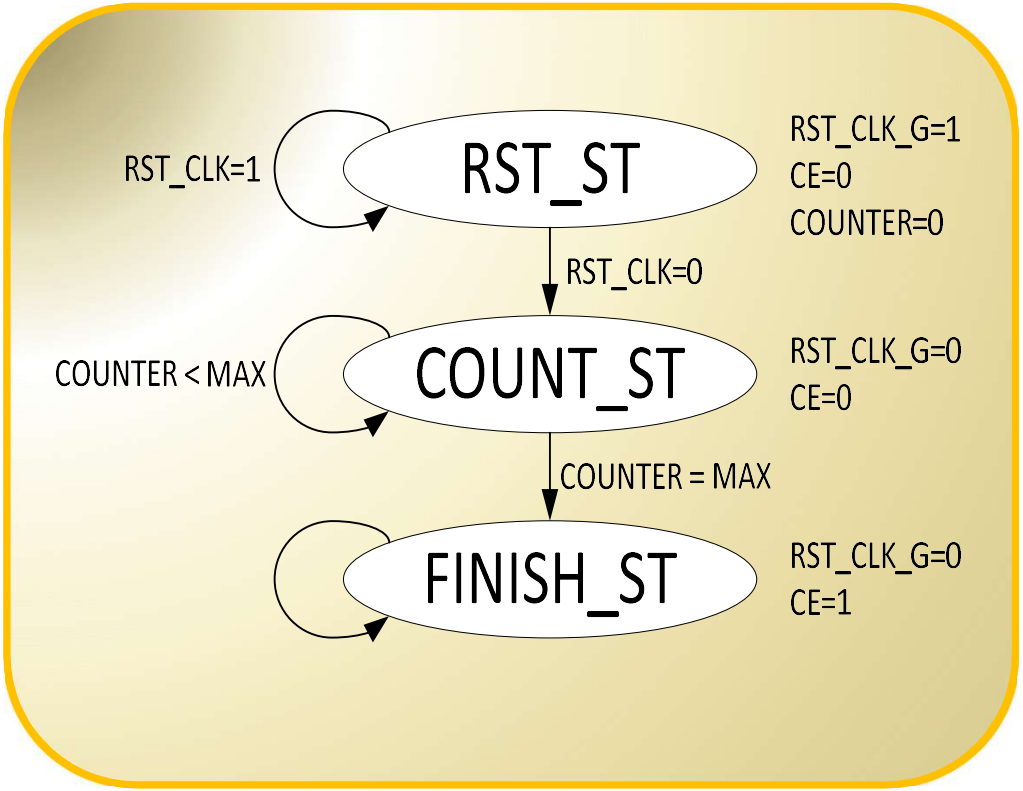

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REF: R. Dobkin, Asynchronous Reset Synchronization and Distribution, embedded.com, 2017

Another Good Approach:
Power Up Initialization in FPGA

- **FPGA allows programming memory default state on power up**
- **Benefits:**
  - A **significant** reduction of FPGA global resources utilization
  - Elimination of the related timing issues of the asynchronous reset removal
- **Not applicable when:**
  - Reset is functional during application run
  - Reset value depends on external value
- **Technically done by replacing asynchronous resets with signal defaults:**
  - VHDL: *signal my_signal : std_logic := '0';*
  - Verilog: *reg my_reg = 1'b0;*
- ***Not* applicable for ASIC**

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Multiple Clock Design *Challenges*

VSYNC circuits

- **Setup: clock & reset requirements …**
- Complexity: design & verification
- Integration: (black-box) Third-party IPs

Getting Requirements … G.I.G.O.

- **Clock setup**
  - Clock relationships
  - Clock sources
    - Async, meso, periodic etc…
    - Intra Black-box clock manipulations
  - Clock switching

- **Reset setup**
  - Reset sequences
  - Power up / @ run

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Clock Scheme Impacts

- **Synchronization solution choice**
- **CDC verification setup**
  - Static
  - Dynamic
- **Reliability verification (MTBF)**
  - E.g. correlated / uncorrelated clocks
- **Constraints generation for CDC**
  - Sync types
  - Quasi-static CDC

Class	$\Delta\phi$	Δf	Synchronizer
Synchronous	0	0	None
Mesochronous	ϕ_c	0	Phase compensation
Multi-synchronous	drifts	0	Adaptive phase compensation
Plesiochronous	Varies	$f_d<\varepsilon$	Adaptive phase compensation
Periodic		$f_d>\varepsilon$	Predictive
Asynchronous			Two-Flop

REF: S. Beer, R. Ginosar, R. Dobkin and Y. Weizman, MTBF Estimation in Coherent Clock Domains, ASYNC'19, 2013.
REF: U.S. Patent 8631364, 2014

Clock & Reset Requirements

- **Challenges**
- **Clock setup**
  - Clock relationships
  - Clock sources
    - Async, meso, periodic etc…
    - Intra Black-box clock manipulations
  - Clock switching
- **Reset setup**
  - Reset sequences
  - Power up / @ run
- **Solutions (EDA)**
- **Auto Clock and Reset setup**
  - Clock & Reset trees auto recognition
  - Vendor-IP recognition (e.g. PLLs, MGT)
  - SDC
  - Call for user intervention when needed
- **Multi-modal analysis support**
  - Clock-gating / switching

Multiple Clock Design *Challenges*

VSYNC circuits

- Setup: clock & reset requirements …
- **Complexity: design & verification**
- Integration: (black-box) Third-party IPs

Complexity … *Key issues*

- **Large designs**
  - Long runtimes
- **Many clocks**
  - Multiple clock relations, large results set
- **Many CDCs**
  - A need to design multiple synchronizers
  - Multiple Quasi-Static CDCs
- **Many third-party IPs**
  - False alarms, undiscovered CDC issues
- **Many operation modes**
  - Long runtimes, enormously large results set

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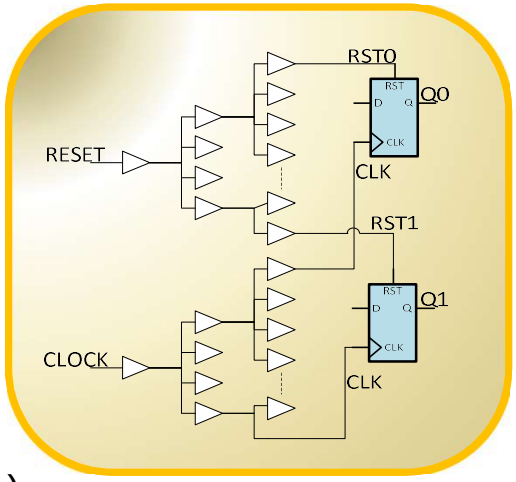
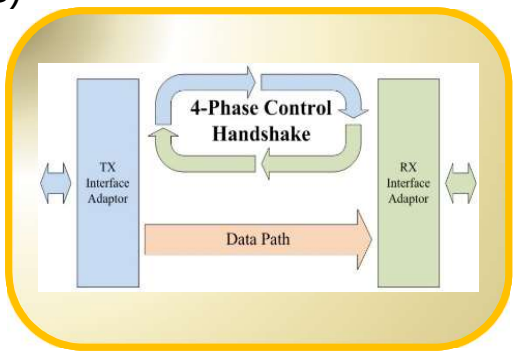
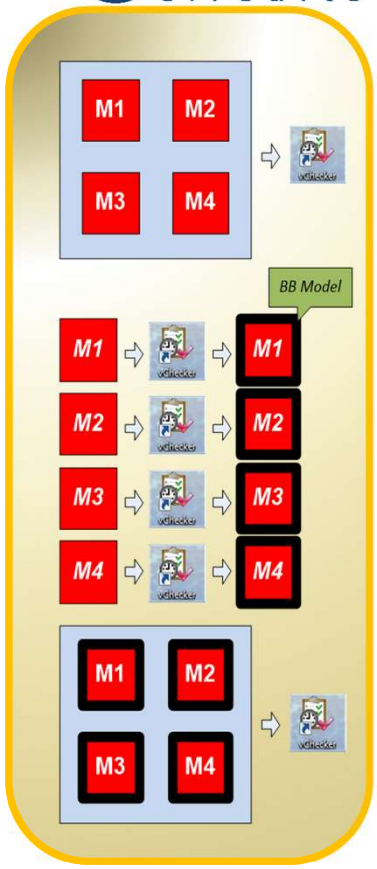
Complexity … *Solutions*

- **Large designs**
  - Parallel exploration, hierarchical analysis
- **Many clocks**
  - Automatic-clock recognition, SDC analysis
- **Many CDCs**
  - Pre-verified synchronizers (incl. Quasi-Static)
  - Verification support (m/s modeling + coverage)
- **Many third-party IPs**
  - Modeling and auto-recognition of the IPs*
- **Many operation modes**
  - Shared user data-base for the multiple modes







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*REF: U.S. Patent 8661383, 2014

Multiple Clock Design *Challenges*

- Setup: clock & reset requirements …
- Complexity: design & verification
- **Integration: (black-box) Third-party IPs**

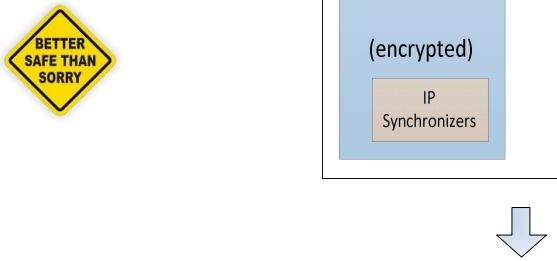
(Black-box) Third-party IPs … Key issues

- **Third-party IP modules**
  - Open-source
  - Encrypted

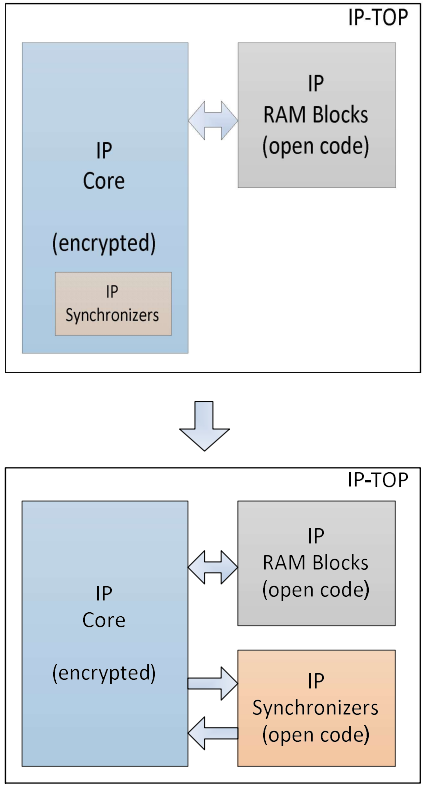
- **May have internal synchronization schemes**
  - May have internal synchronization bugs …
  - May cause CDC bugs, when incorrectly connected
    - Single / Multi-instance connections

Third-party IP integration

- **Open-code IPs:**
  - Hard to dig in someone else's code
  - Thus, it is usually worthwhile to abstract out up Gray/Silver BB*
  - CDC report shall be jointly reviewed with the vendor
    - …



- **Vendor IPs with internal synchronizers:**
  - Ask IP vendor to extract all CDCs to a separate, open code hierarchy
  - Analyze / review this open-code with CDC verification tools
    - Static & Dynamic
  - Communicate with IP vendor on possible issues and waivers



Reuven Dobkin,FPGA Kongress, Munich, 2018

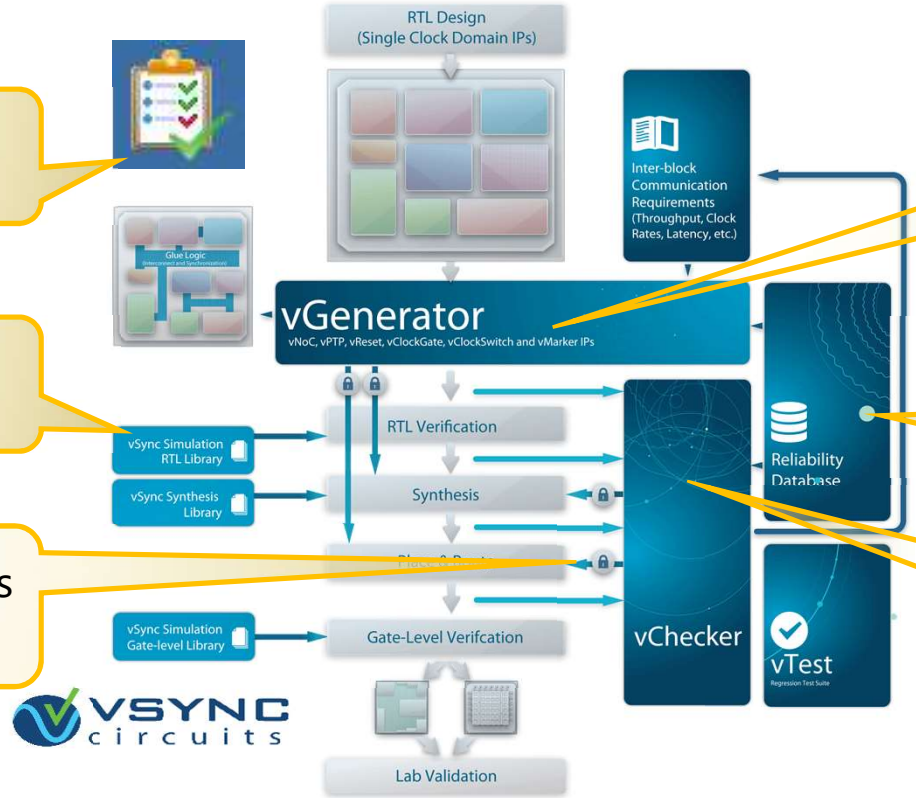
*REF: U.S. Patent 8661383, 2014

vSync Vincent CDC platform for both Design & Verification

LINT
RTL Analysis

Dynamic CDC Verification

Automatic Constraints Generation



Synchronizer Generator

MTBF Computation

CDC Static Analysis and auto-fix

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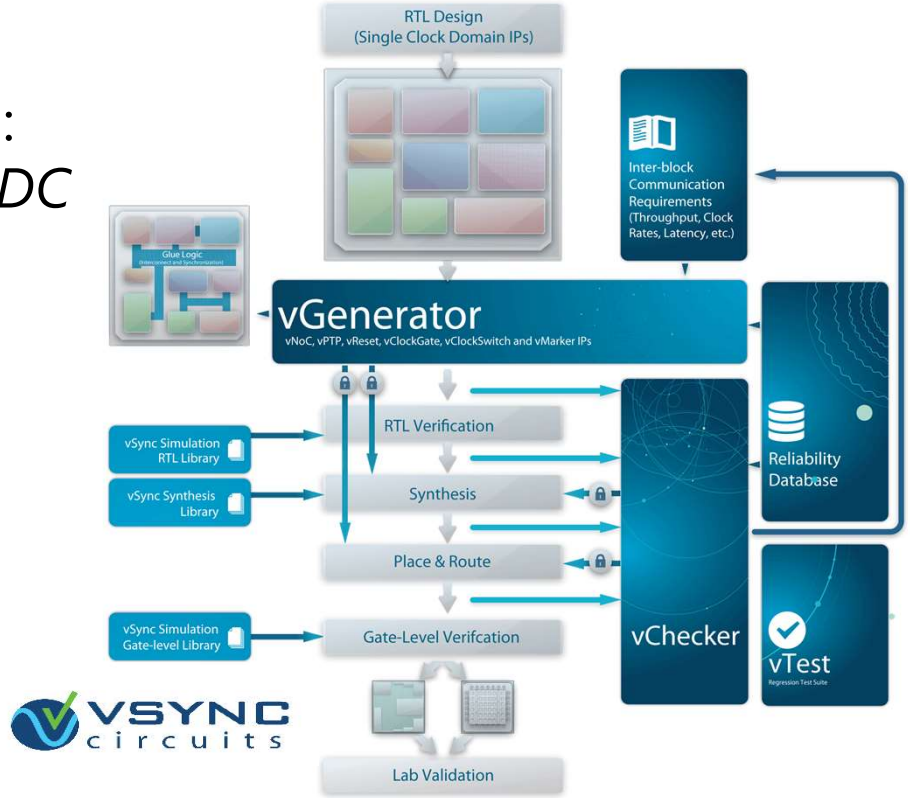
*vSync **Vincent** CDC platform*

- **Visit our booth #14 for more information and demo on …**

vSync ***Vincent*** Platform:
A Complete Solution for CDC

www.vSyncc.com

Thank you!



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Training Program

▶ Essentials of FPGA Design	*1 day*
▶ Designing for Performance	*2 days*
▶ Advanced FPGA Implementation	*2 days*
▶ Design Techniques for Lower Cost	*1 day*
▶ Designing with Spartan-6 and Virtex-6 Family	*3 days*
▶ Essential Design with the PlanAhead Analysis Tool	*1 day*
▶ Advanced Design with the PlanAhead Analysis Tool	*2 days*
▶ Xilinx Partial Reconfiguration Tools and Techniques	*2 days*
▶ Designing with the 7 Series Families	*2 days*

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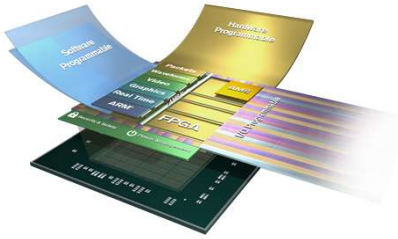

Training Program

- Designing FPGAs Using the Vivado Design Suite 1 — *2 days*
- Designing FPGAs Using the Vivado Design Suite 2 — *2 days*
- Designing FPGAs Using the Vivado Design Suite 3 — *2 days*
- Designing FPGAs Using the Vivado Design Suite 4 — *2 days*
- Designing with the UltraScale and UltraScale+ Architecture — *2 days*
- Vivado Design Suite for ISE Software Project Navigator User — *1 day*
- Vivado Design Suite Advanced XDC and Static Timing Analysis for ISE Software User — *2 days*

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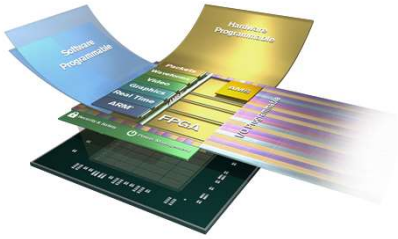

Training Program

▶ Designing with Multi Gigabit Serial IO	*3 days*
▶ High Level Synthesis with Vivado	*2 days*
▶ C-Based HLS Coding for Hardware Designers	*1 day*
▶ C-Based HLS Coding for Software Designers	*1 day*
▶ DSP Design Using System Generator	*2 days*
▶ Essential DSP Implementation Techniques for Xilinx FPGAs	*2 days*

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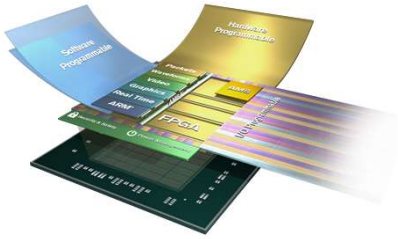

Training Program

▶ Embedded Systems Design	*2 days*
▶ Embedded Systems Software Design	*2 days*
▶ Advanced Features and Techniques of SDK	*2 days*
▶ Advanced Features and Techniques of EDK	*2 days*
▶ Zynq All Programmable SoC Systems Architecture	*2 days*
▶ Zynq UltraScale+ MPSoC for the System Architect	*2 days*
▶ Introduction to the SDSoC Development Environment	*1 day*
▶ Advanced SDSoC Development Environment & Methodology	*2 days*

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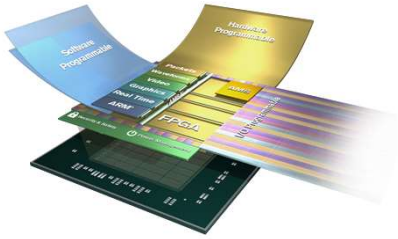

Training Program

▶ VHDL for Designers	*3 days*
▶ Advanced VHDL	*2 days*
▶ Comprehensive VHDL	*5 days*
▶ Expert VHDL Verification	*3 days*
▶ Expert VHDL Design	*2 days*
▶ Expert VHDL	*5 days*
▶ Essential Digital Design Techniques	*2 days*
▶ Developing with Embedded Linux	*2 days*
▶ Essential Phython	*2 days*

DOULOS Delivering KnowHow

Training Program

- Solving Clock Domain Crossover Conflicts *2 days*