CAD to CAM – optimum PCB design flow

- First Think
- Then Act
- Achieve: "Right First Time"
 - In time
 - On Budget
- Dirk Stans, Eurocircuits

DESIGN AUTOMATION & EMBEDDED SYSTEMS TYPESTER TO DER VALLE HOTEL, EINDHOVEN

7 NOV 🔶 **TECHNOPOLIS, MECHELEN** 8 NOV (



PCB Design Flow

- Defining your BOM (Bill Of Material)
- Create Schematics
- Size the PCB and Place Key Components
- Make the PCB Layout
- Export data from CAD for manufacturing

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Defining your BOM (Bill Of Material)

Designer

- Functionality of components.
- Package to use ? Footprint definition.
- Testing implications ?
- Heat Management ?
- Etc....

Manufacturer

- Availability of components
- Pricing ?
- Effect on manufacturability and cost.
- Feasibility and cost
- Reliability
- Etc. ...

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Defining your BOM (Bill Of Material)

Designer

• Search the web and choose on specification and taste

Manufacturer

- Use a proven and tested own data base of components
 - Manufacturable
 - reliable
 - available

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Defining your BOM (Bill Of Material)

- Perform an early check of your BOM with your manufacturer
- Or...
- Build your BOM by selecting components out of your Manufacturers data base (BOM-generator on the eC-Verified DB)

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Size the PCB and Place Key Components

Designer

- Size the PCB according to design requirements or taste
- Place the Key Components

Manufacturer

- How does it fit on a PCB production panel? Cost?
- Effect on manufacturability (solderability)

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Defining your Printed Circuit Board

- What are the PCB cost drivers ?
- What makes a PCB hard/impossible to make ?
- Which tools are available to help me ?
 - Offline direct consulting Quotation All
 - Online capability catalogues All
 - Online smart menus Eurocircuits

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Determine PCB parameters

- Material (spec cost poolable)
- Buildup (poolable or not)
- Copper thicknesses
- DRC values (TW, TT, TP, PP, OAR, IAR)
- PCB/Panel size <-> Production panel filling
- •
- Non Gerber parameters
- => save all for later references and check
- => use DRC values in your CAD system for the layout

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STANDARD pool							Summary	B	usiness customer?	Select here. 📃
			Delivery format	Single PCB		-	Service		STANDA	RD pool
(ER.)	1 months		PCB quantity	10			Delivery term		7 worki	
	A STATE SPACE				-	_	Estimated shipment date		01-10	
			Delivery term	7 working da	ys	-	Quantity		10 P	
			Number of layers	6		-	Board surface / Order surface Prices		0.80 dm ²	
			PCB width (X) (mm)	100.00			Single PCB		€ 31.79	Gross* € 38.47
			PCB height (Y) (mm)	80.00			Total boards		€ 317.92	€ 384.68
			eC-registration compatible PCB				 Express transport Economy transport 		€ 12.48 € 10.49	€ 15.10 € 12.69
▶ Stencils						1	Total		€ 330.39	€ 399.77
				1 and the second			* The gross prices include 21.00% VAT.			
Material definition				Select	t pre-defined b	ouildup		₩ Add to bas	sket	
Board thickness	1.55 mm		Board buildup	Standard		•	Useful documents			
Material Tg	145-150 °C						→ PCB C	alculator user quide		Read more
Outer layer copper foil	18 µm (end 35 µm)		Inner layer copper foil	35 µm		•	→ PCB d	esiqn quidelines		Read more
Extra PTH runs	0		Extra press cycles	0			Alternatives	oolgii guluoliiloo	0.1	
▼ Board technology				1	Select classif	ication		-		stomized matrix
Outer layer trackwidth			Outer layer isolation distance				10 PCBs 7 working days	20 PCBs 7 working days		30 PCBs orking days
(OL-TW)	0.150 mm		(OL-TT-TP-PP)	0.150 mm		•	Net Gross* € 31,79 € 38,47	Net Gro € 21.17 € 25	States and the second second	Gross* € 20.58
Outer layer annular ring (OAR)	0.125 mm		Inner layer trackwidth (IL-TW)	0.150 mm		•	€ 317.92 € 384.68	€ 21.17 € 25		
Inner layer isolation distance (IL-TT-TP-PP)	0.150 mm		Inner layer annular ring (IAR)	0.125 mm		•	Select	Select		Select
Smallest final hole	0.25 mm	-	Hole density	< 1000/dm²		•	10 PCBs	20 PCBs		30 PCBs
Technology class	6C		Holes <= may be reduced	0.45 mm		•	6 working days Net Gross*	6 working days		orking days Gross*
Board definition							€ 39.90 € 48.28 € 399.02 € 482.81	€ 26.58 € 32 € 531.53 € 64	.16 € 21.34	€ 25.82
Top soldermask	Green	•	Bottom soldermask	Green		•	Select	Select		Select
Top legend	White	•	Bottom legend	White		•	* The gross prices include 21.00% VAT.			
Surface finish	Any lead free finish	•	Milling	No		-	The transport costs and total price are o	alculated and shown in the s	ummary according to the	selection.
Bare Board Testing	V		UL marking							
► Advanced options							Î			

Smart menu

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Make your board layout according

- Optimum Component packages placed at the right spot
- Optimum PCB size
- Optimum number of layers
- Optimum DRC values

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PCB - details	Possible issues		Clearly	defined in:	PCB Visualizer
		Gerber X	Gerber X2	Native EAGLE/KiCAD	defines
Base material	On stock / on offer	no	no	no	PCB Configurator
Number of layers	Layers complete or not	no	no	yes	Buildup editor
Definition of the layers	Clear definition / assignment	no	yes	yes	Buildup editor
Board size	Possible open or more contours	no	no	no	Outline editor
Customer panel	Definition not standardized	no	no	no	Panel editor
Copper thickness	Definition base/end Cu	no	no	no/yes	Buildup editor
build up	Definition not standardized	no	no	no/yes	Buildup editor
РТН		no	yes	yes	Drill Editor
Via / component hole		no	yes	yes	Drill Editor
NPTH		no	yes	yes	Drill Editor
Slots & Cut outs	Definition not standardized	no	yes	yes	Outline editor / Drill editor
blind & burried vias	Define the layer name correct	no/yes	yes	yes	Buildup editor
Thermal pads	Defined in CAD or not	no	no/yes	no/yes	-
Surface finish		no	no	no	PCB Configurator
Soldermask colour		no	no	no	PCB Configurator
Legend colour		no	no	no	PCB Configurator
press fit holes	Definition not standardized	no	no	no	PCB Configurator parameter
peelable mask	Definition not standardized	no	no	no	Buildup editor
Carbon contacts	Definition not standardized	no	no	no	Buildup editor
edge connector / beveling	Definition not standardized	no	no	no	PCB Configurator parameter
depth routing	Definition not standardized	no	no	no	PCB Configurator / Drill editor
via-fill	Definition not standardized	no	no	no	PCB Configurator / Drill editor
chamfered holes	Definition not standardized	no	no	no	PCB Configurator / Drill editor
PTH on the board edge	Definition not standardized	no	no	no	PCB Configurator parameter
round-edge plating	Definition not standardized	no	no	no	PCB Configurator parameter
heatsink paste	Definition not standardized	no	no	no	Buildup editor

PCB data CAD

(Computer Aided Design)

to CAM

(Computer Aided Manufacturing)



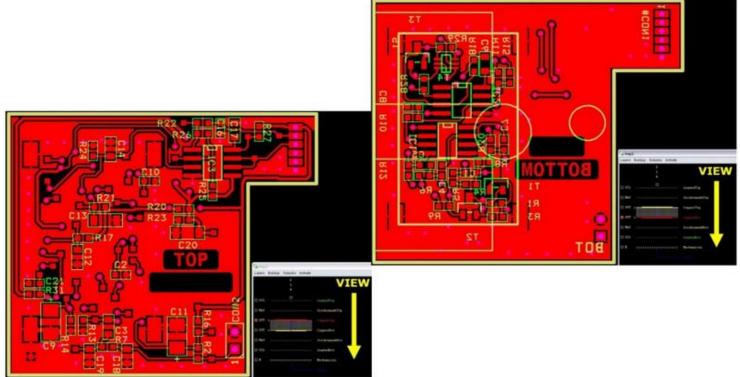
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MBEDDED DESIGN CHALLENGES

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All layers ALWAYS viewed from the TOP

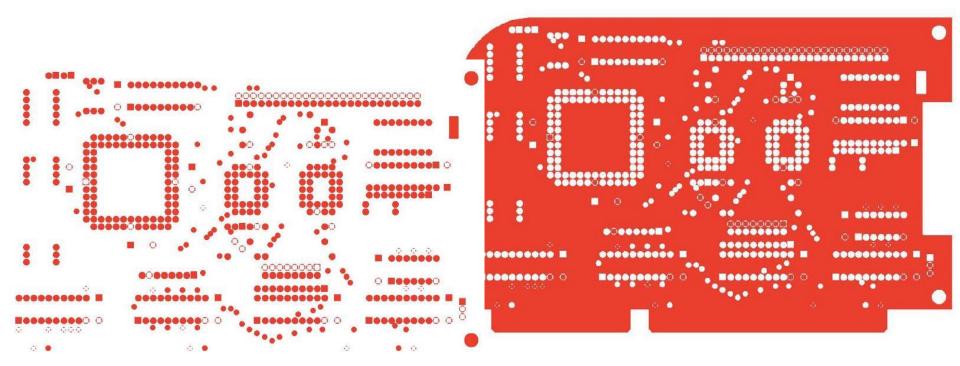


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Layer polarity matters

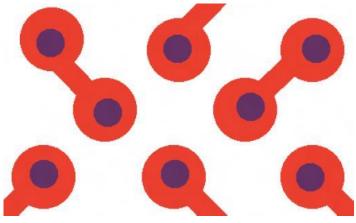


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Drills versus copper pads



Different Unit -Resolution

Non Centered

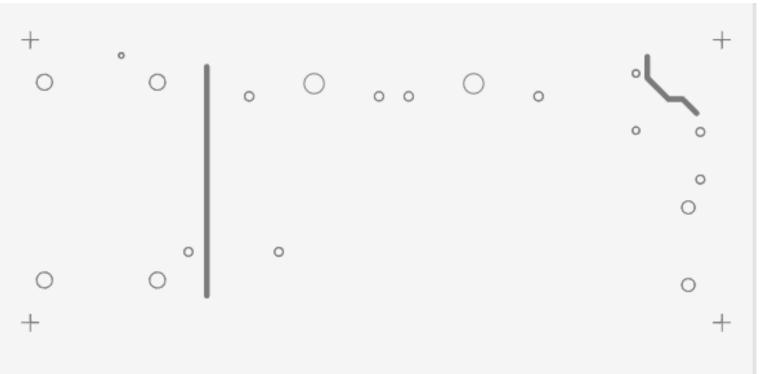
Same Unit -Resolution

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Bad outline

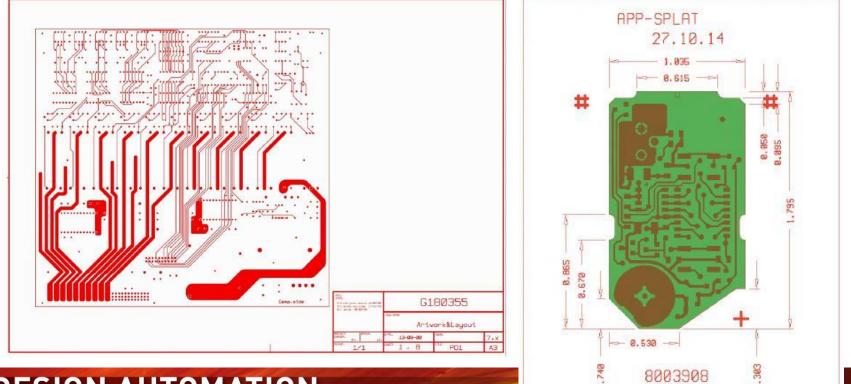


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Data outside the PCB contour



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Buildup selector -	(STANDARDpool)				
Material					Buildup
Number of layers	4 v	Board thickness	1.55 mm	•	Total material thickness: 1.536 mm
Reversed buildup		Blind/Buried via runs	1	÷ 🤪	Top legend
Extra press cycles	1	Special buildup			Top soldermask
Top soldermask	Green 🔻	Bottom solderma	sk Green	v	Top copper Prepreg - PR7628 - 0.18mm
Top legend	White v	Bottom legend	None	•	Prepreg - PR7628 - 0.18mm
Peelable mask	No Y	Carbon contacts	No	•	Inner copper 1
Viafill	No v	Top heatsink past	No	•	
Bottom heatsink paste	No v				Core - FR4-Improved - 0.71mm
Core thickness	Outer layer copp	oer foil	Inner layer copper		
0.710 mm	12 µm ((end 30 µm)	12 µm	9	Inner copper 2
0.710 mm	12 µm ((end 30 µm)	18 µm		Prepreg - PR7628 - 0.18mm
0.710 mm	18 µm ((end 35 µm)	18 µm	9	
0.710 mm	18 µm ((end 35 µm)	35 µm		Prepreg - PR7628 - 0.18mm
0.710 mm	35 µm ((end 60 µm)	35 µm	9	Bottom copper Bottom soldermask
0.710 mm	35 µm ((end 60 µm)	70 µm	9	Plated drill
0.710 mm	70 µm ((end 95 µm)	70 µm	9	Non Plated Through Hole (NPTH)
0.360 mm	12 µm ((end 30 µm)	12 µm	9	Blind/buried via (Top - Inner 1)
0.360 mm	12 µm ((end 30 µm)	18 µm	9	bind/bunca via (rop Timer 1)
0.360 mm	18 µm ((end 35 µm)	18 µm	9	
0.360 mm	18 µm ((end 35 µm)	35 µm	9	
0.360 mm	35 µm ((end 60 µm)	35 µm	9	
0.360 mm	35 µm ((end 60 µm)	70 µm	9	
0.360 mm	70 µm ((end 95 µm)	70 µm	9	
0.200 mm	12 µm ((end 30 µm)	12 µm	9	
0.200 mm	12 µm ((end 30 µm)	18 µm	9	
0.200 mm	18 µm ((end 35 µm)	18 µm	9	
0.200 mm	18 µm ((end 35 µm)	35 µm	9	
0.200 mm	35 µm ((end 60 µm)	35 µm	9	
0.200 mm	35 µm ((end 60 µm)	70 µm	9	
0.200 mm	70 µm ((end 95 µm)	70 µm	9	Remarks
0.100 mm	12 µm ((end 30 µm)	12 µm	9	Blind/buried via (Top - Inner 1) ends at the top side of a
0.100 mm	12 µm ((end 30 µm)	18 µm	9	core. Select the via in the buildup and use the buttons in t
0.100 mm	18 µm ((end 35 µm)	18 µm	9	toolbar to correct the drill span or choose a different boar buildup.
0.100 mm	18 um ((end 35 um)	35 um	<u>e</u>	bundup.
			Cance	І Арр	Py G Click here for more information

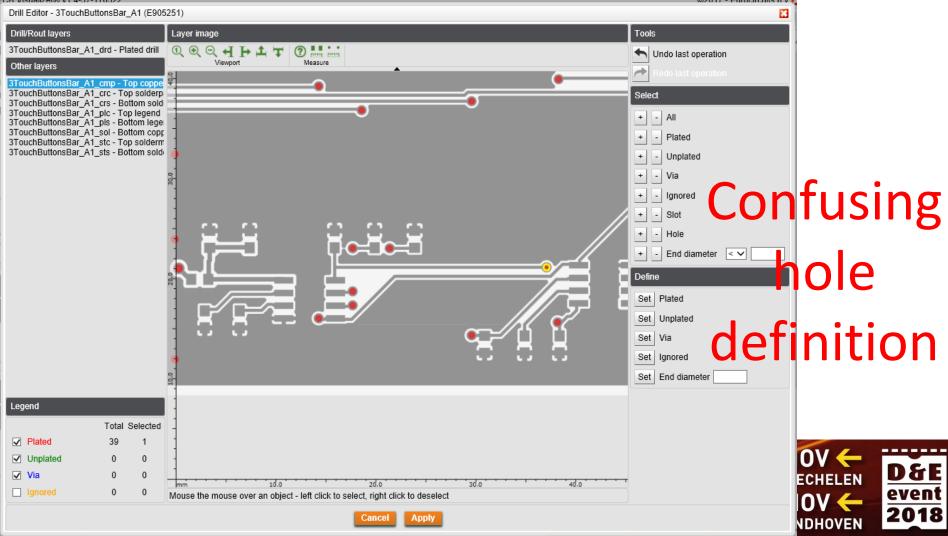
Bad buildup edited with buildup editor

892 combinations possible

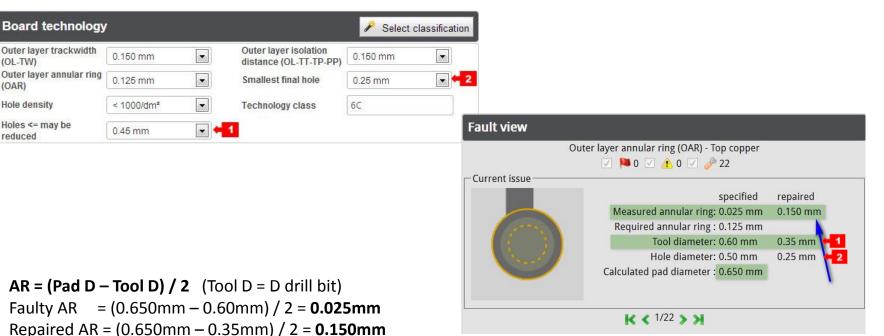


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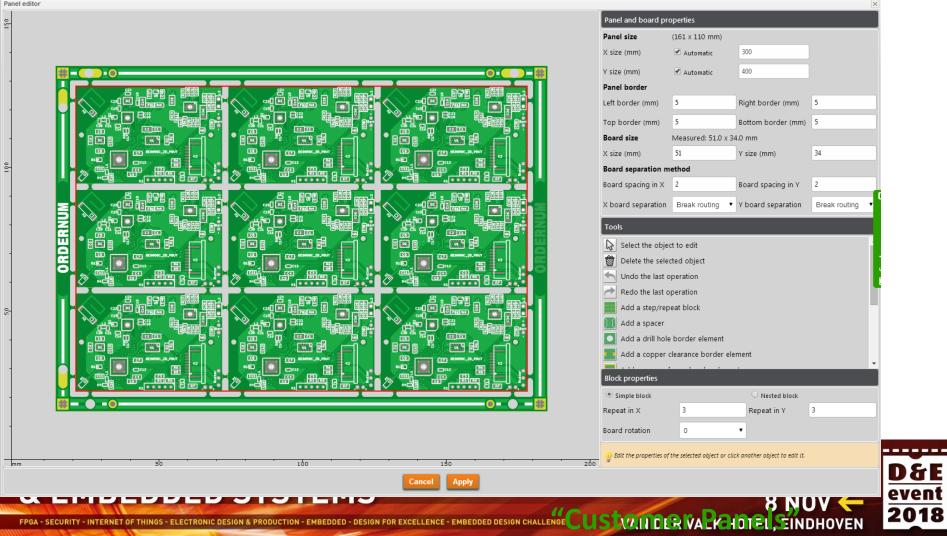
Auto repair annular ring issues



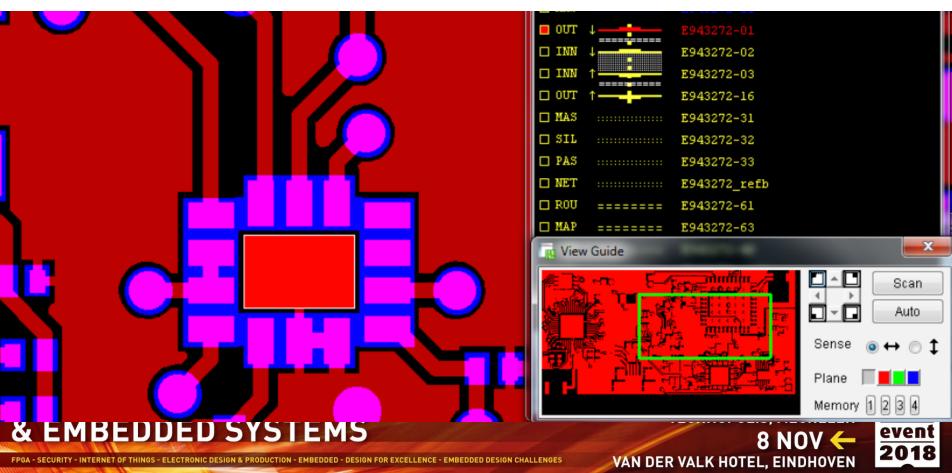
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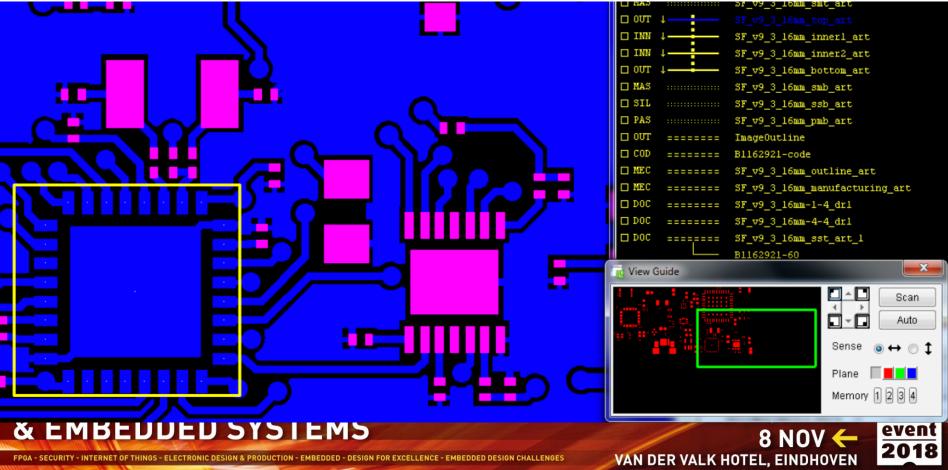




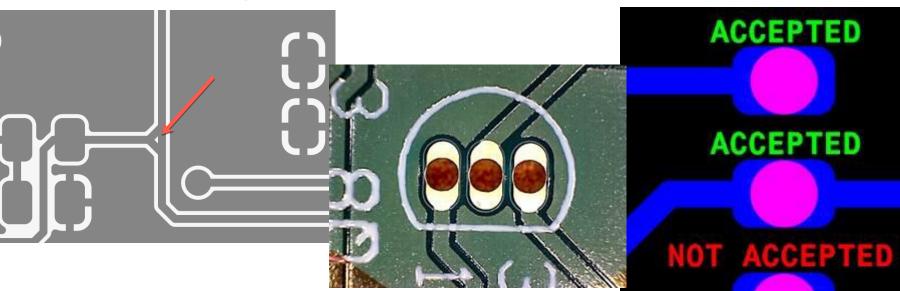
Soldermask issues



Solder paste issues



PCB production issues



NPTH : 0.15mm on toolsize (0.15mm on endsize) PTH - Same net : 0.15mm on toolsize (0.25mm on endsize) PTH - Diff net : 0.25mm on toolsize (0.35mm on endsize)

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Design For Manufacturing

- At your supplier
 - Operator
 - Offline CAM system
- Online tools
 - -?
 - eC Smart Tools PCB Visualizer

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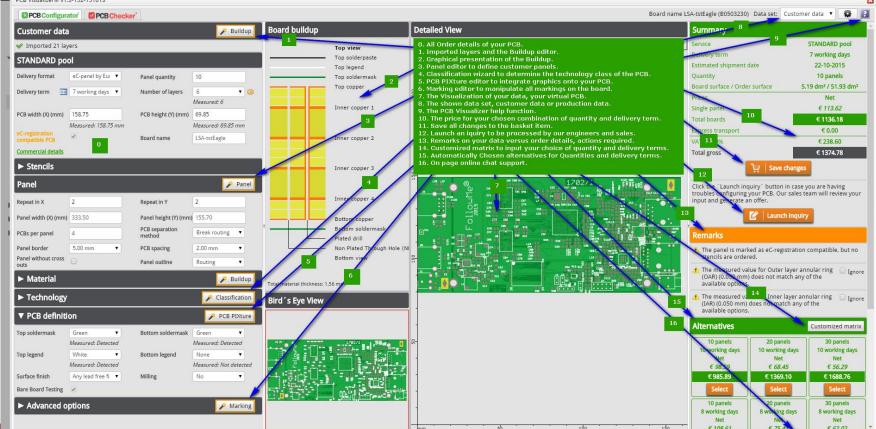
PCB Visualizer® v1.3-152-151013

8

C PCB Configurator		Board name LSA-tstEagle (B0503230) Data set: Customer data	• 😫 🛃
DRC - DFM information	Plating	Summary	
DRC information DFM information	Top plating index 0.8 0. PCB Checker - DFM information	Service STANDA	
Layer Values	1. Plating index	Delivery term 7 workin	
Plating	2. Detailed info on the plating index of the chosen layer 3. Image of the plating index of the chosen layer	Estimated shipment date 22-10- Quantity 10 P	
Top copper 0.80	4. Calculated solder paste surface (SMD)	Board surface / Order surface 1.11 dm² /	
Bottom copper 0.71	5. Potential fiducials 6. % Copper, free of soldermask against the board surface	Prices Ne	
Solderpaste surface	7. On page online chat support	Single PCB € 42	
Top solderpaste 1335.75 mm ²		Total boards € 42	
Not-connected soldermask-free pads - Potential fiducials		Express transport € 0.	
Top copper 16		VAT 21.00% € 88	3.77
Bottom copper 0	1702/1	Total gross €51	0.02
Copper free of soldermask		Save changes	
Top copper 14.80%		Click the 'Launch inquiry' button in case you are h	aving
Bottom copper 3.04%		troubles configuring your PCB. Our sales team will r input and generate an offer.	review your
		input and generate an oner.	
		Launch inquiry	
		Remarks	
		The measured value for Outer layer annular ring (OAR) (0.050 mm) does not match any of the	g 🗌 Ignore
		available options.	
Fault view		A The measured value for Inner layer annular ring	
		(IAR) (0.050 mm) does not match any of the available options.	signore
Plating - Top copper		avanable options.	_
		Alternatives Custom	nized matrix
Current issue		10 PCBs 20 PCBs 3	0 PCBs
Plating index : 0.80		7 working days 7 working days 7 wo	rking days
		Net Net € 42.2x € 27.92 €	Net 22.87
			686.09
			Select
The plating index measures the uniformity of copper density on the board. A completely	v		
uniform board has an index of 1 which means that no plating problems are expected.			0 PCBs
Lower values show less uniformity, highlighted on the visual image by the red and blue areas. If the index falls to 0.4 or less, then special attention is required.		6 working days 6 work	rking days Net
More information can be found here.		€ 52.95 € 34.97 €	28.65
			859.58
	Underplating Normal plating	Overplating Salact Salact	Folget
5- EUROCIRCUITS N.V. Privacy Policy Terms of Sales Contact us		 Contact s 	support
		8 NUV 🧲 🗜	010
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	VAN	JER VAER HOTEL, EINDHOVEN	_

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PCB Visualizer® v1.3-152-151013



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PCBAssembly data - CAD to CAM

PCBA - details	Possible issues		Clearly defined in:		PCBA Visualizer
		вом	CPL	Native EAGLE/KiCAD	defines
File format	Definition not standardized	no	no	yes	BOM editor / CPL editor
Component description	Definition not standardized	no	no	no	BOM editor
Manufacturing Part Number	Not clear or partial description	no	no	no	BOM editor
Supplier Part Number	Not clear or partial description	no	no	no	BOM editor
Component package	Poor definition leads to different package link in manufacturing DB	no	no	no	BOM editor
Component origin (Offset)	Different origin than manufacturing DB	no	no	no	CPL editor
Component Rotation (pin 1)	Different rotation than manufacturing DB	no	no	no	CPL editor
Component centroid	Different centroid than manufacturing DB	no	no	no	CPL editor
Component footprint	Poor definition leads to different footprint link in manufacturing DB	no	no	no	-
IPC definition of the footprint	Almost never available	no	no	no	show
Component Packaging	Need to be decided by the manufacturer	no	no	no	removed in BOM editor

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	A B	с	D	E	F
				R6, R7, R8, R9, R10, R11,	
10 9	10k	R_0603	0603_TYPE_B	R12, R25, R26	Bill Of Material - Jibberish
				C45, C46, C47, C48, C49,	
11 6	10n	C_0603	0603_TYPE_B	C50	
12 1	10u	C_0805	0805_TYPE_A	C34	
13 1	15EDGRC-3.5/6P			CN6	
14 2	18p	C_0603	0603_TYPE_B	C56, C57	Qty Value Device Package Parts Description
15 1	1k	R_0603	0603_TYPE_B	R13	1 JP_1X14 JP_1X14 CN1
16 1	1u	CPOL-EUSMCA	SMC A	C31	POLARI 1 JP_1X4 JP_1X4 CN5
16 1 17 2	10	C 0603	0603 TYPE B	C36, C39	Europe 1 JP_1X5 JP_1X5 CN3
1/ 2	10	c_0005	0003_1192_8	C30, C35	1 JP_1X6 JP_1X6 CN4 POLARI 1 JTIMPER SMD ROTIND JP1
18 2	2.2u	CPOL-EUSMCA	SMC A	C25, C28	
19 3	2.2u 20k	R 0603		R16, R19, R22	
20 4	20	R 0603		R2, R3, R4, R14	2 100k R 0603 0603 TYPE B R1, R27
21 1	22uH	L-EUL3225M		L1	40 100n C_0402 0402_TYPE_C C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C1
-1 1		E EGEDEZDIWI	LOLLOW.		
22 4	4.7u	CPOL-EUSMCA	SMC A	C1, C33, C35, C37	
	-174			01,000,000,007	
	40 PIM CON 0.5 MM		CON FFC 40-PIN 0.5MM WURTH-		1 15EDGRC-3.5/6P CONTERMINAL 3.5MM_6-PIN CONTERMINAL 3.5MM_6-PIN CN6
23 1	WURTH	40 PIM CON 0.5 MMWURTH	687140149022	CN2	2 18p C_0603 0603_TYPE_B C56, C57 1 1k R_0603 0603_TYPE_B R13
24 1	5	R 0603		R15	1 1k R_0603 0603_TYPE_B R13 1 1u CPOL-EUSMCA SMC A C31 POLARIZED CAPACITOR, European symbol
25 1	8MHz	CRYSTAL 2PIN		Q1	2 lu C 0603 0603 TYPE B C36, C39
26 1	AP5724WG-7	AP5724		IC4	2 10 CPOL-EUSMCA SMC A C25, C28 POLARIZED CAPACITOR, European symbol
27 1	AS4C4M16S-6BIN	SDRAM 16-BIT	TFBGA-54	IC2	3 20k R 0603 0603 TYPE B R16, R19, R22
28 1	IP4252CZ8-4-TTL,13	EMIF_4CH_IP4252	EMIF_4CH_IP4252	IC7	4 22 R 0603 0603 TYPE B R2, R3, R4, R14
29 2	IRLML2246TRPBF	BSS84	SOT23	T1, T2	P-CHAN 1 22 H L-EUL3225M L3255M L1 INDUCTOR, European symbol
30 1	LD-BZEN-0803	BUZZER_01	BUZZER_01	BZ1	4 4.7u CPOL-EUSMCA SMC A Cl. C33, C35, C37 POLARIZED CAPACITOR, European symbol
31 1	M95512-WMN6P	EEPROM_SPI_SO8	SO08	IC5	1 40 PIM CON 0.5 MMWURTH 40 PIM CON 0.5 MMWURTH CON FFC 40-PIN 0.5MM WURTH-687140149022 CN2
32 3	MAX31856MUD+	MAX31856MUD+	TSSOP14	IC8, IC9, IC10	1 5 FIN_CONTINUE 1 50 FIN_CONTINUE CONTINUE CONTINUE CONTINUE CONTINUES CONT
33 1	MCP130T-300	MCP130	SOT-23-II	IC3	1 8MHz CRYSTAL 2PIN CRYSTAL 3.2MM 2PIN Q1
					200 WT 1 AP5724WG-7 AP5724 SOT73-6 IC4
34 2	PMEG4005AEA.115	SMF5.0AT1	SOD123FL	D2, D3	Suppre 1 AS4C4M165-6BIN SDRAM 16-BIT TFBGA-54 IC2
		DIODE_SUPRESSOR_UNIDRECTION			1 IP4252C28-4-TTL,13 EMIF 4CH IP4252 EMIF 4CH IP4252 IC7
35 1	SMLVT3V3	ALDO-214AA		D1	2 IRLML2246TRPBF BSS84 SOT23 T1, T2 P-CHANNEL MOS FET
36 1	STM32F429NI	STM32F429N		IC1	1 LD-BZEN-0803 BUZZER 01 BUZZER 01 BZ1
37 1	TSC2046	TSC2046		IC11	1 M95512-WMN6P EEPROM SPI SO8 SO08 IC5
38 1	W25Q32FVSSIG		SO08W	IC6	3 MAX31856MUD+ MAX31856MUD+ TSSOP14 IC8, IC9, IC10
٠	Differen	t file formats	lised		1 MCP130T-300 MCP130 SOT-23-II IC3
	Differen		uscu		2 PMEG4005AEA.115 SMF5.0AT1 SOD123FL D2, D3 200 W Transient Voltage Suppressor
			.		1. SMLVT3V3 DIODE SUPRESSOR UNIDRECTIONALDO-214AA DO-214AA D1
٠	BOMIOU	Itput from CA	D system is l	imited - C	TVDLC STM32F429NI STM32F429N TFBGA IC1
		•			1 TSC2046 TSC2046 TSS0P16 IC11
	descrint	ion of compo	nent and na	ckage	1 W25Q32FVSSIG EEPROM SPI SO8SOIC8 WIDE SO08W IC6
	ucscript	lon or compe	nent and pa	Chage	
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DESIGN AUTOMATION & EMBEDDED SYSTEMS

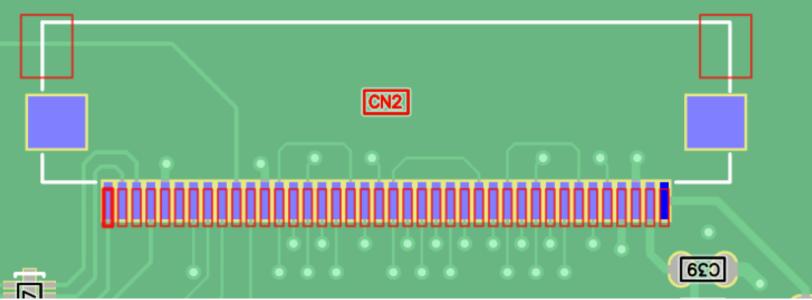
FPGA - SECURITY - INTERNET OF THINGS - ELECTRONIC DESIGN & PRODUCTION - EMBEDDED - DESIGN FOR EXCELLENCE - EMBEDDED DESIGN CHALLENGES

TECHNOPOLIS, MECHELEN 8 NOV ← VAN DER VALK HOTEL, EINDHOVEN

D&E

event

2018

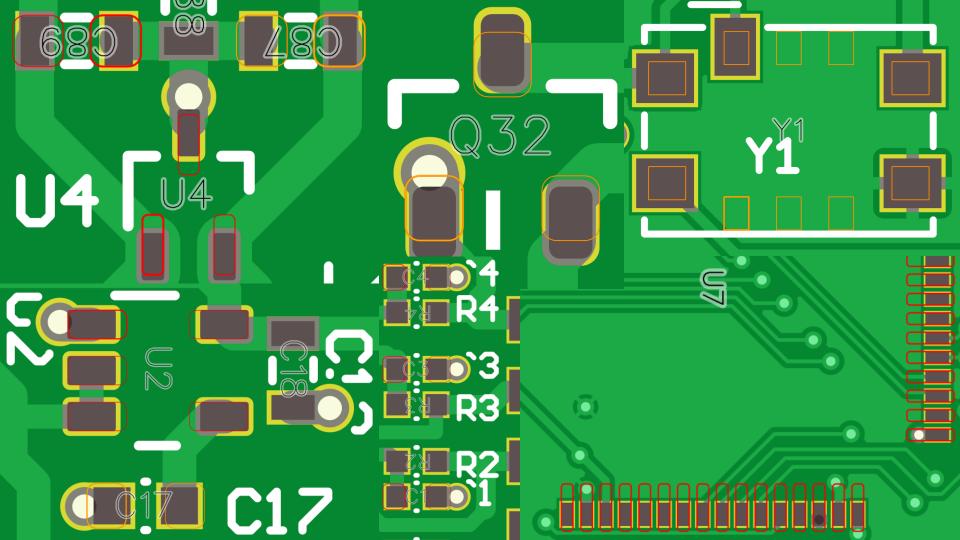


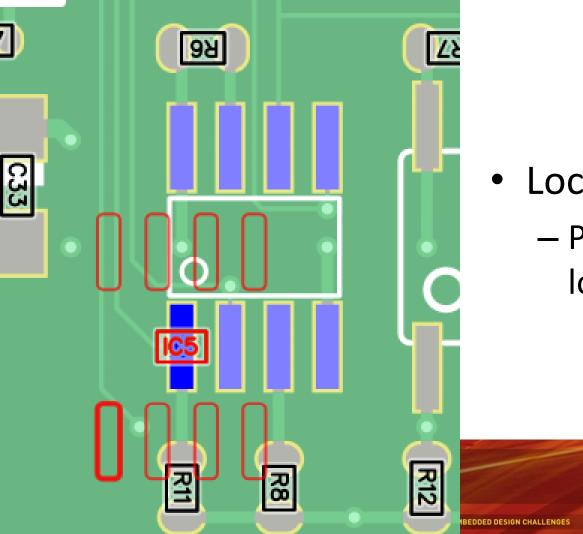
- Footprint check CAD-info against other database
 - Incorrect component chosen. Same device available with different packages
 - Incorrect footprint definition in CAD library

DESIGN AUTOMATION & EMBEDDED SYSTEMS

FPGA - SECURITY - INTERNET OF THINGS - ELECTRONIC DESIGN & PRODUCTION - EMBEDDED - DESIGN FOR EXCELLENCE - EMBEDDED DESIGN CHALLENGES



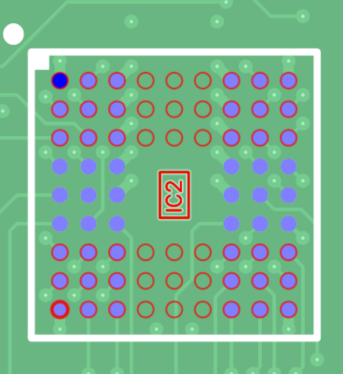


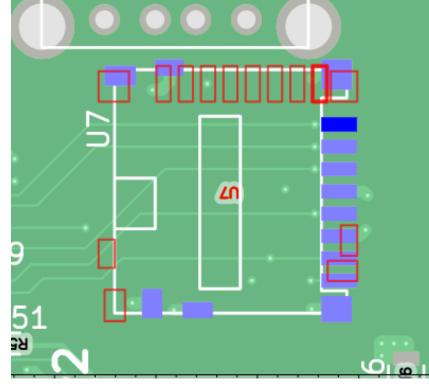


- Location
 - PIN1 vs centroid
 location in CPL file









- Each library can define its own default rotation
- CAD ERP Machine

Rotation

DESIGN AUTOMATION & EMBEDDED SYSTEMS

FPGA - SECURITY - INTERNET OF THINGS - ELECTRONIC DESIGN & PRODUCTION - EMBEDDED - DESIGN FOR EXCELLENCE - EMBEDDED DESIGN CHALLENGES



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Q9

FPGA - SECURITY - INTERNET OF THINGS - ELECTRONIC DESIGN & PF



TOP DFM ISSUES

- Solder escapes
- Cold spot Hot spot
- Copper unbalanced per comp (tomb stoning)
- Pad sizes <-> geometry component
- Footprint: component vs PCB
- Rotation
- Pin1 + polarity
- Solder mask problems Bridges not manufacturable etc...

DESIGN AUTOMATION & EMBEDDED SYSTEMS

FPGA - SECURITY - INTERNET OF THINGS - ELECTRONIC DESIGN & PRODUCTION - EMBEDDED - DESIGN FOR EXCELLENCE - EMBEDDED DESIGN CHALLENGES

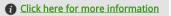
- BGA QFN LGA <= 0.5 mm -> finish Che Ni/Au or Ag
- Via in pad -> adapt layout or Via filling or No Go
- Fiducials?
 - Panel
 - PCB
 - Component
- Overhanging components?
 - V-Cut
 - Break bridges
 - Panel border width
 - IPC component clearance



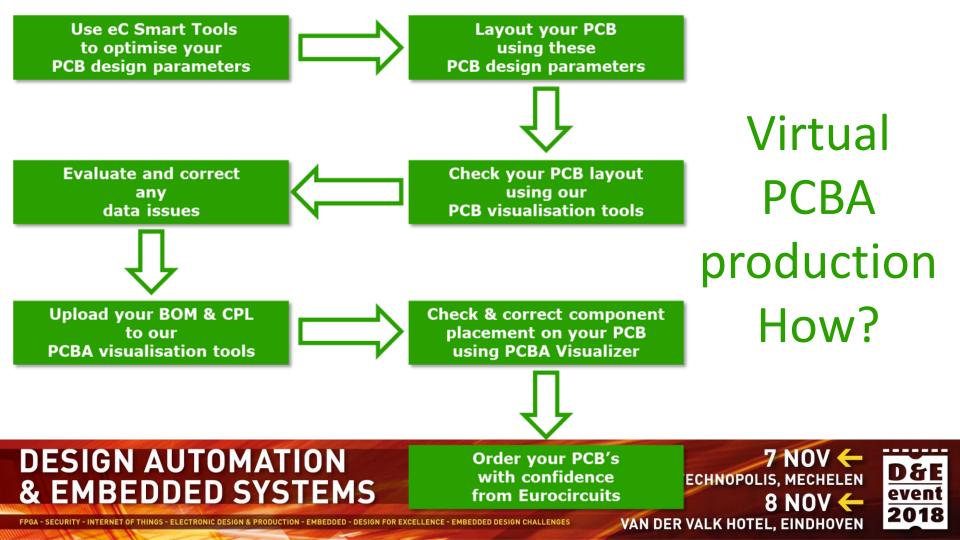
Eurocircuits :: Shopping 🗄 🗙								Wîm — 🗇 🗄
	lits.com/: top/_rders_back ogle Drive 🔍 por '''	etitems.stpx# puts 🗋 parow 🖸	ogy e 🚹 Bit Partos 🗗 jacebook				'nur DFľ	☆ ╗ 0 因
PCB Assembly Visualizer v1.0-2-1	171012 - WDG Demo Assem	ibly (B1228416)				_	Home 🕅 Cart 12 💥 Endich	BETA test version - ©2017 - Eurocircuits n.v.
BOM CPL								📃 Comments 🗲 🏕
Review component place 168 components defined. of whi		pproved.						Load CPL
Bird´s Eye View - Top 📑] Detailed View - Top						Component thumbnails Approve all	Tools
			Footprint 3D 🖌 🖌 Z T+ D Markup	3 🛛 🖻			MT47H128M16RT-25E:C - Micron IC SDRAM 2GBIT 400MHZ 84FBGA	Switch view to bottom side
			A	UZ I				Show component rotation
			118 10					Select overlay
							00000000000000000000000000000000000000	Component list tools
No. L	1					91	525035525 <u>5</u> 5359 <u>5</u> 55	Rotate list left
			000000000000000000000000000000000000000				47 R3 CR4	Rotate list right
	្តំល 📿		000000000					Gffset list
							Approve IC1 Top	Swap sides
	IC3 151							Component tools On selected part
	0		000000000000000000000000000000000000000					Rotate component left
			00000000					Rotate component right
) Bird´s Eye View - Bottom								Set component centroid
		140	$\overline{22} \overline{23} \cdot \overline{R4} R4$	50	160			Offset component
	Click on a component to	select it.						Invert component rotation
	Component list							Delete component
	 Reference designator 	X Y Rotation		Identified part	Image	Datashe		Selected component
	IC1	148.80 -91.30 0	Top MT47H128M16RT-25E:C - Micro IC SDRAM 2GBIT 400MHZ 84FE	on IGA	•	<u>×</u>		- Not approved Approve
	IC2	154.40 -132.5 180	Top ACT8865QI305-T - Active-Semi Processor PMIC 32-TQFN (4x4)	International Inc.	1	<u>×</u>		- No issues detected.
	IC3	132.30 -92.65 0	Top AP5724WG-7 - Diodes Inc. LED Driver IC 1 Output DC DC I	Regulator Step-Up (Boost) PWM Dimming	g 750mA (Switch	0		
	L1	132.20 -89.40 180	Top BRC2518T220K - Taiyo Yuden 22µH Unshielded Wirewound I	nductor 490mA 560 mOhm 1007 (2518 N	Metric)	<u>×</u>		
	L10	-144.7(-132.8(0	Botton MPZ1608S601ATA00 - TDK FERRITE BEAD 600 OHM 0603	ILN		<u>×</u>		
	144	470 4 04 40 0	MPZ1608S601ATA00 - TDK		. 📹	1		

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PCBAVisualizer



Contact support





- Your board "right first time"
 - on time
 - accurate to your intentions
 - at best total cost

• Thanks



Who are Eurocircuits ?

- PCB prototypes & small series producer
- Almost 100% of our sales = online
- + 12.000 customers (20.000 users) in Europe
- + 107.000 orders in 2017
- Started 1991 and is privately owned
- Factories in Hungary, Germany & India
- Local sales in Belgium (HQ), Holland, France, Germany, Switzerland, Italy, UK and Hungary

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