Todays challenges of controlled impedance design and material choice

By: Boy van Veghel

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Q.P.I. Group BV ➔ Fineline QPI BV

- 1988 Quality Products International did start (became QPI Group later on)
  - Development Printed circuit technology
  - Supply of printed circuits
    - Multi-layer, Flex, Flex-rigid, Stretch
    - Advanced materials and constructions
  - PCB Design
    - PCB Lay-out with Mentor, Cadence, Altium and Zuken software
  - PCB Laboratory
- 2015 We became part of Fineline Global Ltd.
  - One of the world leading PCB providers
- 2018 We changed our name to Fineline QPI BV and moved to new location in Panovenweg 12, Helmond

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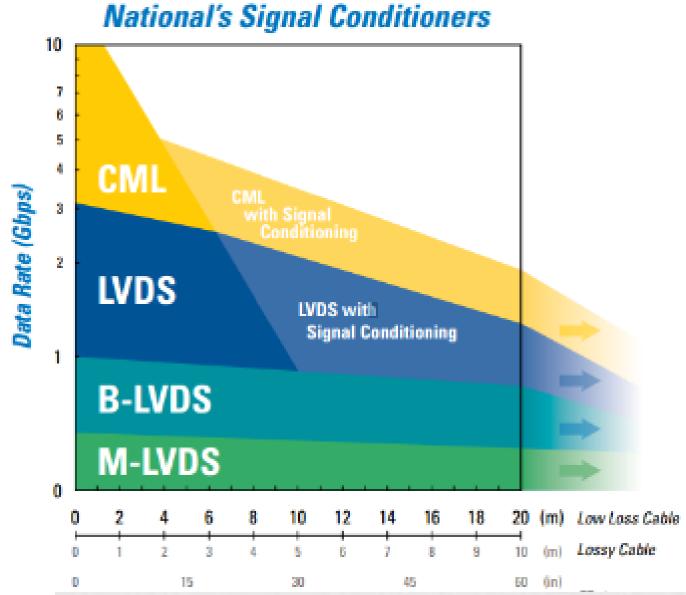
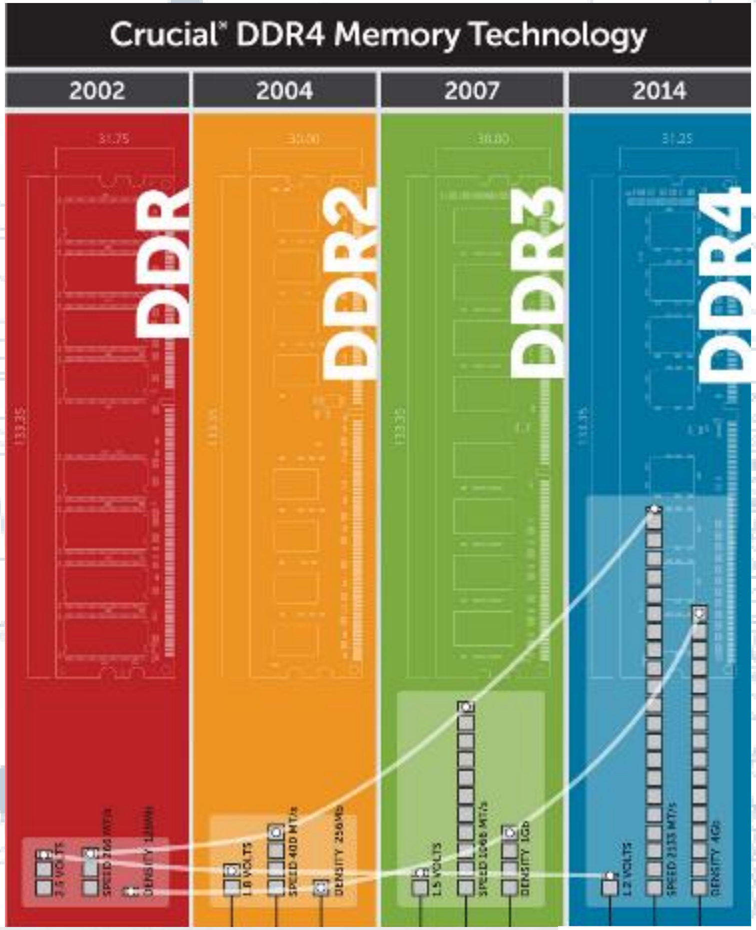
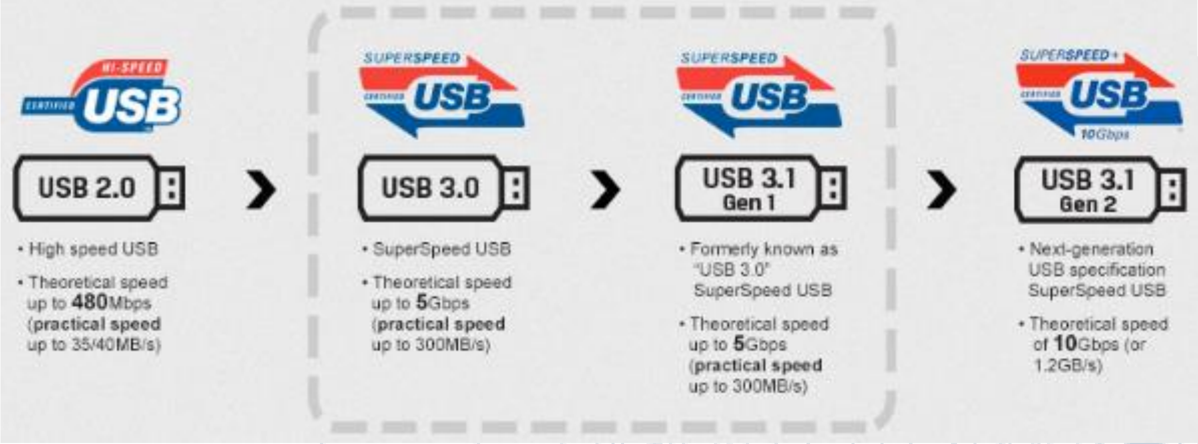
Impedance requirements

- More and more PCB's require Impedance control
- Increase in demand of data speed
  - Higher bit rates
  - Higher frequencies
- Technology drivers
  - DDR 4 signals
  - USB 3 signals
  - LVDS signals
- Material choice is becoming crucial
  - Dk(Er) and Df are very important







What is impedance?

- Impedance (Zo) is the sum of the resistance and reactance of an electrical circuit
- It is measured in Ohms (Ω)
- Impedance is an alternating current characteristic in which signal frequency is an important element
- The longer the trace or the higher the frequency, the more imperative it becomes to control the trace impedance
- Signal frequency is a vital factor for traces which connect to components requiring two to three hundred MHz or more

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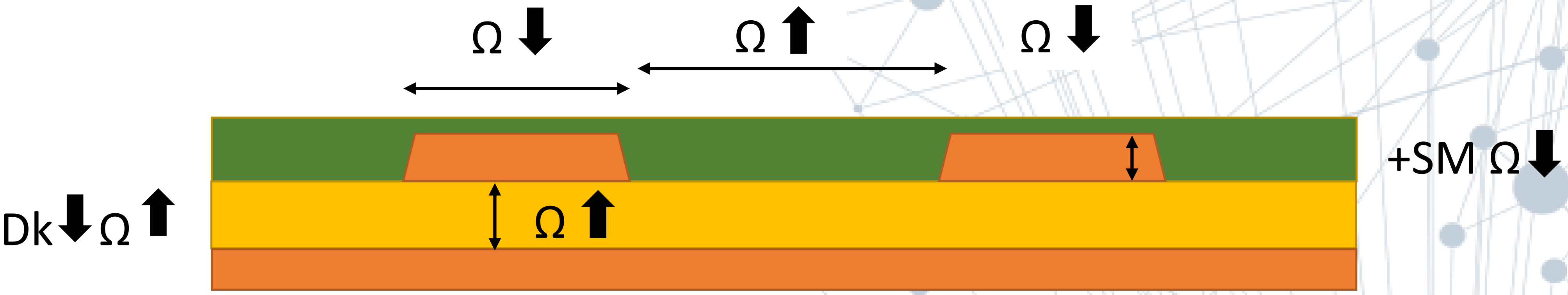
Controlled impedance on PCBs

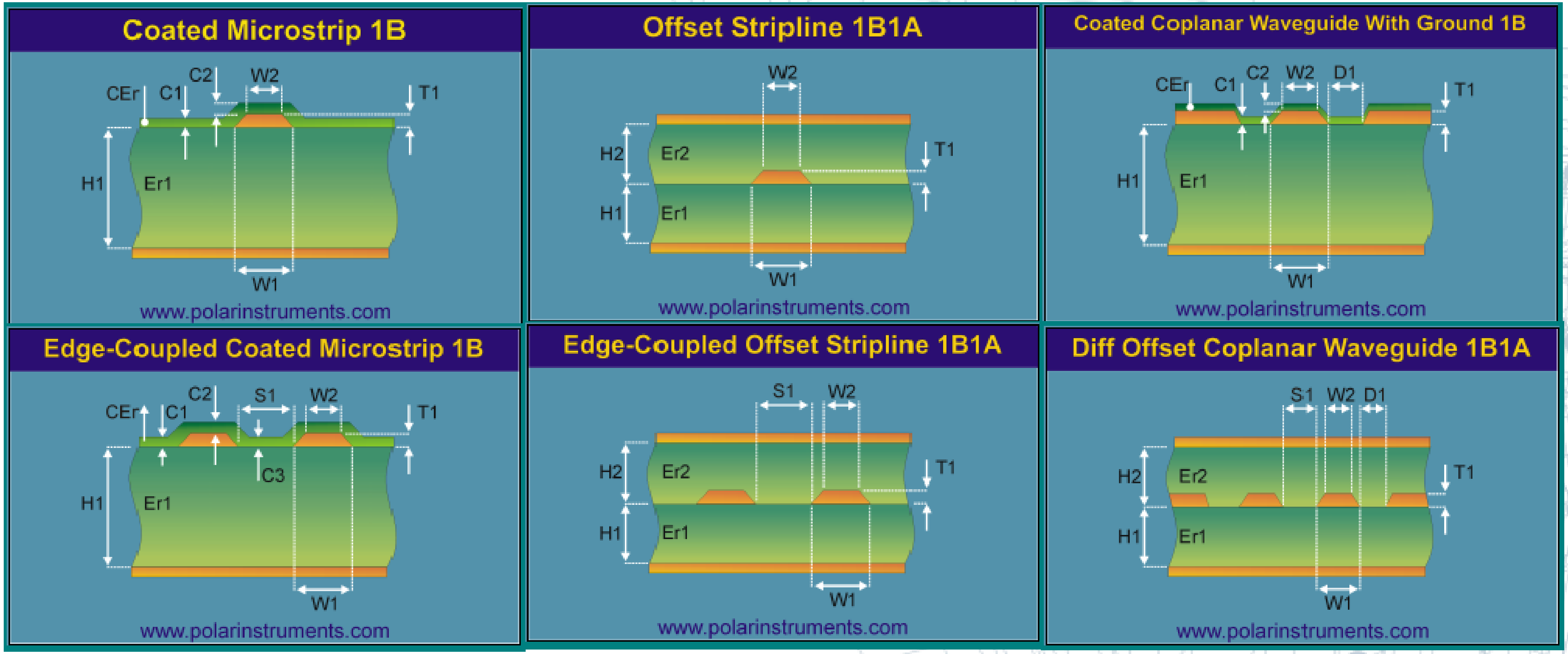
- The impedance is determined by
  - Trace width, trace height
  - Dielectric constant of the board material
  - Distance to reference plane(GND)
- Some basic rules



Common impedance models

Single ended

Differential



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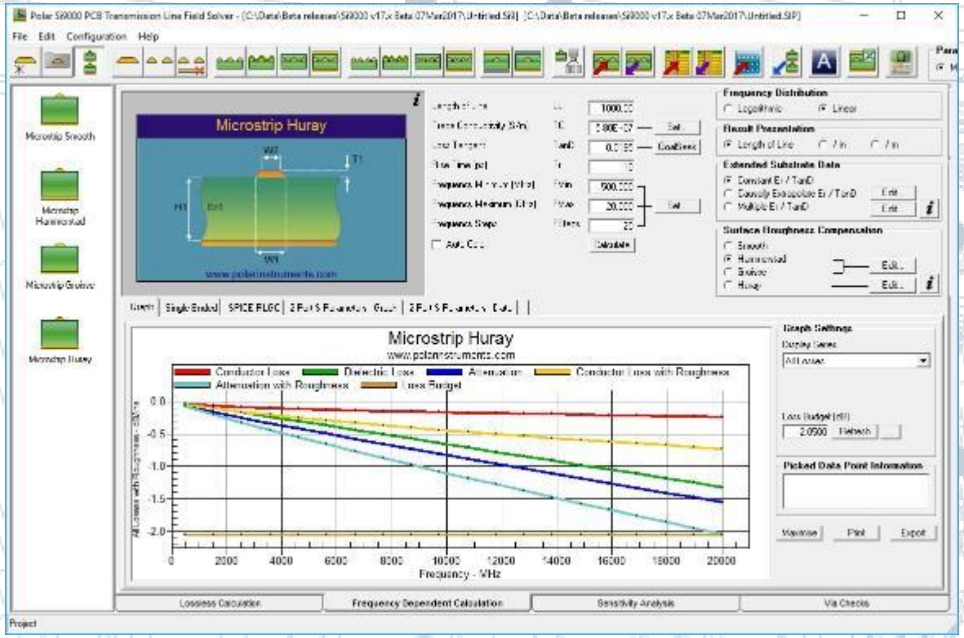
Common controlled impedance values

- Single ended impedance 40Ω, 45Ω, 50Ω, 55Ω, 60Ω, 75Ω
- Differential impedance 80Ω, 85Ω, 90Ω, 100Ω
- Impedance at Fineline-QPI will be calculated using
  - ➢ Polar SI9000
  - ➢ Polar speedstack
- After production impedance will be verified
  - Via a special designed test coupon on production panel



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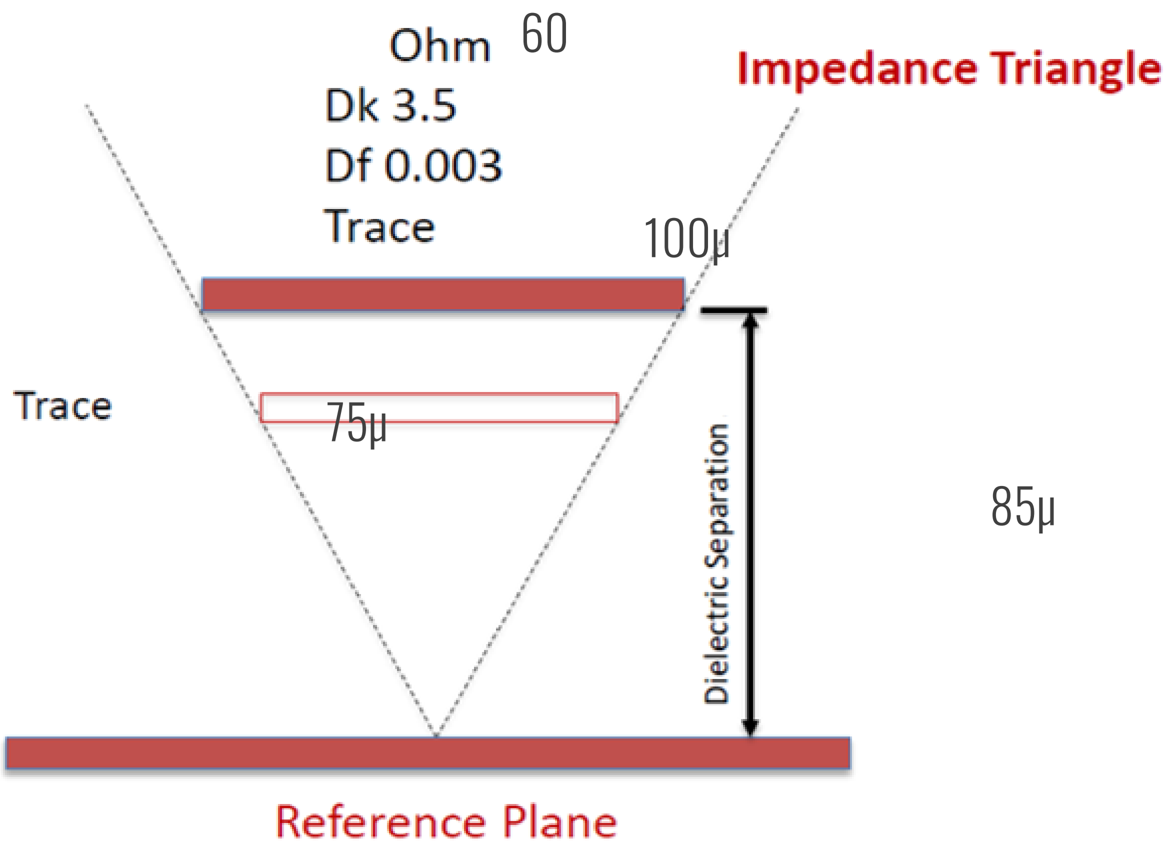
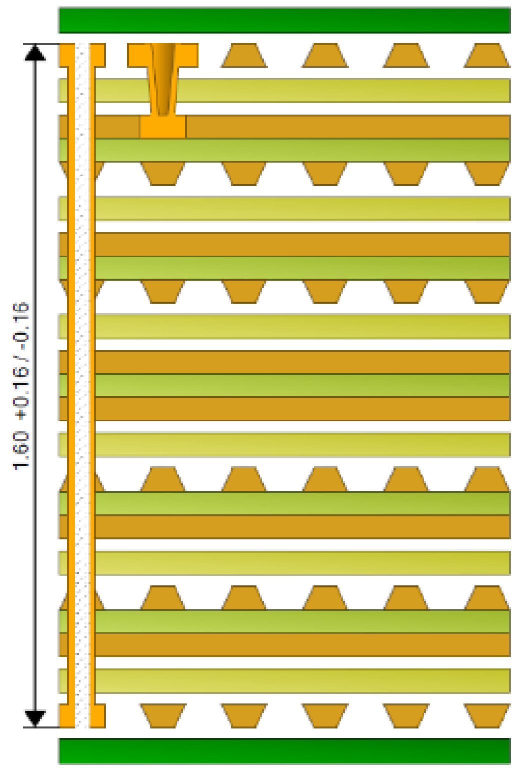
Design challenges

- Combination of low and high impedance
  - e.g. 40Ω, and 60Ω single ended
  - e.g. 80Ω and 100Ω differential
- Require the opposite value
  - In trace width
  - In trace thickness
  - In reference isolation to GND



Impedance calculation

- Example outer layer impedance of 40,50,60 Ω SE and 80,90,100 Ω Diff.

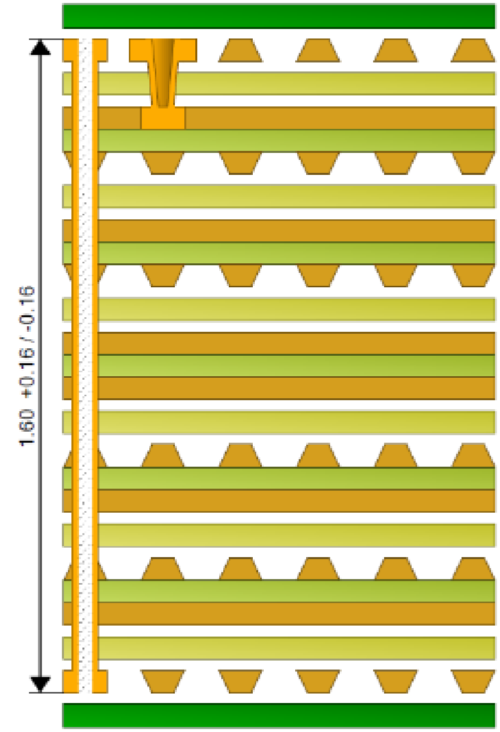


Layer	Stack up	Processed Thickness	εr	Mask Thickness	Isolation Distance
		0.020	4.000	0.020	
1		0.035			
		0.070	4.400		0.070
2		0.018			
		0.075	4.400		0.075
3		0.018			
		0.140	4.400		0.140
4		0.035			
		0.075	4.400		0.075
5		0.035			
		0.140	4.400		0.140
6		0.035			
		0.150	4.400		0.150
7		0.035			
		0.140	4.400		0.140
8		0.035			
		0.075	4.400		0.075
9		0.035			
		0.140	4.400		0.140
10		0.035			
		0.075	4.400		0.075
11		0.035			
		0.070	4.400		0.070
12		0.035			
		0.020	4.000	0.020	

Structure Image	Impedance ID	Structure Name	Impedance Signal Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Calculated Impedance
	1	Coated Microstrip 1B	1	0.155	0.135	0.000	40.350
	2	Coated Microstrip 1B	1	0.095	0.075	0.000	51.320
	3	Coated Microstrip 1B	1	0.060	0.040	0.000	61.520
	4	Edge Coupled Coated Microstrip 1B	1	0.130	0.110	0.150	80.440
	5	Edge Coupled Coated Microstrip 1B	1	0.100	0.080	0.150	90.740
	6	Edge Coupled Coated Microstrip 1B	1	0.080	0.060	0.150	99.440

Impedance calculation

- Example inner layer impedance of 40,50,60 Ω SE and 80,90,100 Ω Diff.



Layer	Stack up	Processed Thickness	εr	Mask Thickness	Isolation Distance
		0.020	4.000	0.020	
1		0.035			
		0.070	4.400		0.070
2		0.018			
		0.075	4.400		0.075
3		0.018			
		0.140	4.400		0.140
4		0.035			
		0.075	4.400		0.075
5		0.035			
		0.140	4.400		0.140
6		0.035			
		0.150	4.400		0.150
7		0.035			
		0.140	4.400		0.140
8		0.035			
		0.075	4.400		0.075
9		0.035			
		0.140	4.400		0.140
10		0.035			
		0.075	4.400		0.075
11		0.035			
		0.070	4.400		0.070
12		0.035			
		0.020	4.000	0.020	

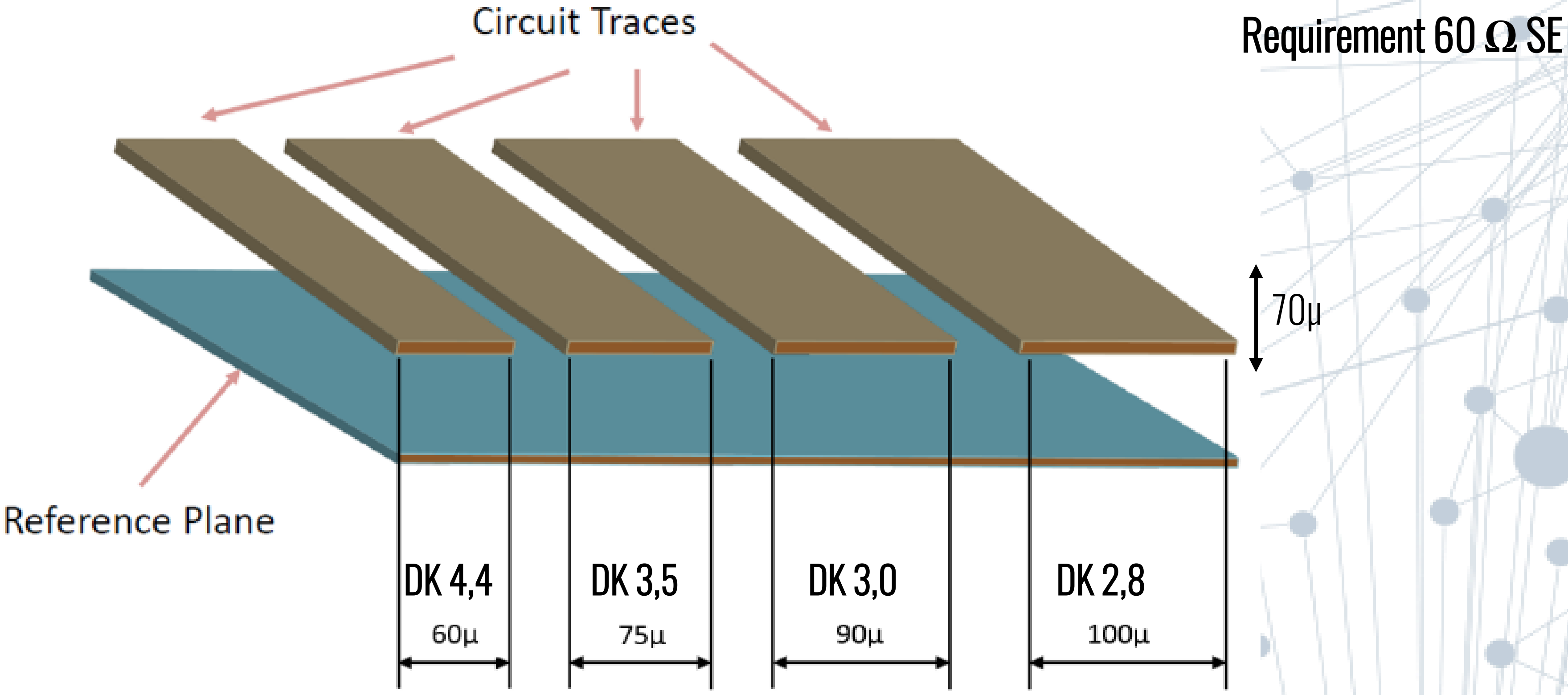
Structure Image	Impedance ID	Structure Name	Impedance Signal Layer	Lower Trace Width (W1)	Upper Trace Width (W2)	Trace Separation (S1)	Calculate Impedanc
	7	Offset Stripline 1B1A	3	0.110	0.095	0.000	40.740
	8	Offset Stripline 1B1A	3	0.070	0.055	0.000	50.450
	9	Offset Stripline 1B1A	3	0.045	0.030	0.000	59.870
	10	Edge Coupled Offset Stripline 1B1A	3	0.100	0.085	0.150	81.490
	11	Edge Coupled Offset Stripline 1B1A	3	0.080	0.065	0.150	90.260
	12	Edge Coupled Offset Stripline 1B1A	3	0.060	0.045	0.150	101.530

Design challenges

- Thinner/smaller traces = higher trace resistance = lower system performance
- Traces <75µm
  - Will lower the yield in manufacturing
  - Price of the PCB will increase
  - Lead-time will be longer
- Solution would be to lower the Dk
- Lowering the Dk to e.g. 3,5 makes the track width go up to 75µm
  - Better yield,
  - Lower price
  - Shorter leadtime

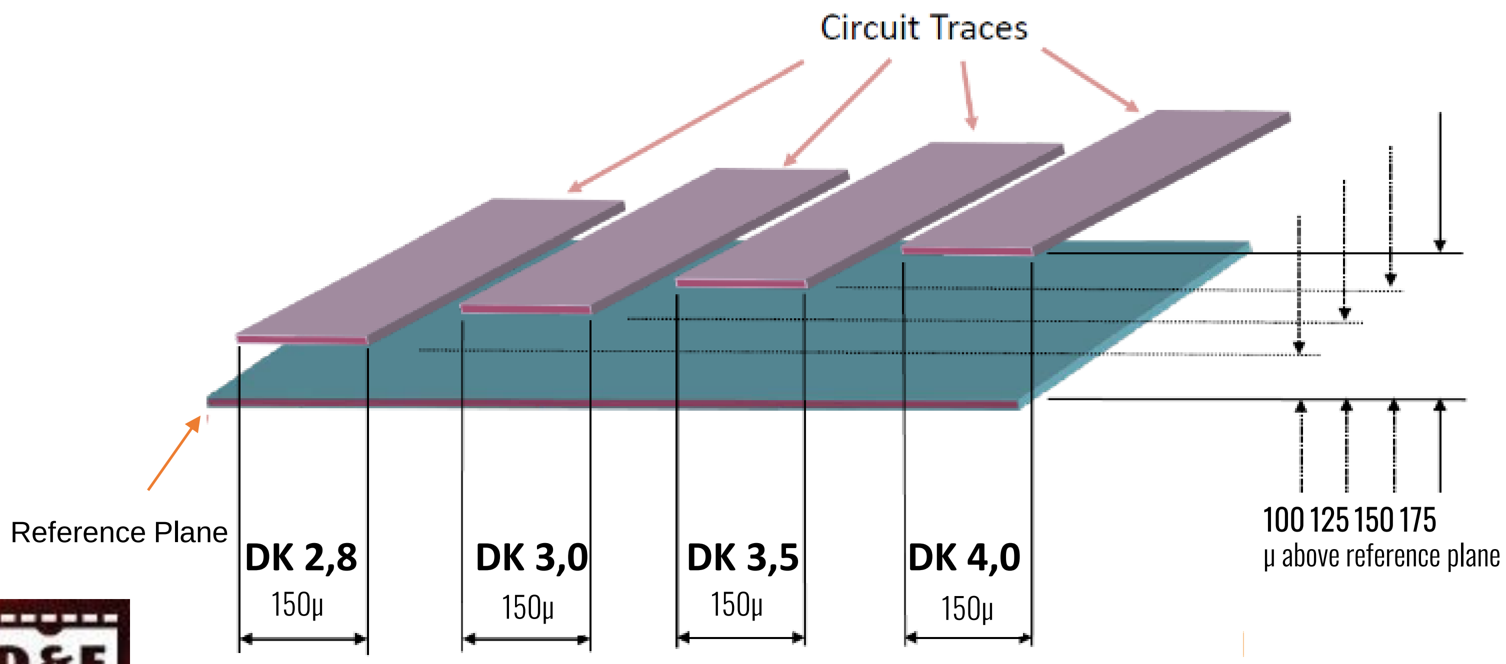
Low Dk material

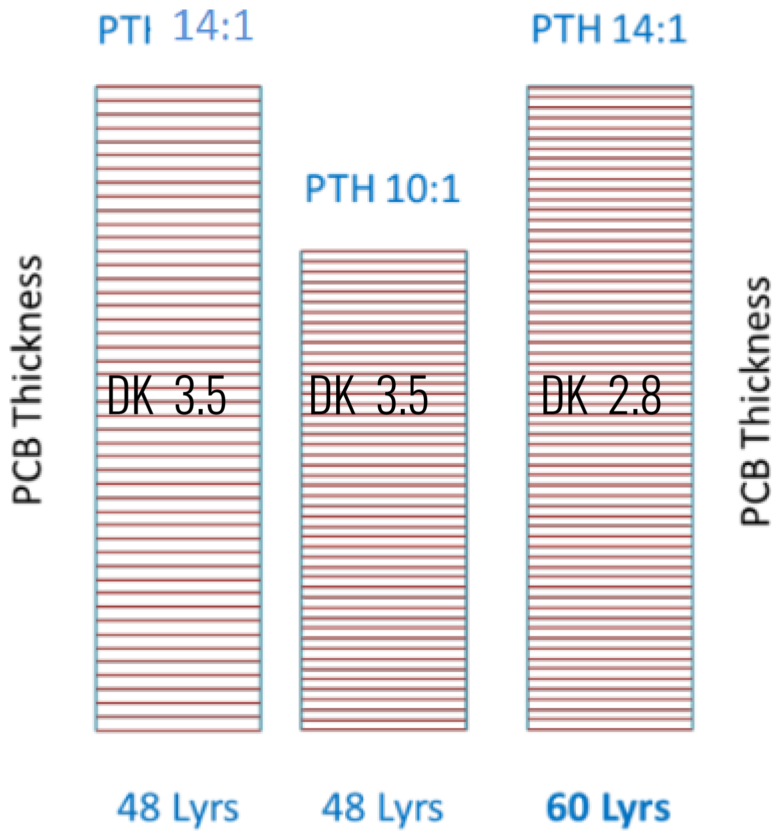
- Using a low DK material has several advantages
  - The trace width increases
  - Copper weights can increase for high current



Low Dk material

- The number of layers can be increased within the same thickness
- The thickness can be decreased to improve on aspect ratio





Choosing the rigth material

- Key factors in choosing the right material for your design
  - Dielectric contant (Dk)
  - Dissipation factor (Df)
  - Copper foil type
  - Glass style
- A lot of different laminate manufactures offer a wide range of products
  - Dk&Df are often given as an average value
  - Every prepreg and laminate thickness has there own Dk&Df value
  - These small differences can have a huge impact on controlled impedance lines and signal integrity
- Lead-times and MOV or MOQ varies from one to another

Choosing the rigth material

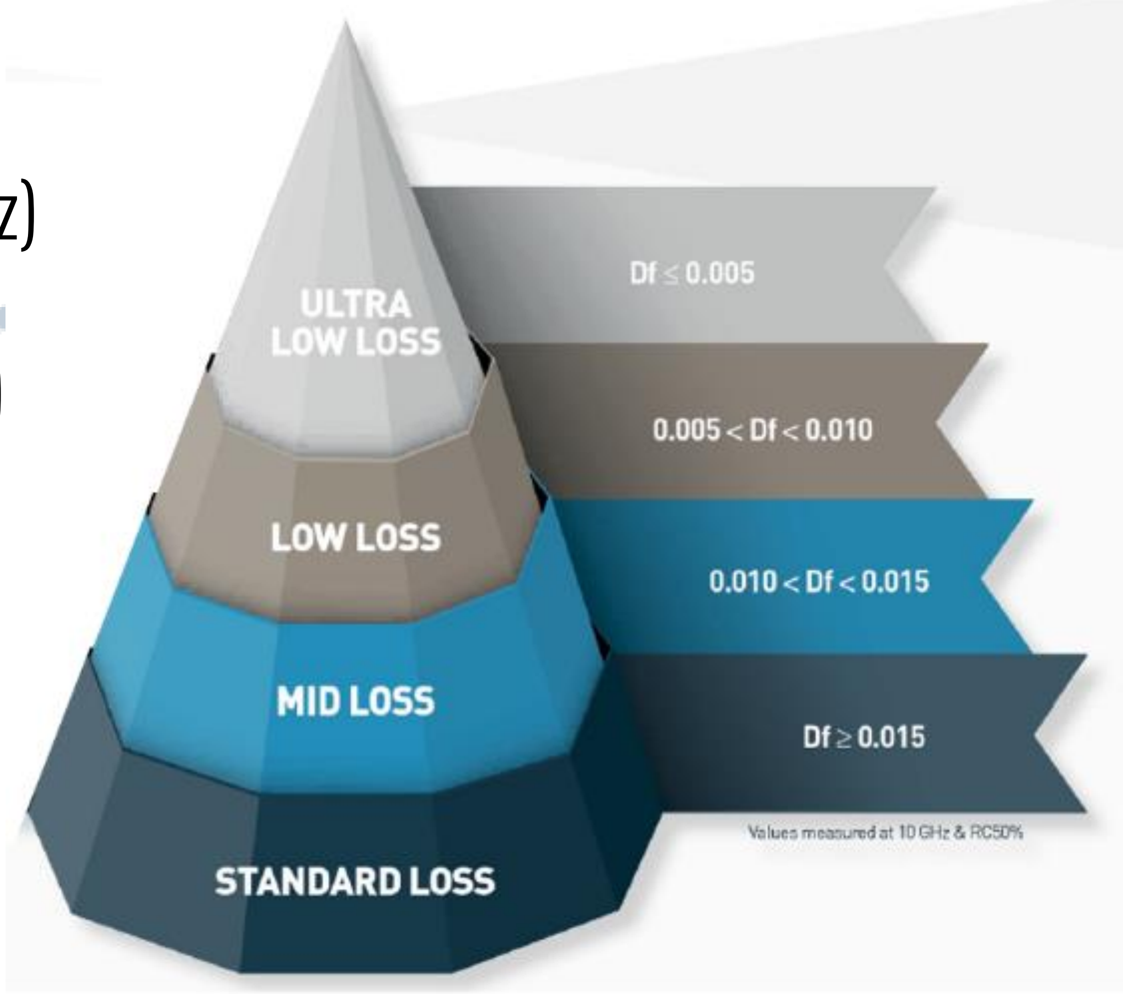
- Material vs frequency
  - Depending on insertion loss

High speed FR-4 (40-77Ghz)

Advanced FR-4 (10-20Ghz)

Improved FR-4 (5-10Ghz)

Standard FR-4 (<5Ghz)



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Choosing the rigth material

- Some examples

Brand	Type	Dk	Df
Isola	FR408HR	3,65	0,0095
Panasonic	Megtron 6	3,61	0,004
Isola	I-Tera MT40	3,45	0,0031
Ventec	VT-464	3,5	0,013
Nelco	N4800-20SI	3,24	0,0064
Ventec	VT-462	3,05	0,0035
Isola	Astra MT77	3,00	0,0017

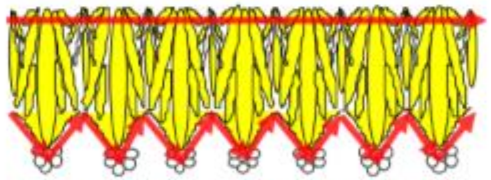
Copper foil

- The roughness of the copper foil has an effect on impedance and signal loss(Skin depth)
- Low profile copper foils gives the lowest loss

Frequency	Skin Depth
10 MHz	21 µm

The current is able to tunnel below the surface profile and through the bulk of the conductor

Frequency	Skin Depth
100 MHz	6.6 µm



The current is forced to follow every peak and trough of the surface profile increasing path length and resistance

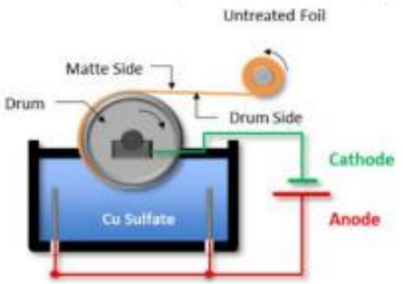
Frequency	Skin Depth (Copper)
50 Hz	9.3 mm
10 MHz	21 µm
100 MHz	6.6 µm
1 GHz	2.1 µm
10 GHz	0.66 µm

Copper foil

- There are two sorts of copper foils
  - RA (Rolled annealed)
  - ED (Electro deposited)

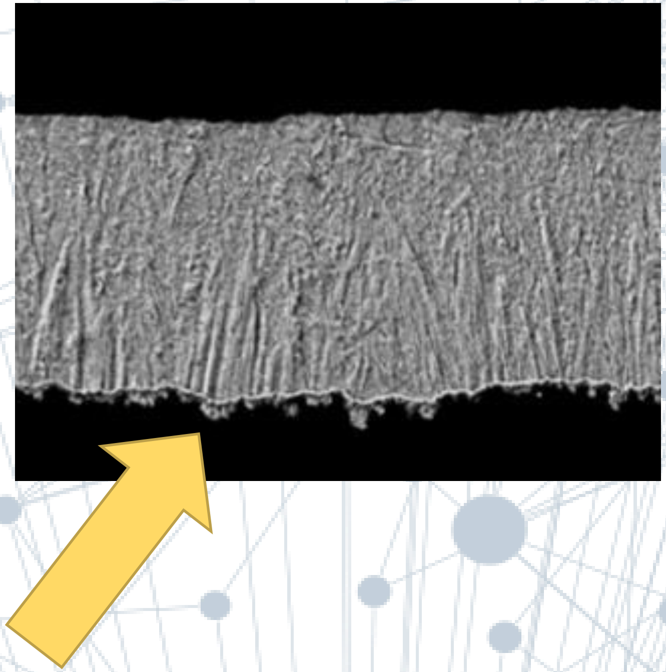
Copper Foil Manufacturing Processes

Rolled	VS	Electro-deposited (ED)



- Smoother
- Higher Cost

- Rougher
- Lower Cost



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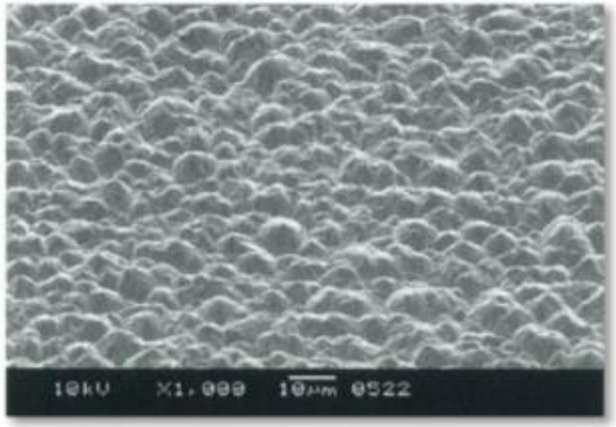
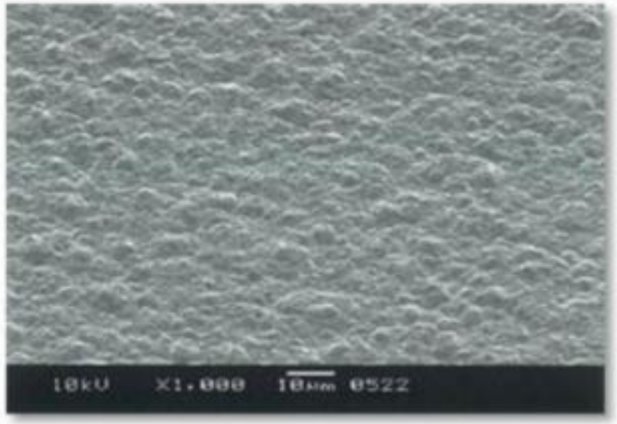
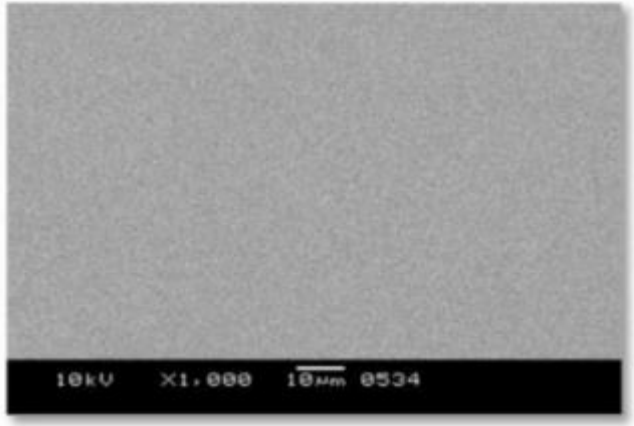
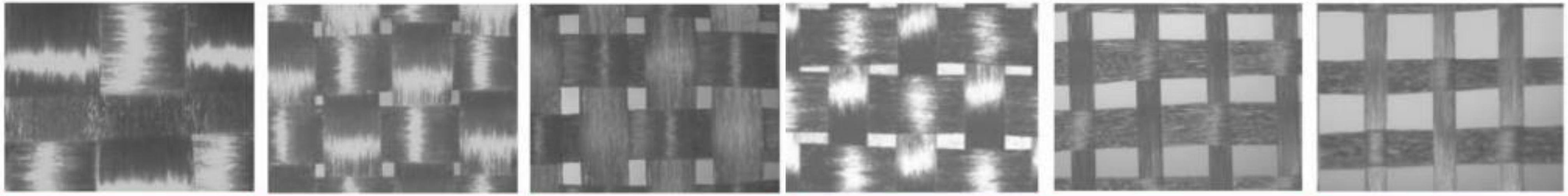
Copper foil

Common Roughness Profiles

IPC Standard Profile	IPC Very Low Profile(VLP)	Ultra Low Profile (ULP)Class
		
No min/max spec	< 5.2 μm max	-*Other names: HVLP*, VSP -No IPC spec -Typically < 2 μm max

Glass style

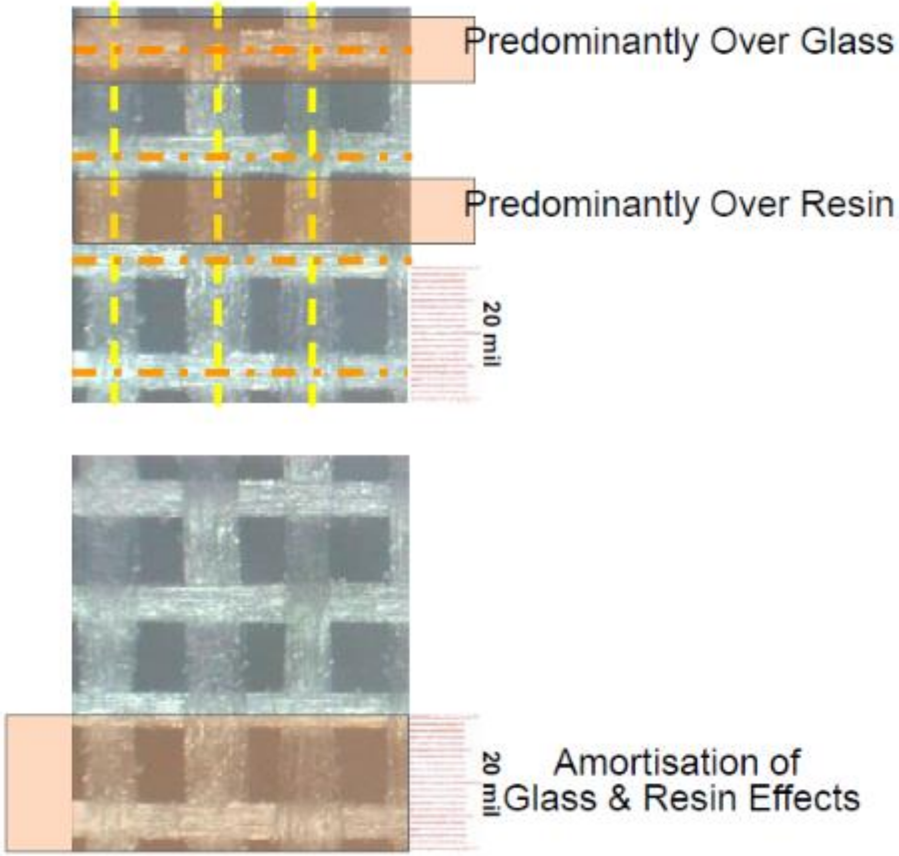
- High variety of glass styles and resin contents available
- The resin content determins the Dk for a great deal

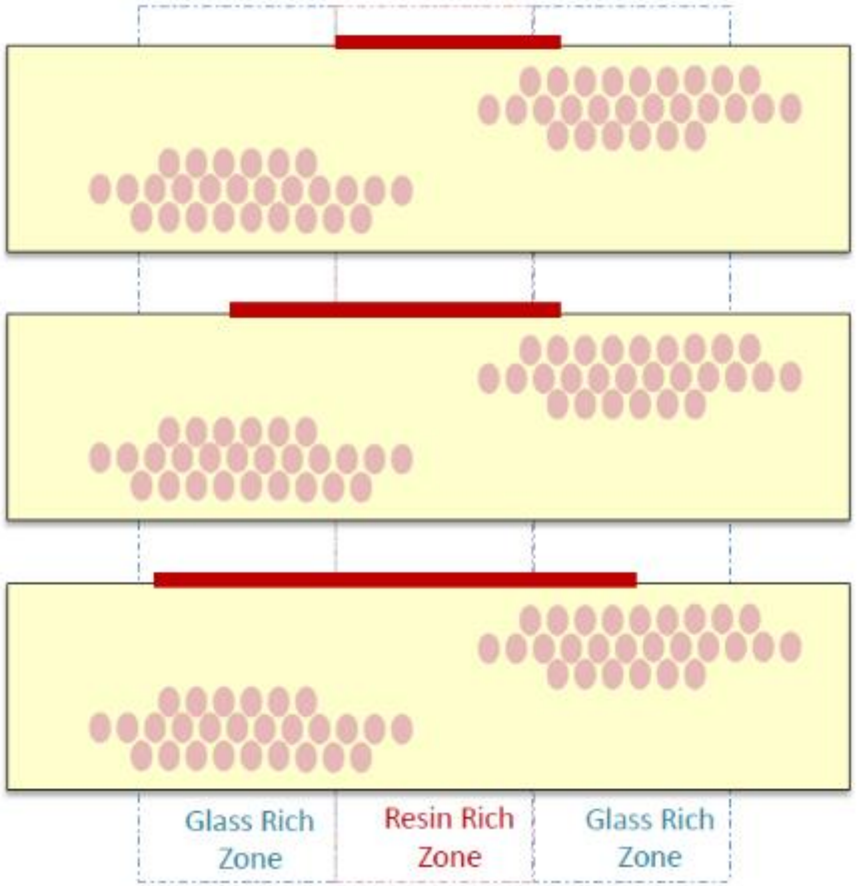


Glass Style	7628	2116	2113	2125	1080	106
Weight (grams/sq.m)	203	104	78	87	47	24
Thread count	17.3 x 12.2	23.6 x 22.8	23.6 x 22.0	15.7 x 15.4	23.6 x 18.5	22.0 x 22.0
Yarn (warp/weft)	EC9 68/EC9 68	EC7 22/EC7 22	EC7 22/EC5 11	EC7 22/EC9 34	EC5 11/EC5 11	EC5 5.5/EC5 5.5
Glass thickness (mm)	0.17	0.095	0.079	0.09	0.05	0.033
Pressed thickness* (mm)	0.18 - 0.22	0.110 - 0.125	0.085 - 0.10	0.10 - 0.12	0.065 - 0.080	0.048 - 0.060

Glass style

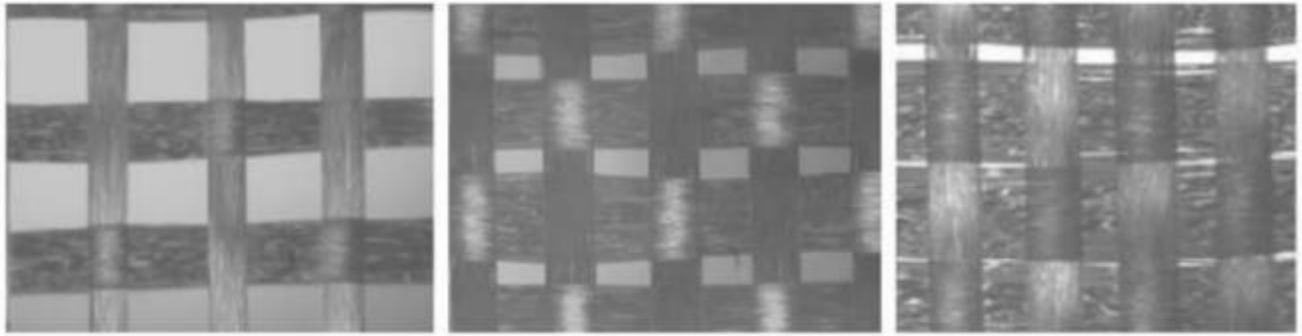
- Trace width effects on Skew





Glass style

- Spread glass



Glass Style	106	1067	1067 Spread **
Weight (grams/sq.m)	24	31	31
Thread count	22.0 x 22.0	27.6 x 27.6	27.6 x 27.6
Yarn (warp/weft)	EC5 5.5/EC5 5.5	EC5 5.5/EC5 5.5	EC5 5.5/EC5 5.5
Glass thickness (mm)	0.033	0.035	0.035
Pressed thickness* (mm)	0.050 - 0.060	0.054 - 0.064	0.054 - 0.064

Conclusion

- Before starting a design be aware of all your requirements
- Determine the material needed and check availability
- Do not over specify your design
    - E.g. don't choose an ultra low loss material if you are only running on 5-10Ghz
- Consult Fineline-QPI for advise

Thank you for your attention!

FINELINE QPI BV

The Dutch based Subsidiary of Fineline Global

Panovenweg 12
5708 HR Helmond
The Netherlands

T +31 (0)492 590059
E INFO-QPI@FINELINE-GLOBAL.COM
I FINELINE-GLOBAL.COM | QPIGROUP.COM

PCB

Single | Double sided
Multi-layer
Flex circuit
Flex-rigid circuit
Stretch circuits
IMS - Al_2O_3 technology

Design

Mentor - PADS | Expedition | DX
Zuken – Cadstar
Altium – Designer
Cadence – Orcad | Allegro

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