• Ruggedize your AI & Edge Computing with Modularized LGA

Jarry Chang / DFI

DESIGN AUTOMATION & EMBEDDED SYSTEMS
FPGA - SECURITY - INTERNET OF THINGS - ELECTRONIC DESIGN & PRODUCTION - EMBEDDED - DESIGN FOR EXCELLENCE - EMBEDDED DESIGN CHALLENGES
7 NOV
TECHNOPOLIS, MECHELEN
8 NOV
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DFI AT a Glance

10M+ EMBEDDED BOARDS ALL OVER THE WORLD

37 YEARS IN-DEPTH EXPERIENCE IN EMBEDDED SOLUTIONS

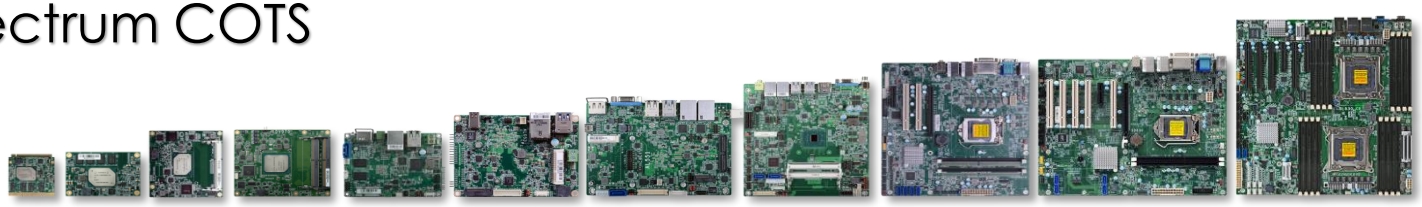
180+ R&D OUTSTANDING ENGINEERS

122.2M REVENUES IN 2017

11 SITES SERVICE CENTERS WORLDWIDE

15 YEARS EXTENDED LONG TERM SUPPORT

| Full Spectrum COTS



| No Compromise Customization

| One Stop ODM Service

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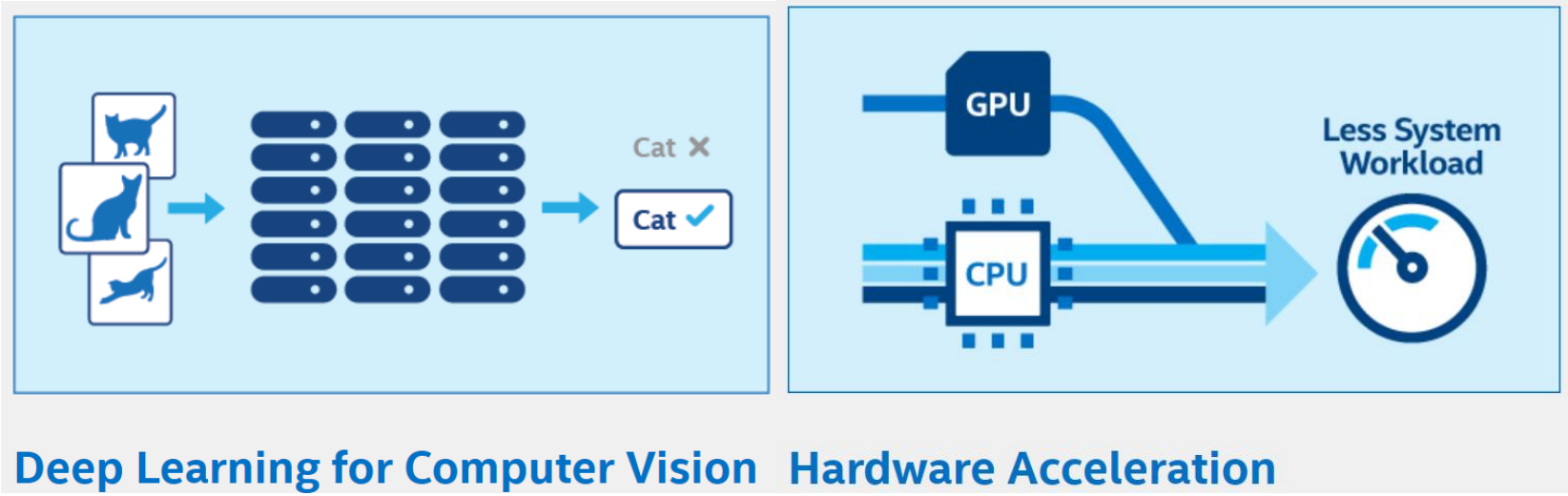
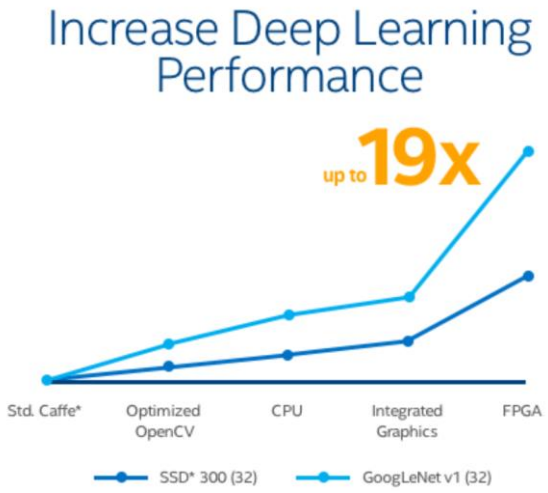
• Blueprint of AI & IoT

- OpenVINO

OpenVINO™ is a comprehensive toolkit for quickly developing applications and solutions that emulate human vision. It extends CV workloads across Intel® hardware, maximizing performance.





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• DFI Blueprint of AI & IoT

Intel® Movidius™ Myriad™ X VPU

A dedicated hardware accelerator for deep neural network inferences.

Movidius Myriad Family VPUs		
	Myriad 2	**Myriad X**
Compute Capacity	>1 TOPS	>4 TOPS
Vector Processors	12x SHAVE Processors	16x SHAVE Processors
CPUs	2x LEON4 cores (RISC; SPARC V8)	2x LEON4 cores (RISC; SPARC V8)
Neural Network Capability	1st Gen DNN Support (Up to 100 GFLOPS)	Neural Compute Engine (Up to 1 TFLOPS)
Key Interfaces	12x MIPI lanes (DPHY 1.1) USB 3 SPI I2S SD 1GbE	16x MIPI lanes (PHY 1.2) USB 3.1 Quad SPI I2S 2x SD 10GbE

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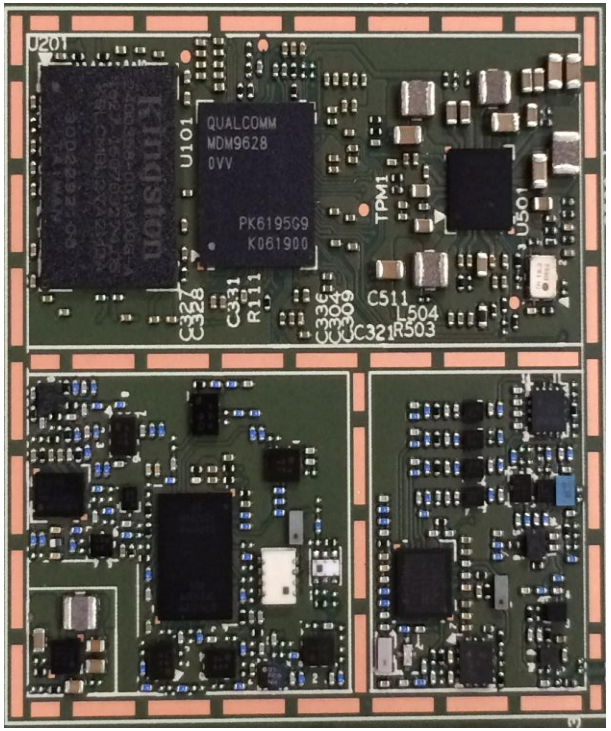
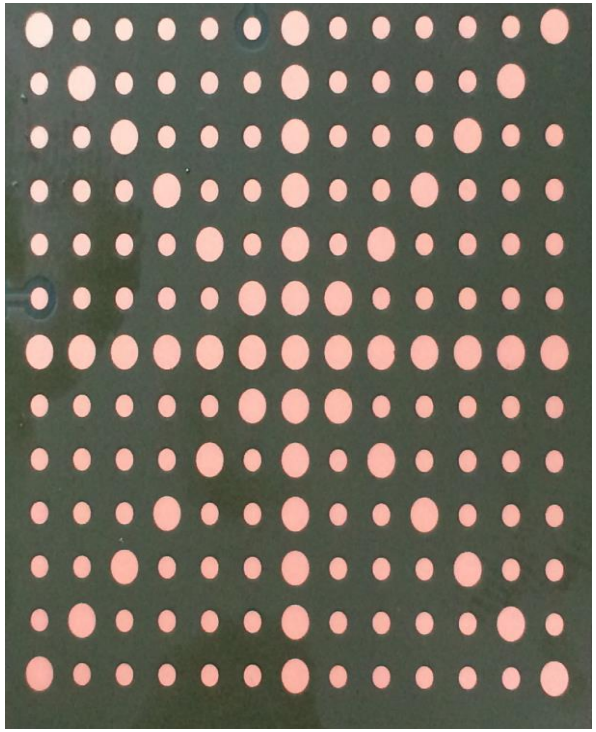
•LTE Module Design (Pre-Tin Ready)

- LGA Land Pad Specification
  - Total 168 pads
  - Pad diameter
    - Large size pad: 1.6mm
    - Small size pad: 1.0mm





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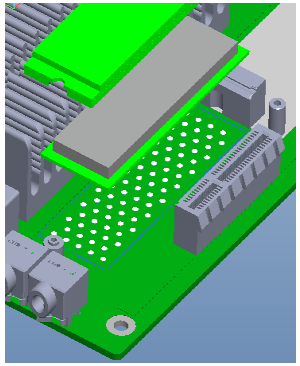
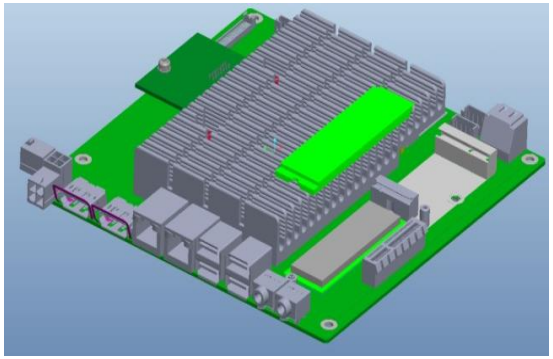
•On M/E Point of View

- DFI propose AI LGA board, Best for in-vehicle & industrial harsh environment

- Anti-Vibration for transportation.
- w/Conformal coating, excellent protection against corrosion.





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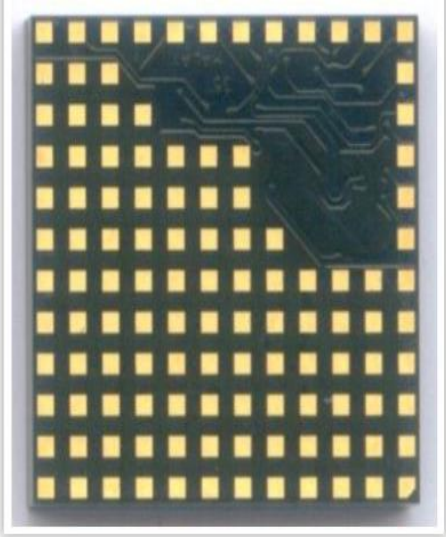
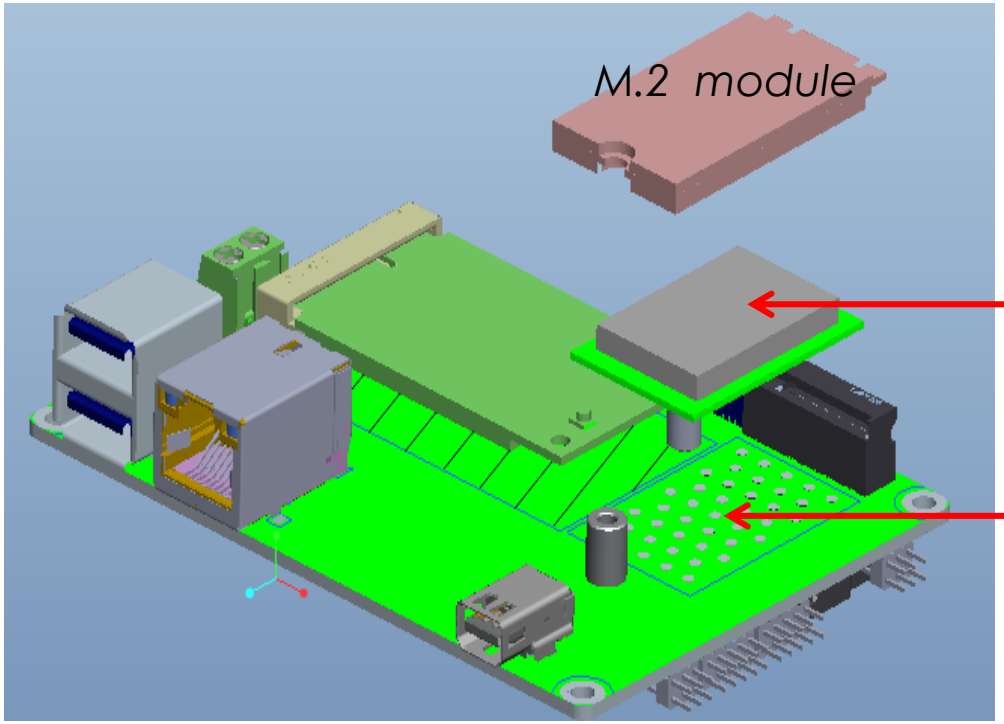
• New Define for AI board, LGA Design

- AI core as LGA Lan Pad board



Benefit :
Anti-vibration
field side upgradable.

- AI board fitted on M/B by LGA pad. (reference to M.2 dimension)



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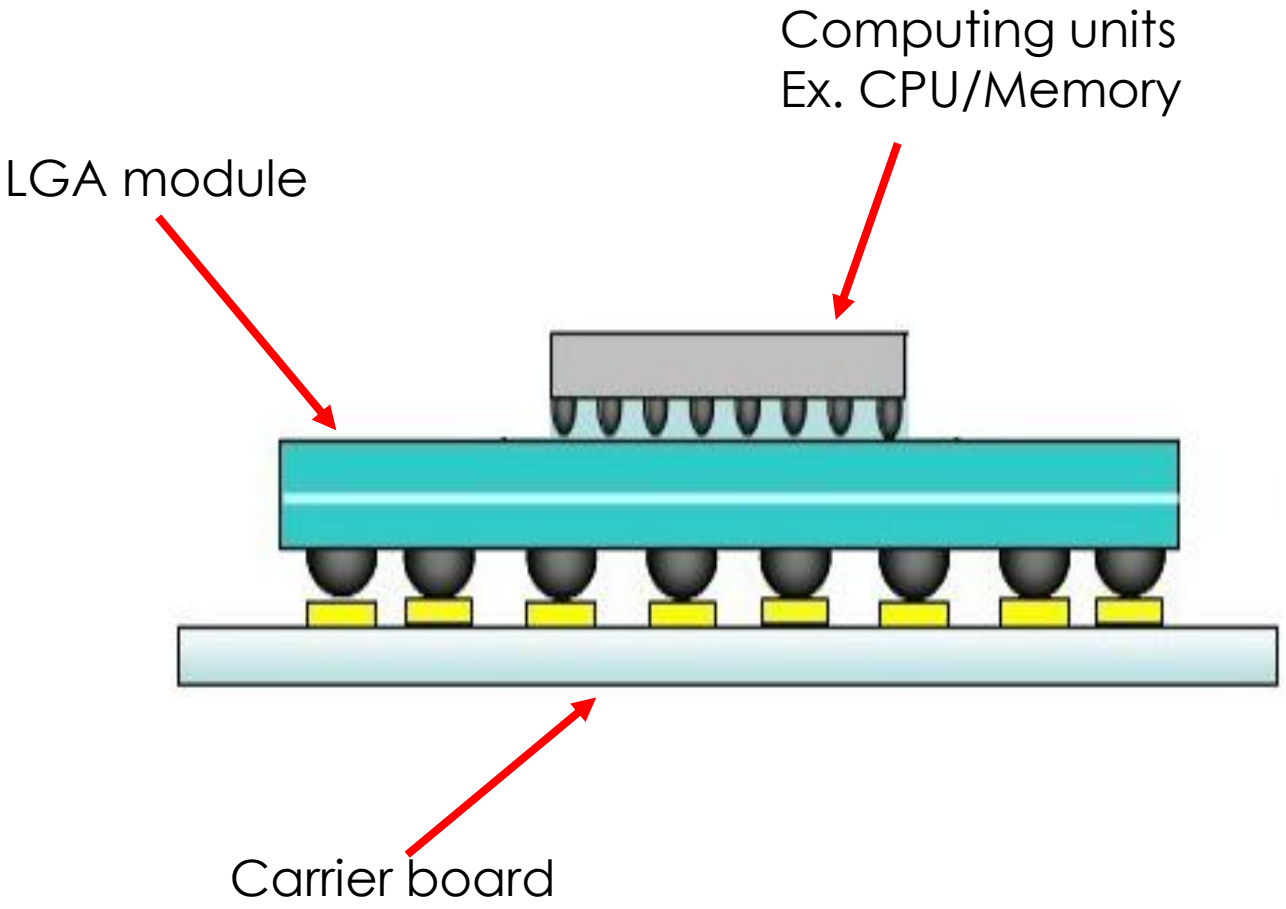
•LGA Module Concept



- Connector Free
- Anti-vibration
- Easy for Coating
- Made for rugged application

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Ruggedized design of ML & AL Application

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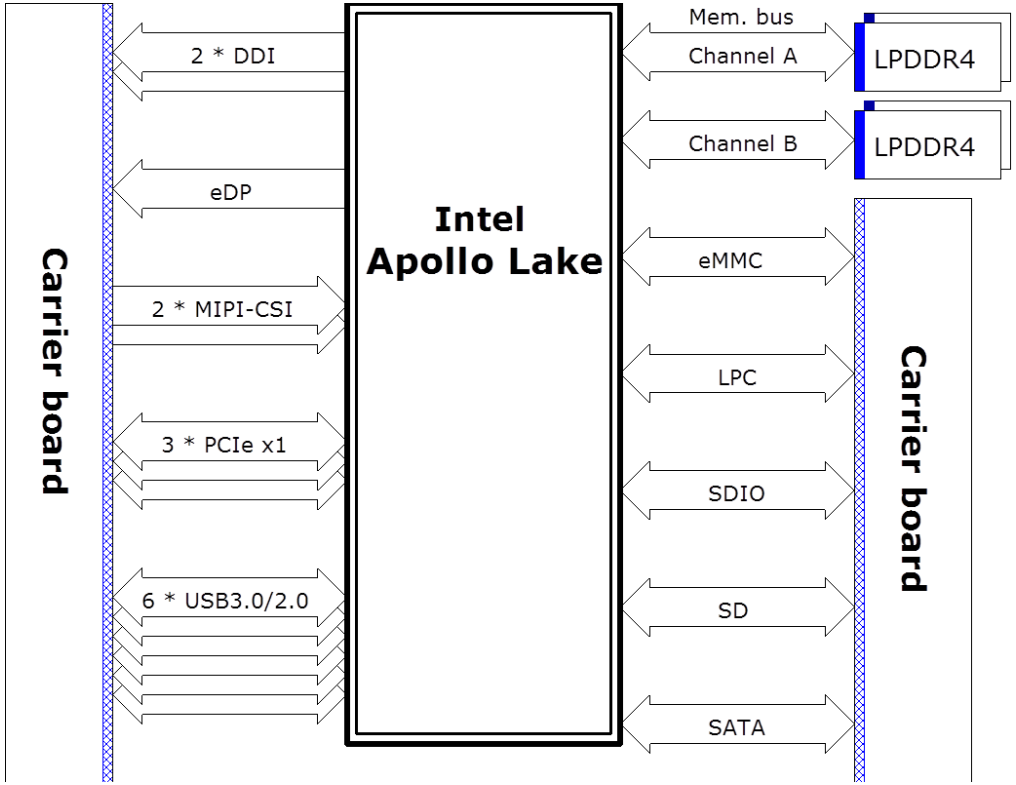
•Design Experience Sharing

LGA module Block Diagram



- LGA module
- Intel® Atom E3900/A3900 series
- LPDDR4 up to 8GB
- eMMC up to 64GB
- 6 USB 3.0
- 2 DDI, 1 eDP
- 2 MIPI-CSI
- 3 PCIex1
- 1 SDIO
- 1 SD interface
- 1 SATA
- 1 LPC interface

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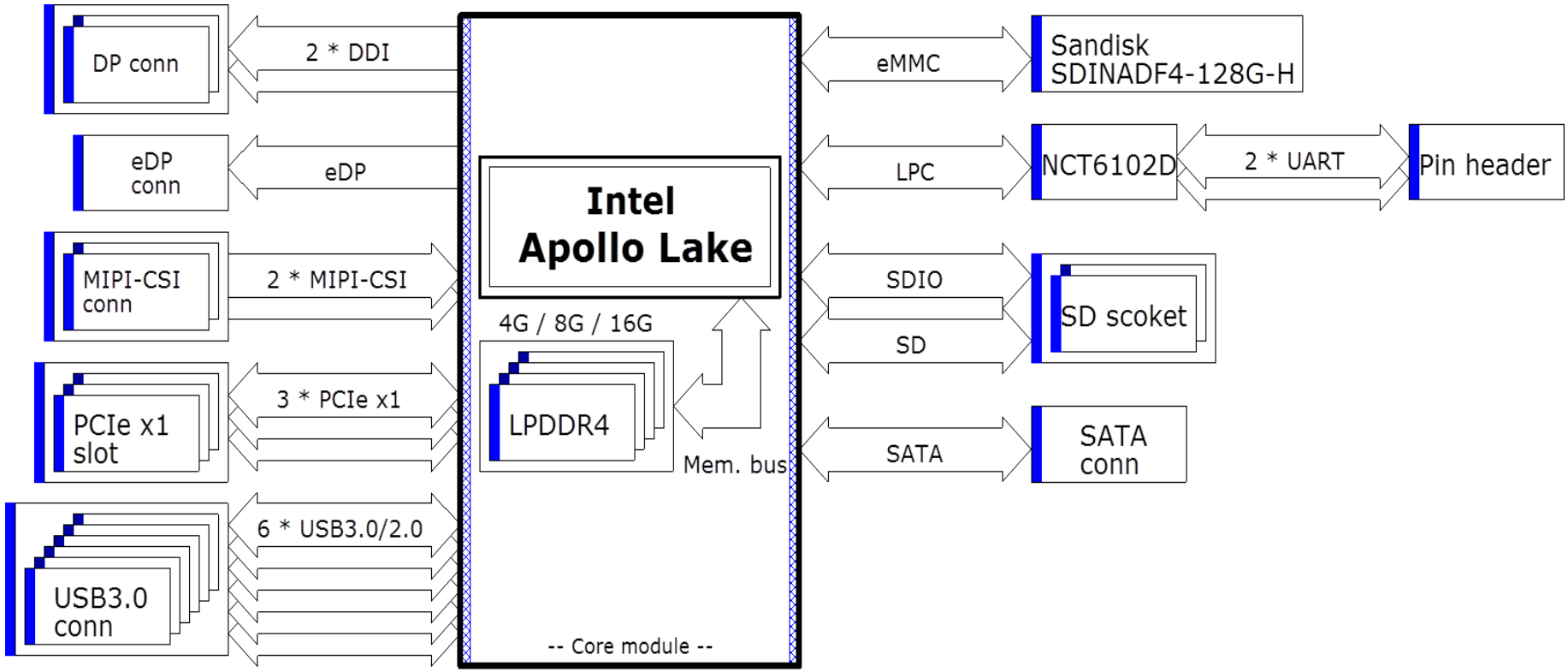
• Design Experience Sharing

- LGA Carrier Block Diagram



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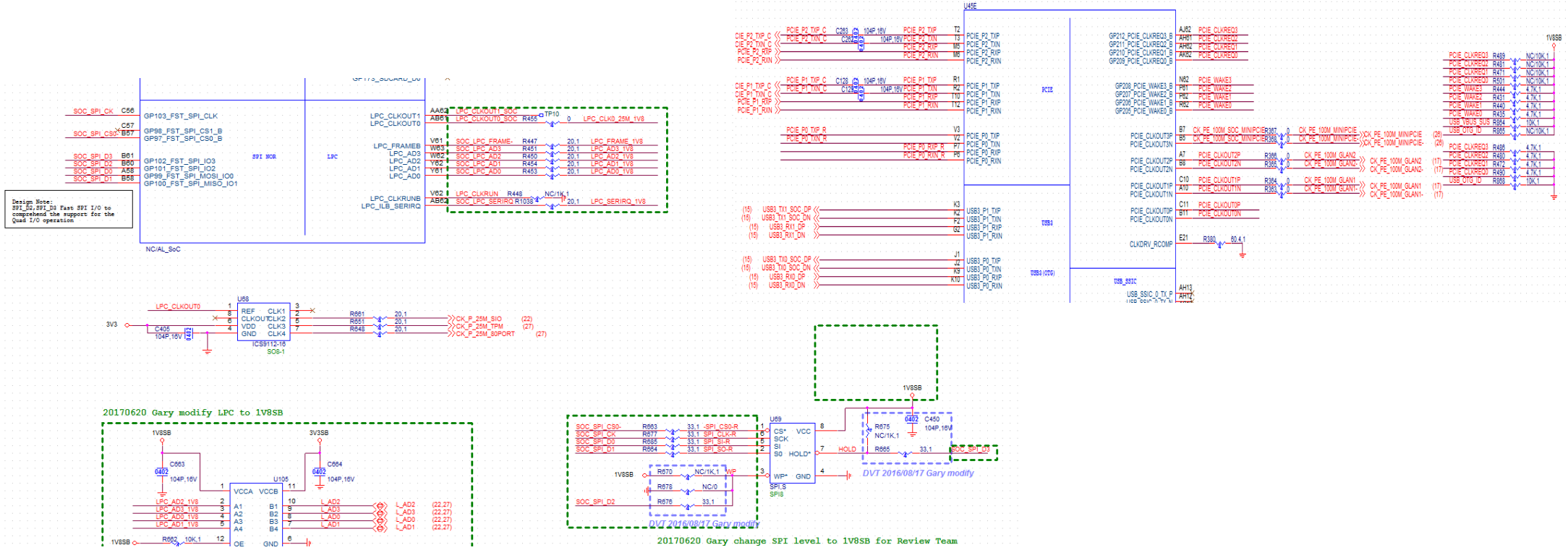
•Design Experience Sharing

Challenge

Extremely small PCB size is only 55*53.3mm Components are only on top size



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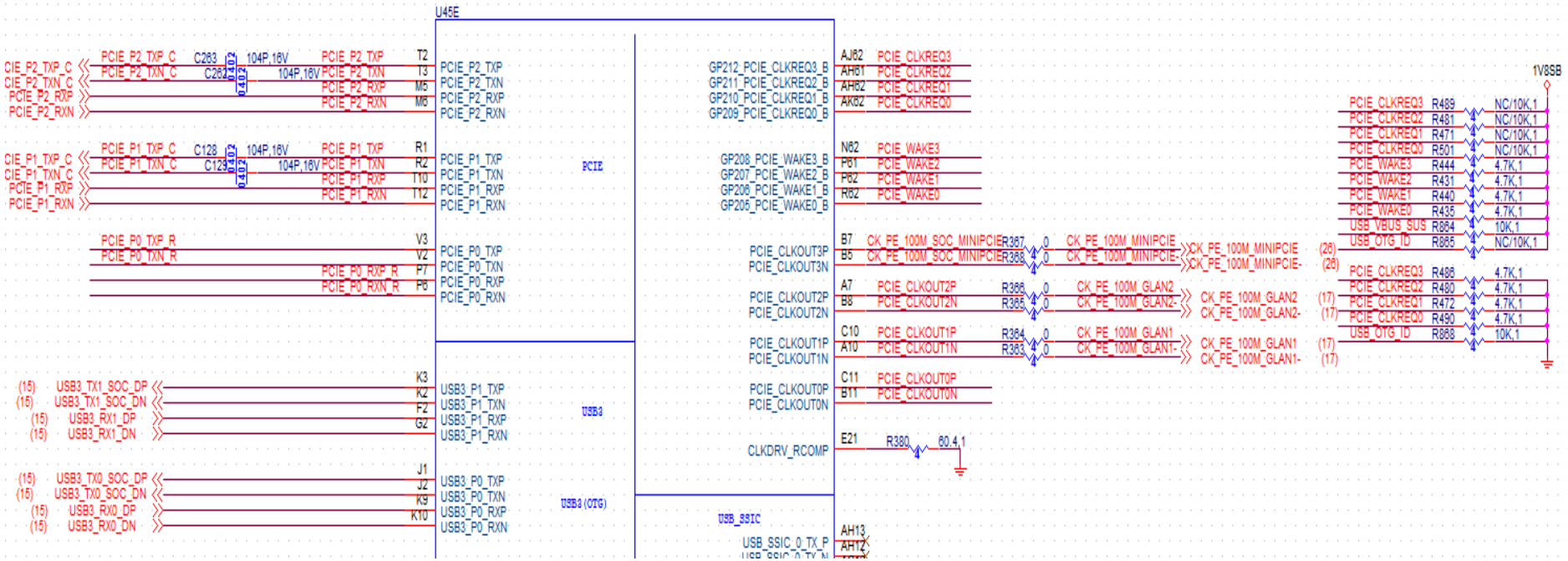
•Design Experience Sharing

Concept

To reduce components on LGA module Base on layout guide and check list to list the component must be close to CPU.



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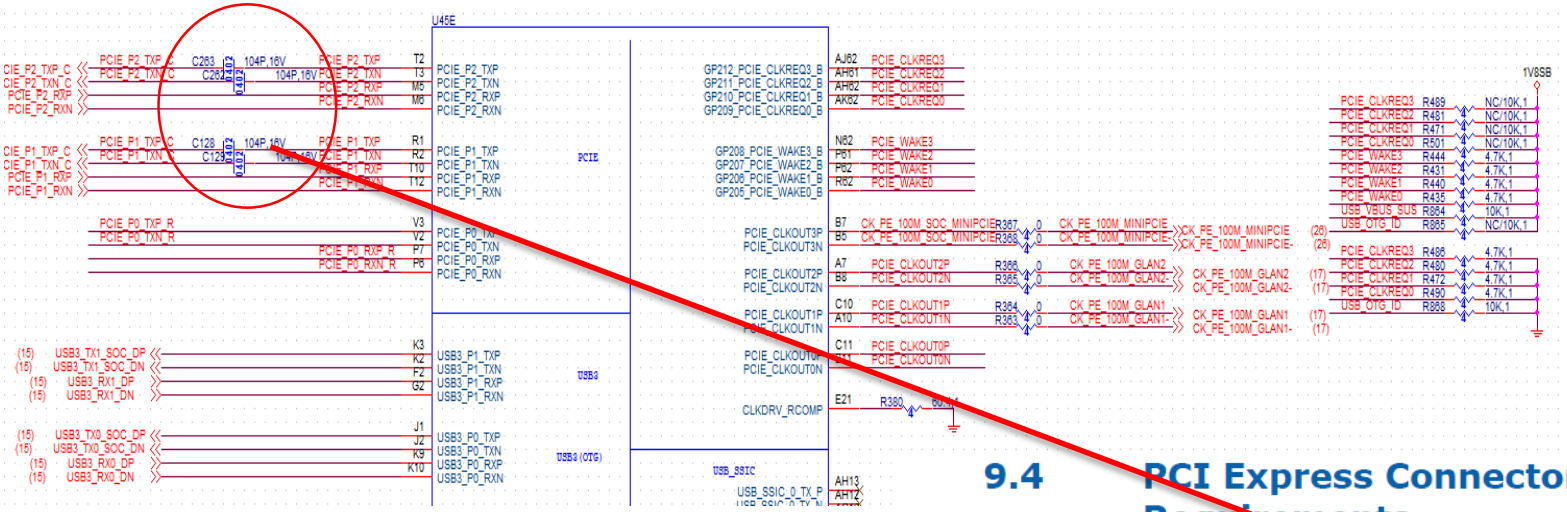
•Design Experience Sharing

- Ex. AC coupling capacitors must be close to CPU.



Layout check list

9.4 PCI Express Connector Trace Length Requirements

Signal Name	Signal Length	Notes	✓
PCIE_P[2:0]_TXP/N PCIE_P5_USB3_P2_TXP/N PCIE_P4_USB3_P3_TXP/N PCIE_P3_USB	0.2″ ≤ L_LA1_BO ≤ 0.5″ 0.5″ ≤ L_LA1_MAIN ≤ 2.5″ 0.5″ ≤ L_LB ≤ 2.5″ 0.5″ ≤ L_LC ≤ 2.5″ 0.5″ ≤ L_LD ≤ 1.0″ 1.2″ ≤ L_LE ≤ 3.0″	AC caps are recommended to be placed close to either PCIe* interface of SoC or PCIe* device side (avoid placing AC caps on mid-bus. 100nF AC caps recommended for 2.5 GT/s and 5 GT/s. For 5 GT/s main routing, we recommend the use of DSL to reduce crosstalk. For breakout (L_LA1_BO) and breakin (MS_BI) region route TX and RX on different layers to reduce crosstalk.	

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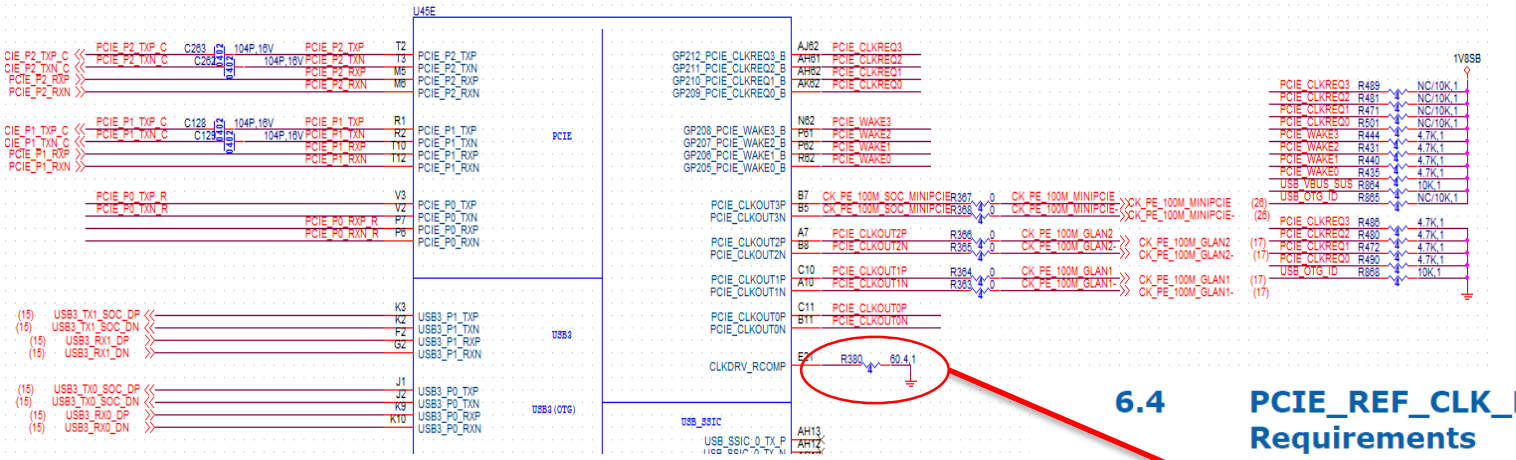
•Design Experience Sharing

- Ex. According to layout guide, it is better to keep RCOMP on LGA module.



Layout check list

6.4 PCIE_REF_CLK_RCOMP Trace Length Requirements

Signal Name	Signal Length	Notes	✓
PCIE_REF_CLK_RCOMP	B1 < 500 mils M1 < 1000 mils B1+M1 < 1000 mils Length Matching OSCIN-OSCOUT < 50 mils	No hard value for trace width and isolation spacing as long as DCR is met NOTES: • Must maintain low DC resistance routing (<0.5 Ω) • A recommendation is to route the signal to 4-8mils trace width with <1000 mils to meet DCR	

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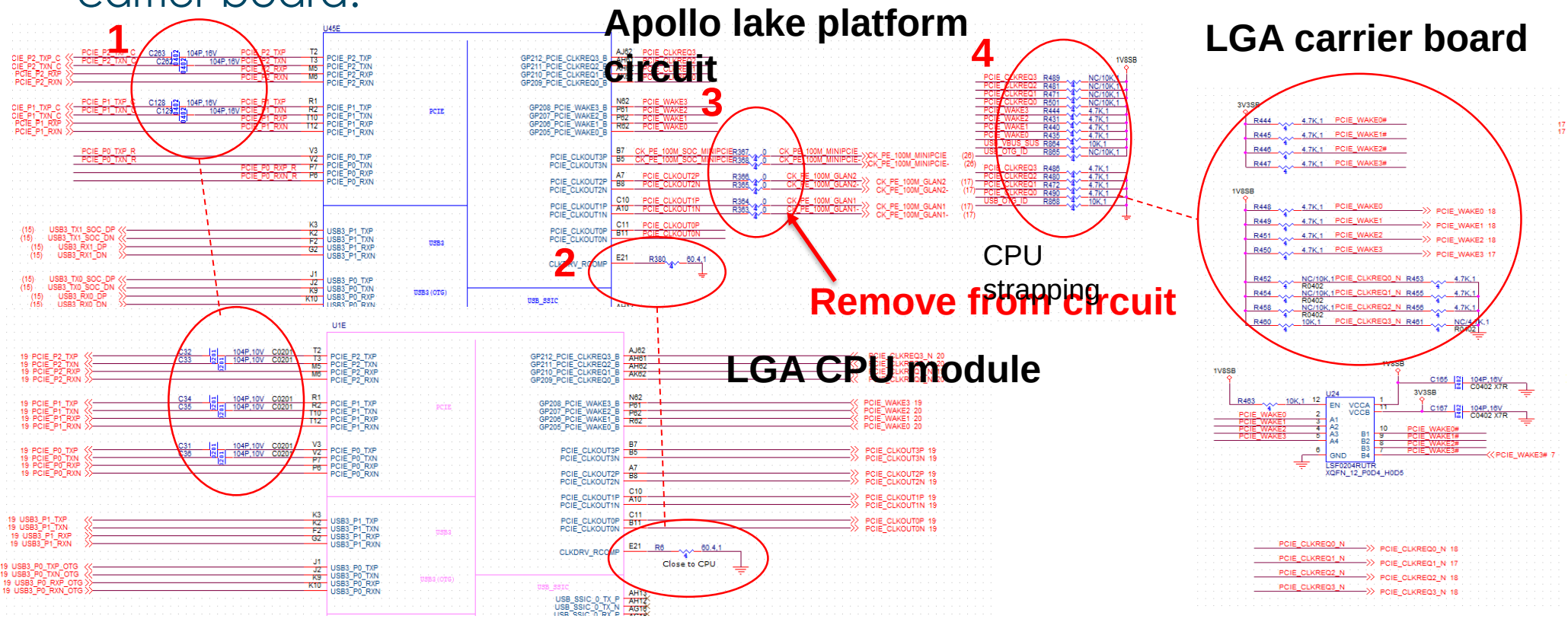
•Design Experience Sharing

- Ex. CPU strappings allow longer trace length and more vias, move to carrier board.



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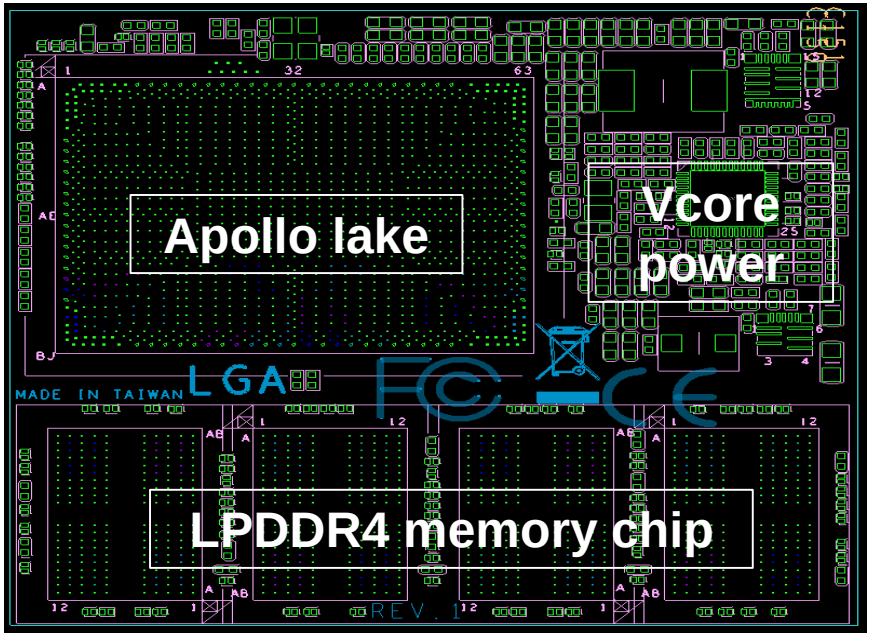
•Design Experience Sharing

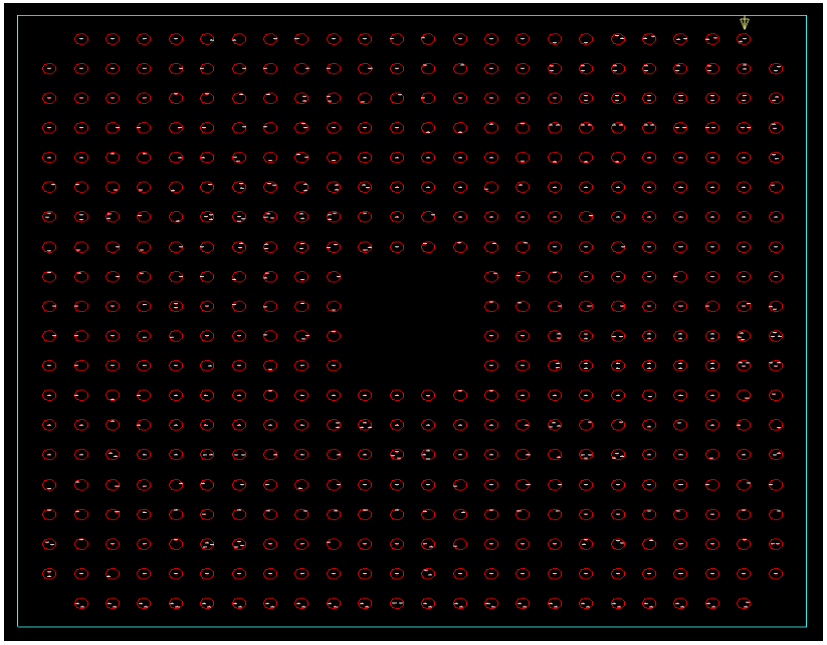
Final placement

After reducing, all components can be on one side

Top view



Bottom view



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• Design Experience Sharing

- Pin out definition concept

1. Define current of per pin.
2. Define power pin base on power budget.
3. Define total signals pin
4. Base on Top size placement to define pin out

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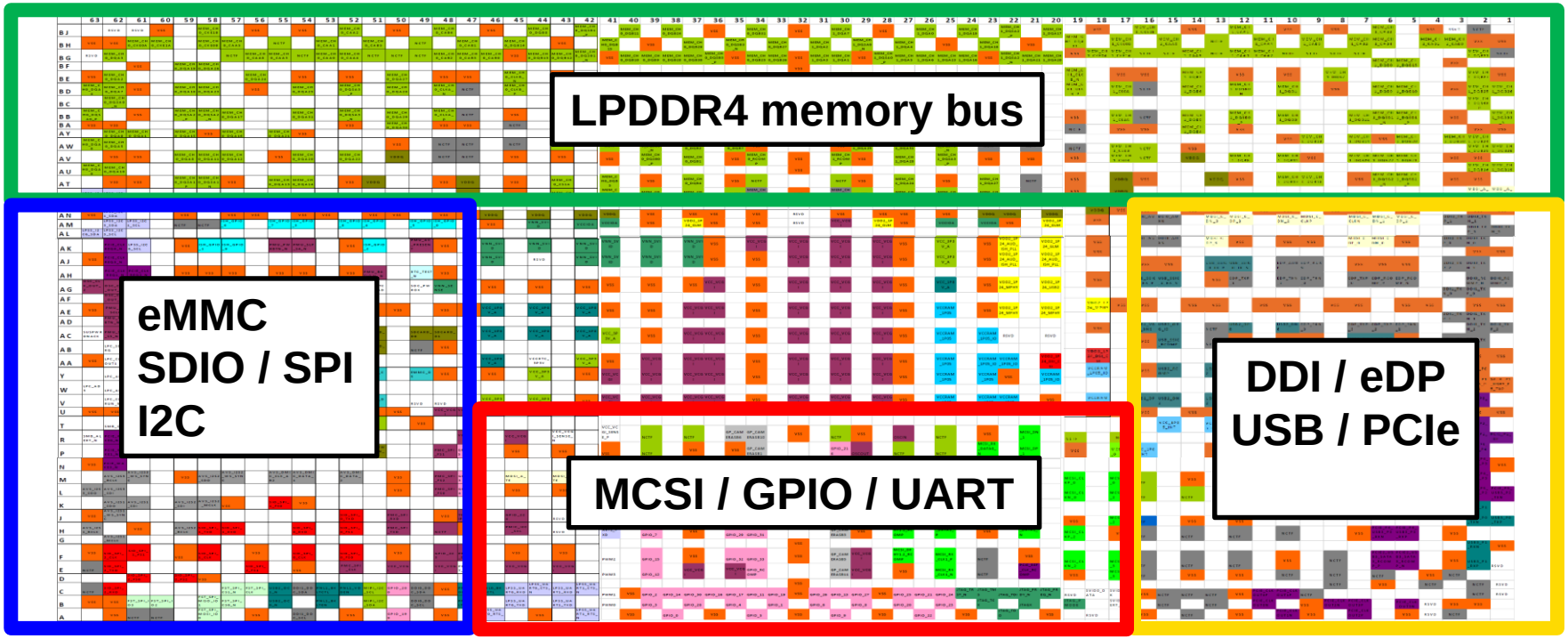
• Design Experience Sharing

- Define CPU pin out



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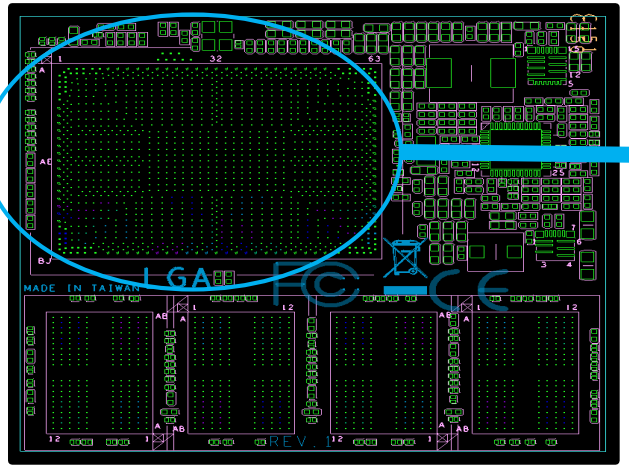
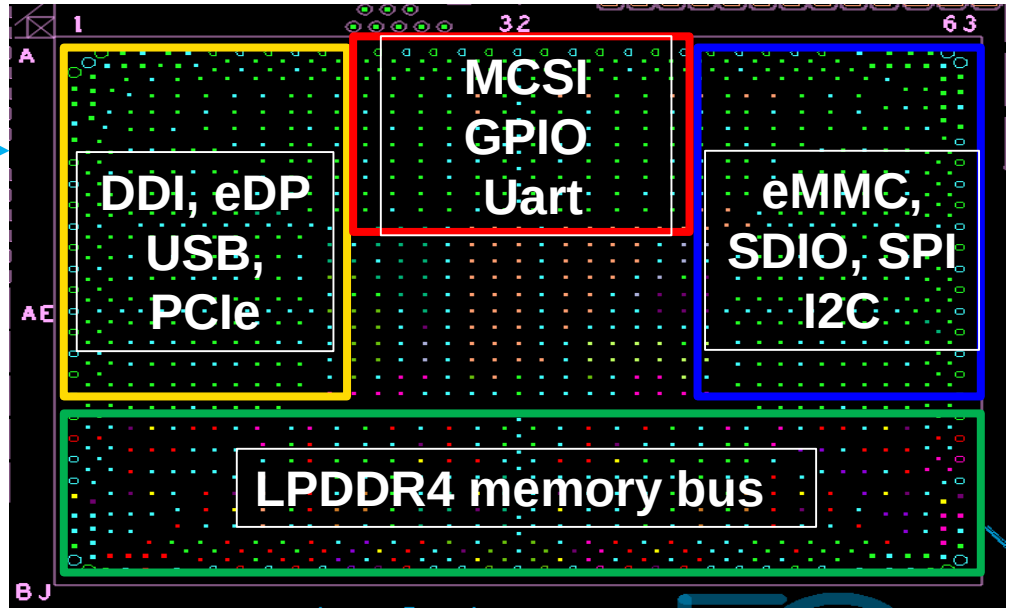
• Design Experience Sharing

- Mapping CPU pin out to layout footprint

LGA CPU module Top view



CPU Top view



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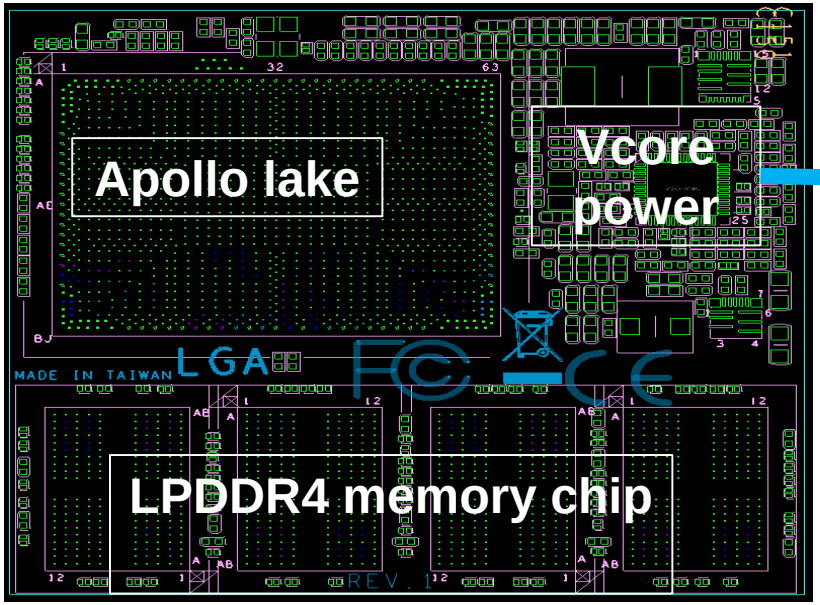
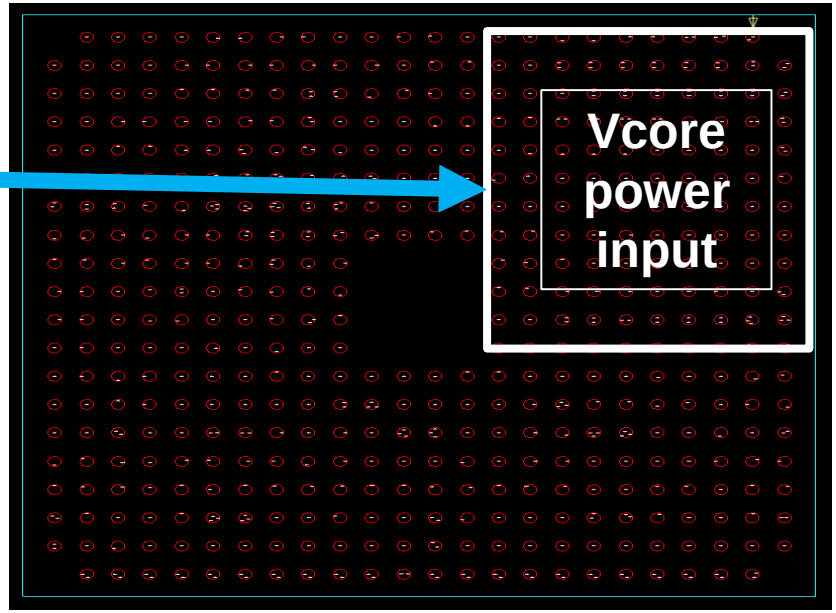
• Design Experience Sharing

- Define power area of Vcore power

LGA CPU module top view



LGA CPU module bot view



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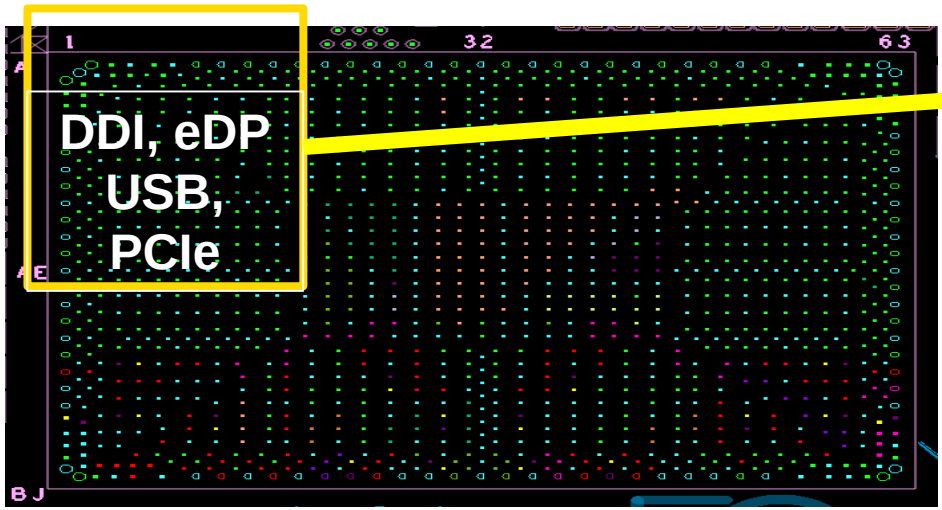
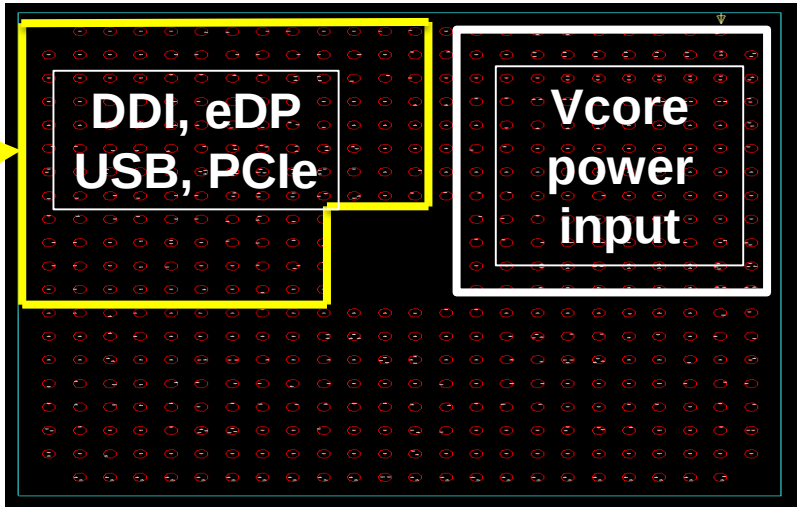
• Design Experience Sharing

- Define high speed signals area, it needs to be as close to CPU as possible

CPU Top view



LGA CPU module bot view



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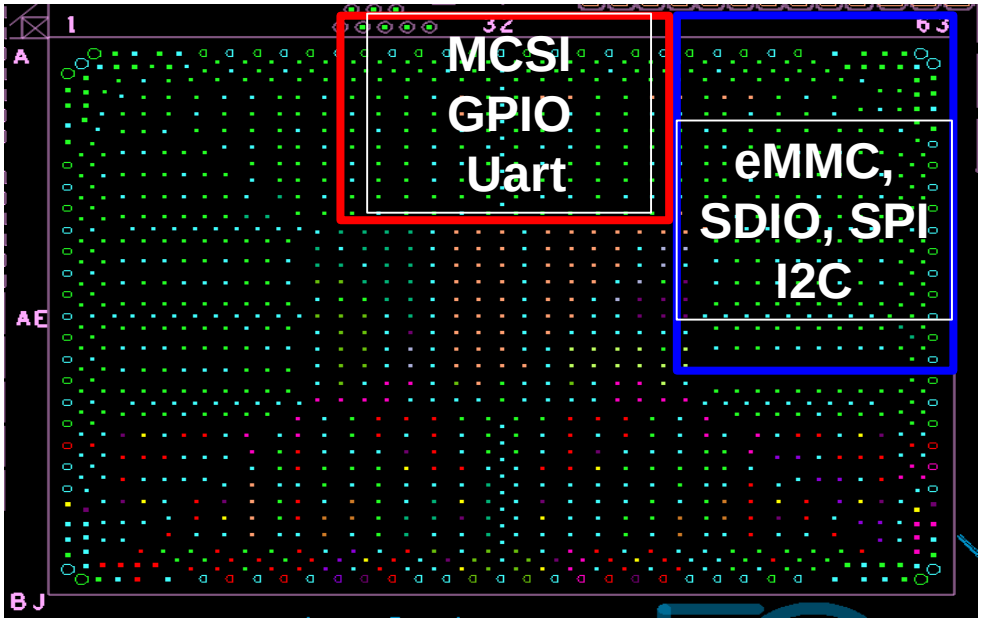
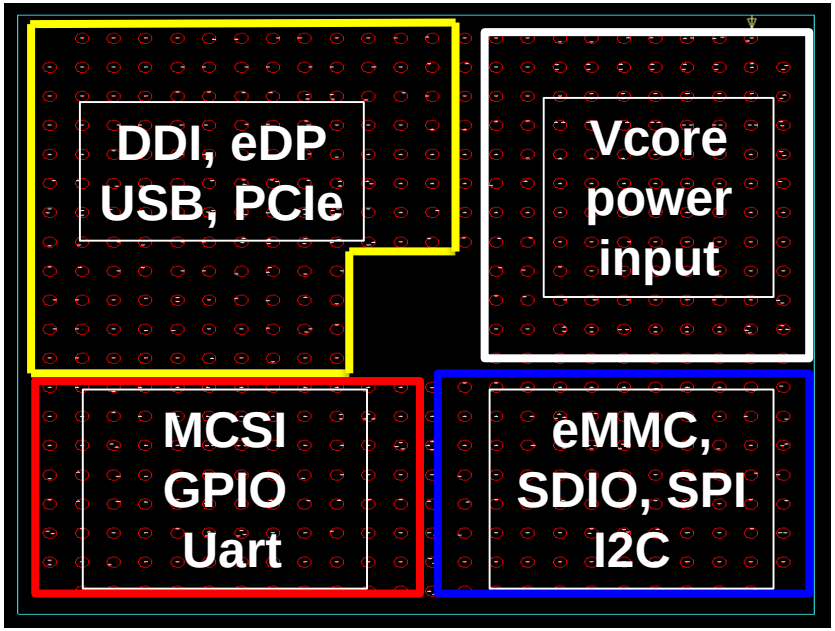
• Design Experience Sharing

- Define low speed signals area

CPU Top view



LGA CPU module bot view



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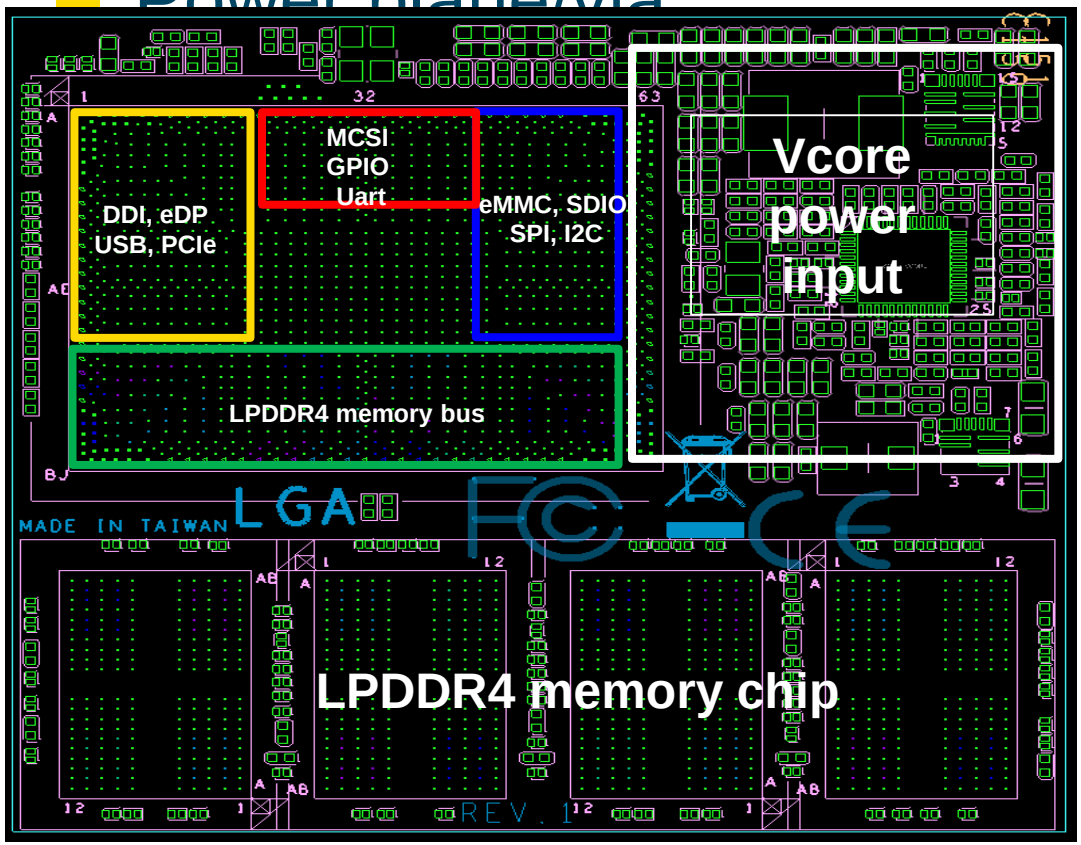
•Layout Experience Sharing

- Power plane/via



- Estimate power and signal routing and design power plane base on placement.

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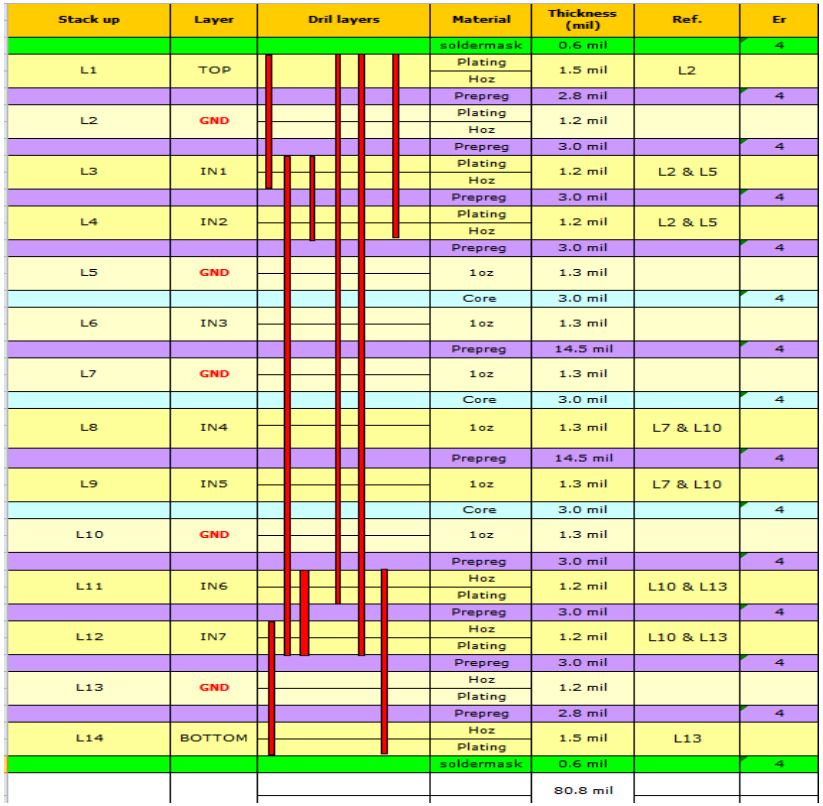
Stack up of HDI



Stack up	Layer	Dril layers	Material	Thickness (mil)	Ref.	Er
			soldermask	0.6 mil		4
L1	TOP		Plating Hoz	1.5 mil	L2	
			Prepreg	2.8 mil		4
L2	GND		Plating Hoz	1.2 mil		
			Prepreg	3.0 mil		4
L3	IN1		Plating Hoz	1.2 mil	L2 & L5	
			Prepreg	3.0 mil		4
L4	IN2		Plating Hoz	1.2 mil	L2 & L5	
			Prepreg	3.0 mil		4
L5	GND		1oz	1.3 mil		
			Core	3.0 mil		4
L6	IN3		1oz	1.3 mil		
			Prepreg	14.5 mil		4
L7	GND		1oz	1.3 mil		
			Core	3.0 mil		4
L8	IN4		1oz	1.3 mil	L7 & L10	
			Prepreg	14.5 mil		4
L9	IN5		1oz	1.3 mil	L7 & L10	
			Core	3.0 mil		4
L10	GND		1oz	1.3 mil		
			Prepreg	3.0 mil		4
L11	IN6		Hoz Plating	1.2 mil	L10 & L13	
			Prepreg	3.0 mil		4
L12	IN7		Hoz Plating	1.2 mil	L10 & L13	
			Prepreg	3.0 mil		4
L13	GND		Hoz Plating	1.2 mil		
			Prepreg	2.8 mil		4
L14	BOTTOM		Hoz Plating	1.5 mil	L13	
			soldermask	0.6 mil		4
				80.8 mil		

- To increase routing space, stack up is HDI 14 layers
- To make sure signals quality, each layer is reference to GND layer
- Power plane is shared with TOP, BOTTOM, and INER layer
  - TOP (L1) – IN1 (L3)
  - TOP (L1) – IN2 (L4)
  - TOP (L1) – IN6 (L11)
  - TOP (L1) – IN7 (L12)
  - IN1 (L3) – IN2 (L4)
  - IN1 (L3) – IN7 (L12)
  - IN6 (L11) – IN7 (L12))
  - IN6 (L11) – BOTTOM (L14)
  - IN7 (L12) – BOTTOM (L14)

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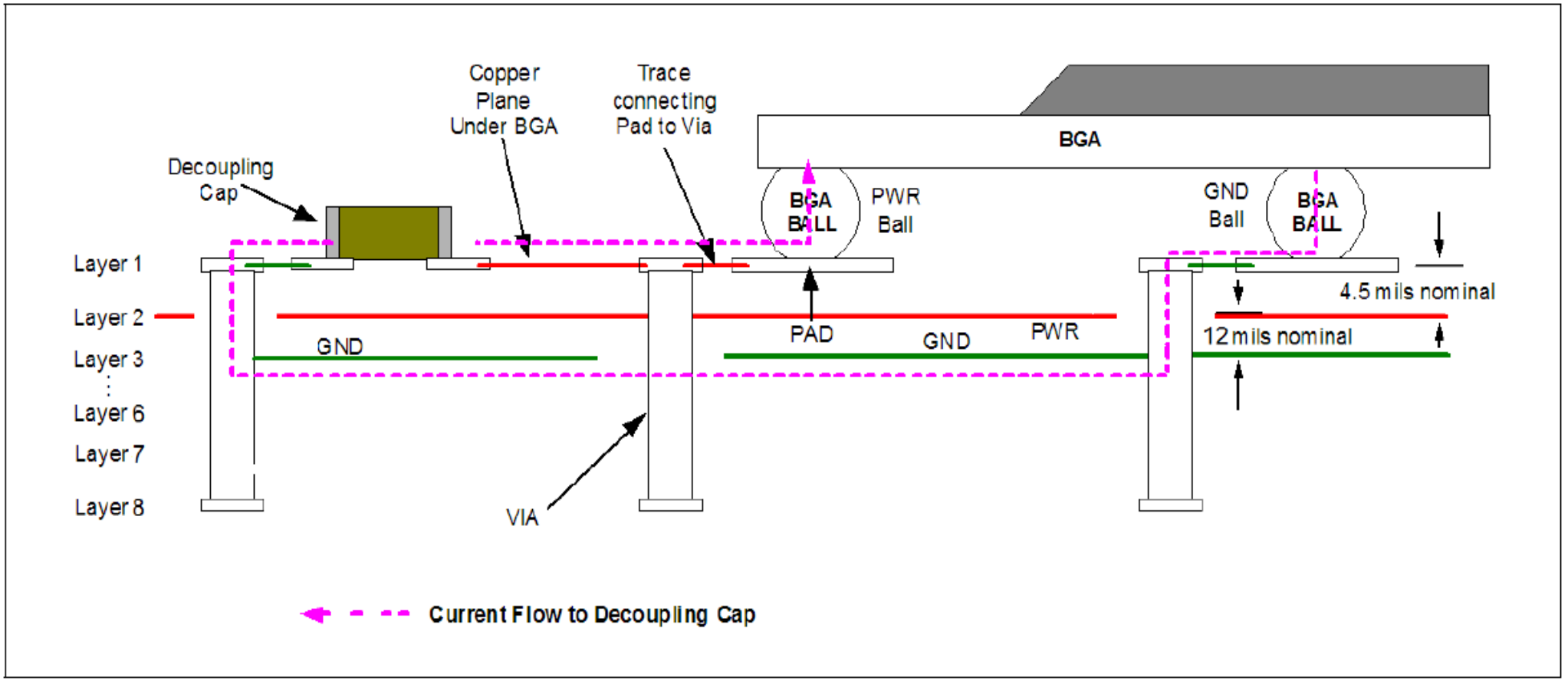
• Return Path

- Edge decoupling capacitor placement)



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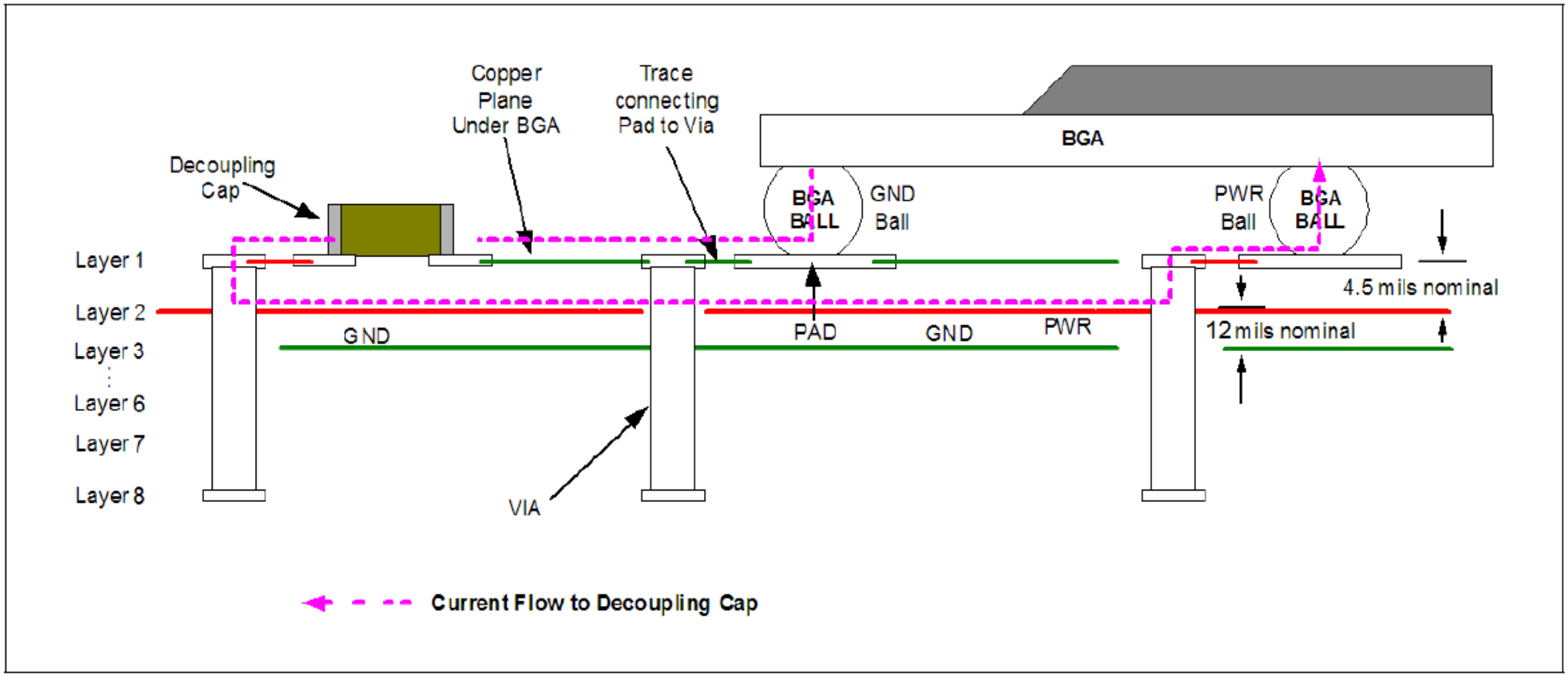
• Return Path

- Minimized loop inductance example runway



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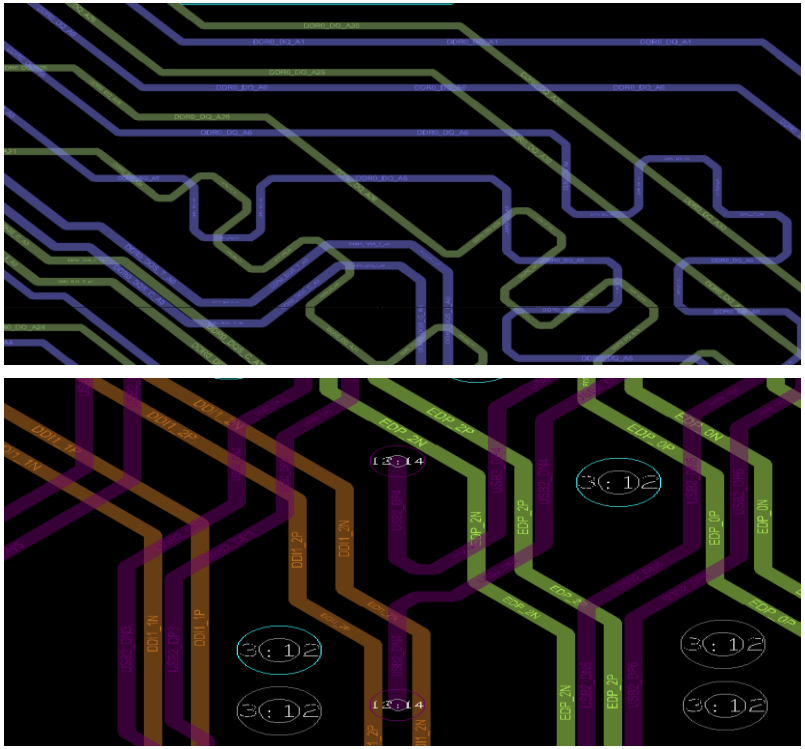
•Layout Experience Sharing

- Dual stripline



- To avoid crosstalk, high speed signals in nearby layers should be shift.

Ex. DDR, USB, SATA, eDP, DDI, PCIe, MIPI-CSI

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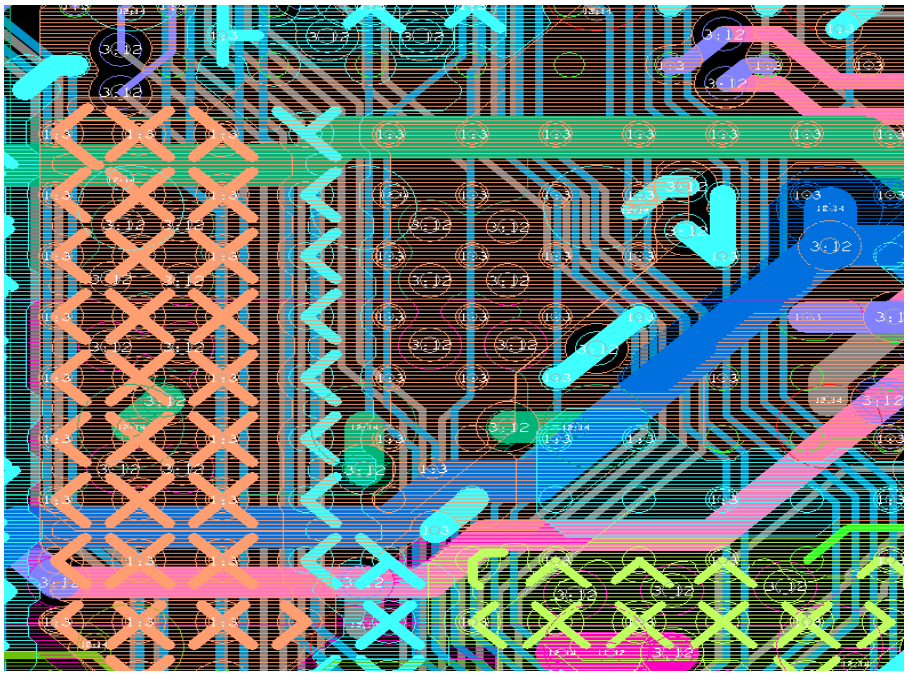
- Power plane/via



- High density layout design is difficult to implement via for power plane and return path. To reduce the difficulty, choose Layer 3 to be default power layer.

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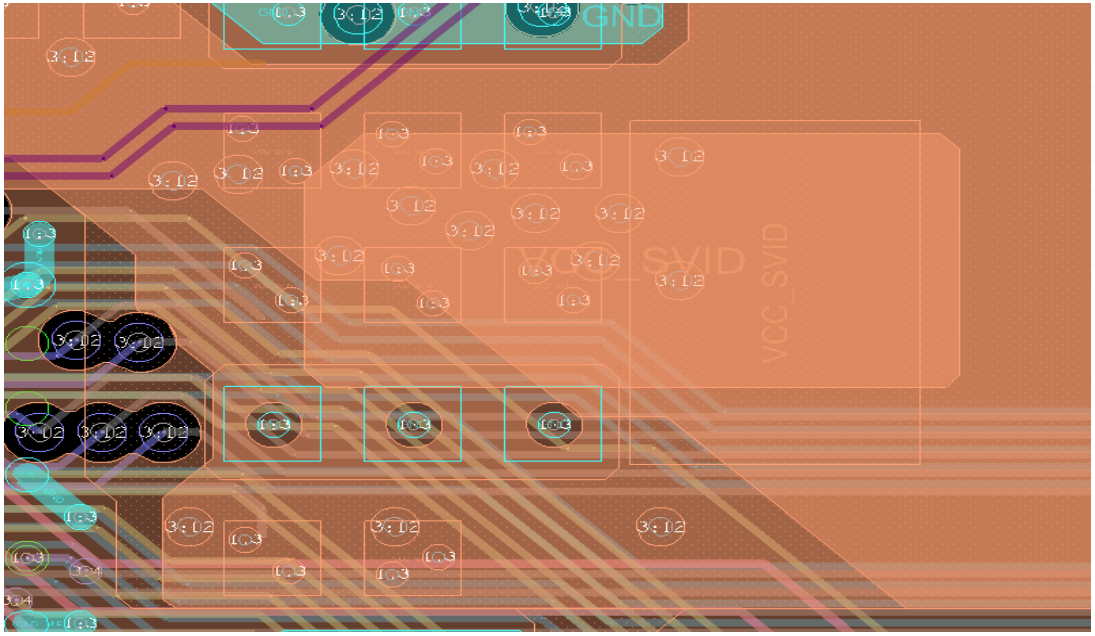
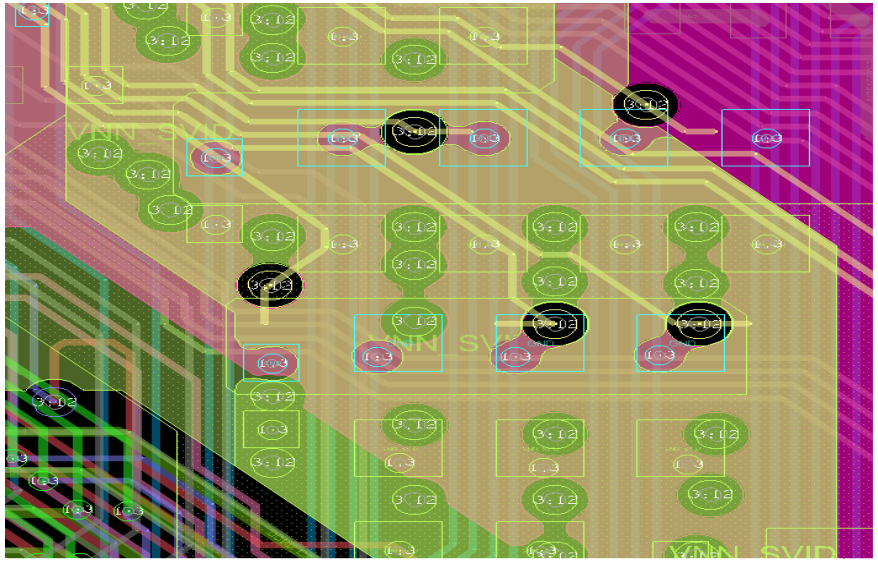
•Layout Experience Sharing

- Power plane/via



➢ Ex. Power plane L3 to I12



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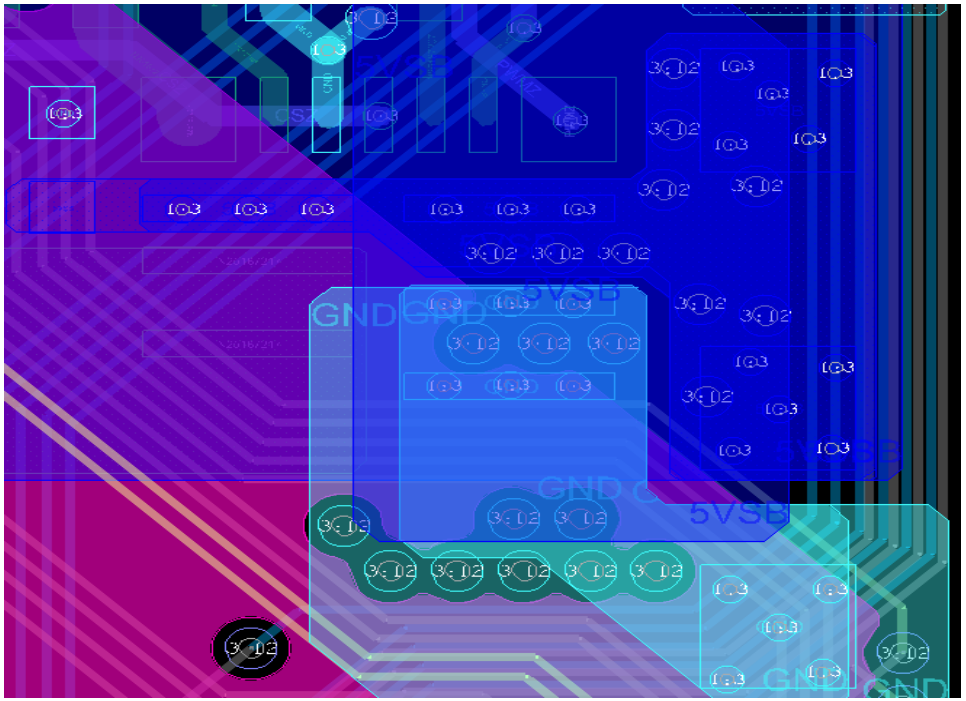
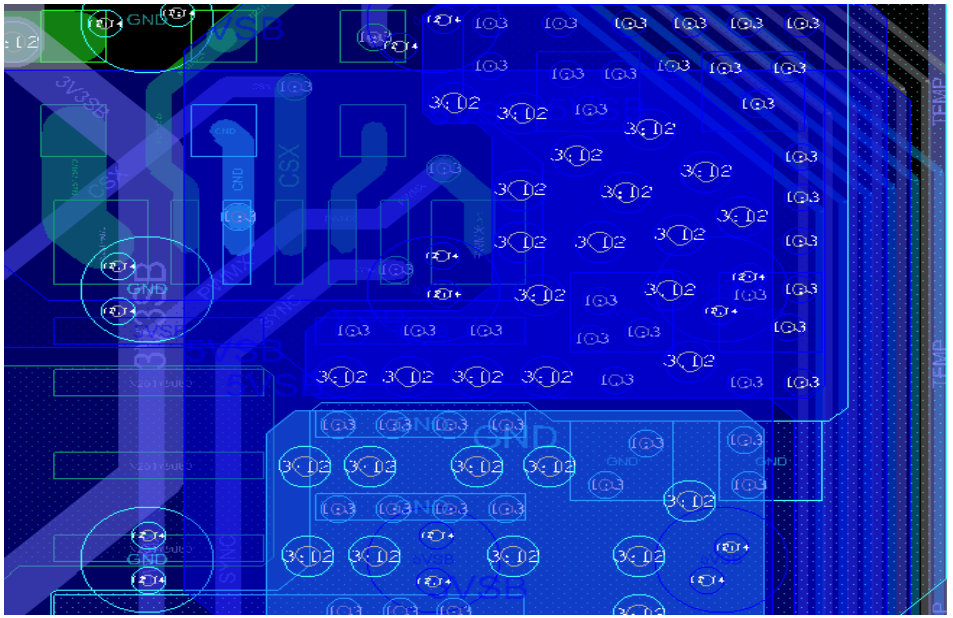
- Power plane/via



- Ex. Power plane L1 to L3 and L3 to L12



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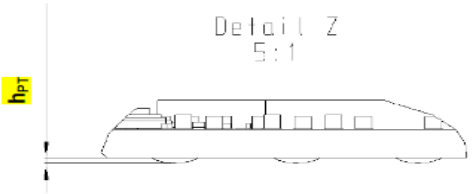
• Manufacturing Experience Sharing

Specification for pre soldering of LGA

A soldering depot on all LGA connection lands has to be applied.

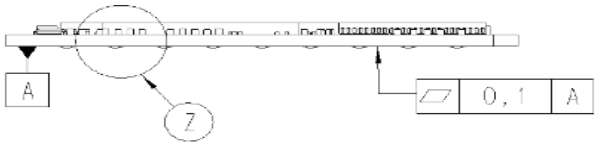
This is required to improve soldering connection of LGA to motherboard.

- Material: SAC305 alloy or equivalent, no low silver alloy
- Final Solder deposit height Hpt: **200 - 280µm** (First)
- Final Solder deposit height Hpt: **200 - 300µm** (Second)



Additional requirements:

- Void rate max. 25% in X-ray image of any pre soldered LGA-land (acc. IPC A610)
- No Flux residues permitted (cleaning process required, usage of water soluble solder paste recommended)
- PCB-finish must be able to resist cleaning process



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Architecting the Next Edge Generation of Embedded IOT Application

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•Combination of Edge AI Technology

Application ready

Computer vision

Voice control

Cloud based & off-line speech recognition

amazon alexa

Google Assistant SDK

Acceleration & off-load

Intel® processor graphics

Intel® Movidius™ Myriad™ VPU

Intel Atom® and Intel® Core™

Intel® Stratix® 10 FPGA

H/W dedicated core

Intel® OpenVINO™

Intel® Movidius™ Myriad™ VPU SDK

SW optimizer

Hardware platform

Panel PC

Box PC

Industrial SBC

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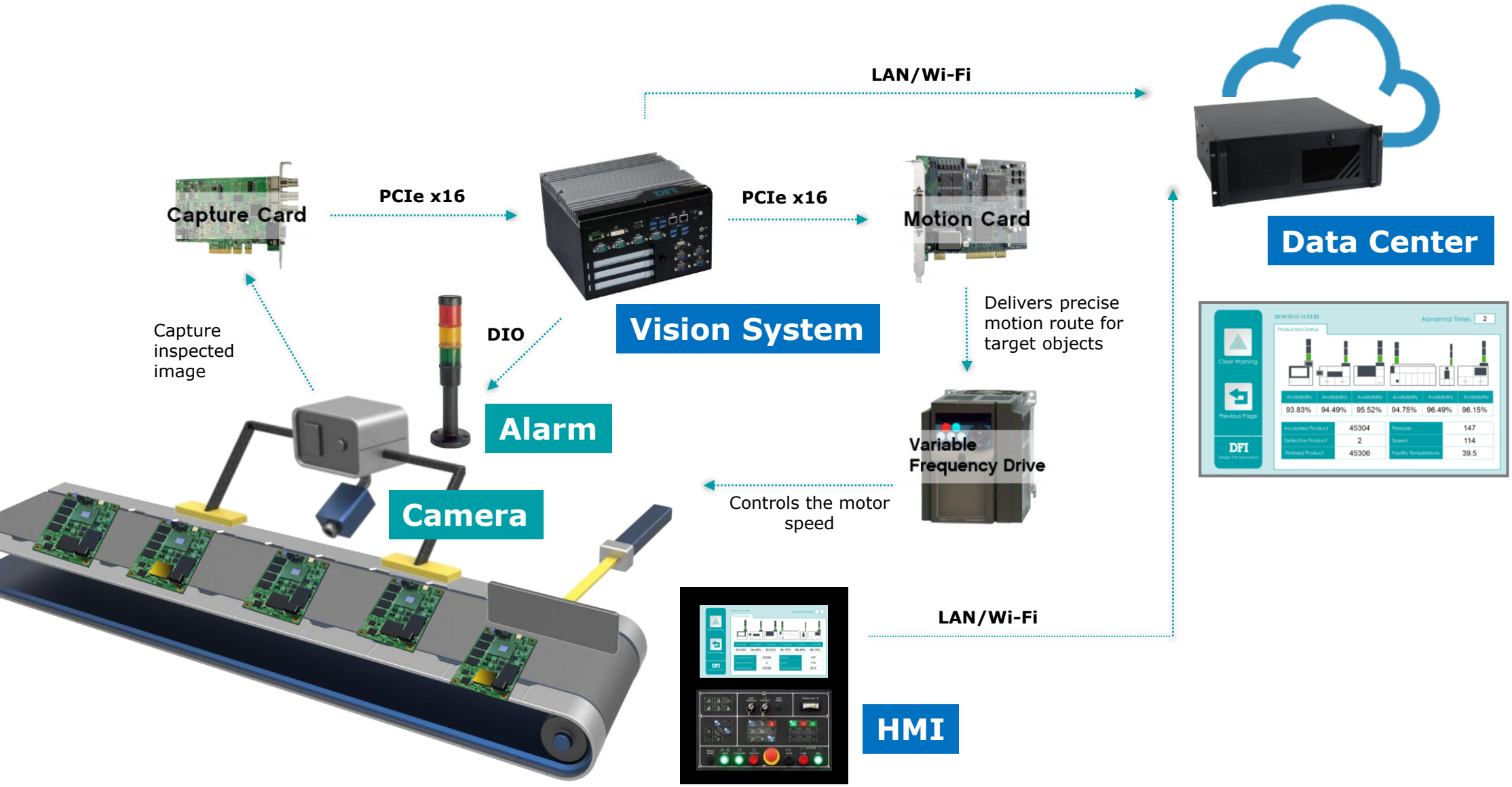
• Machine Vision



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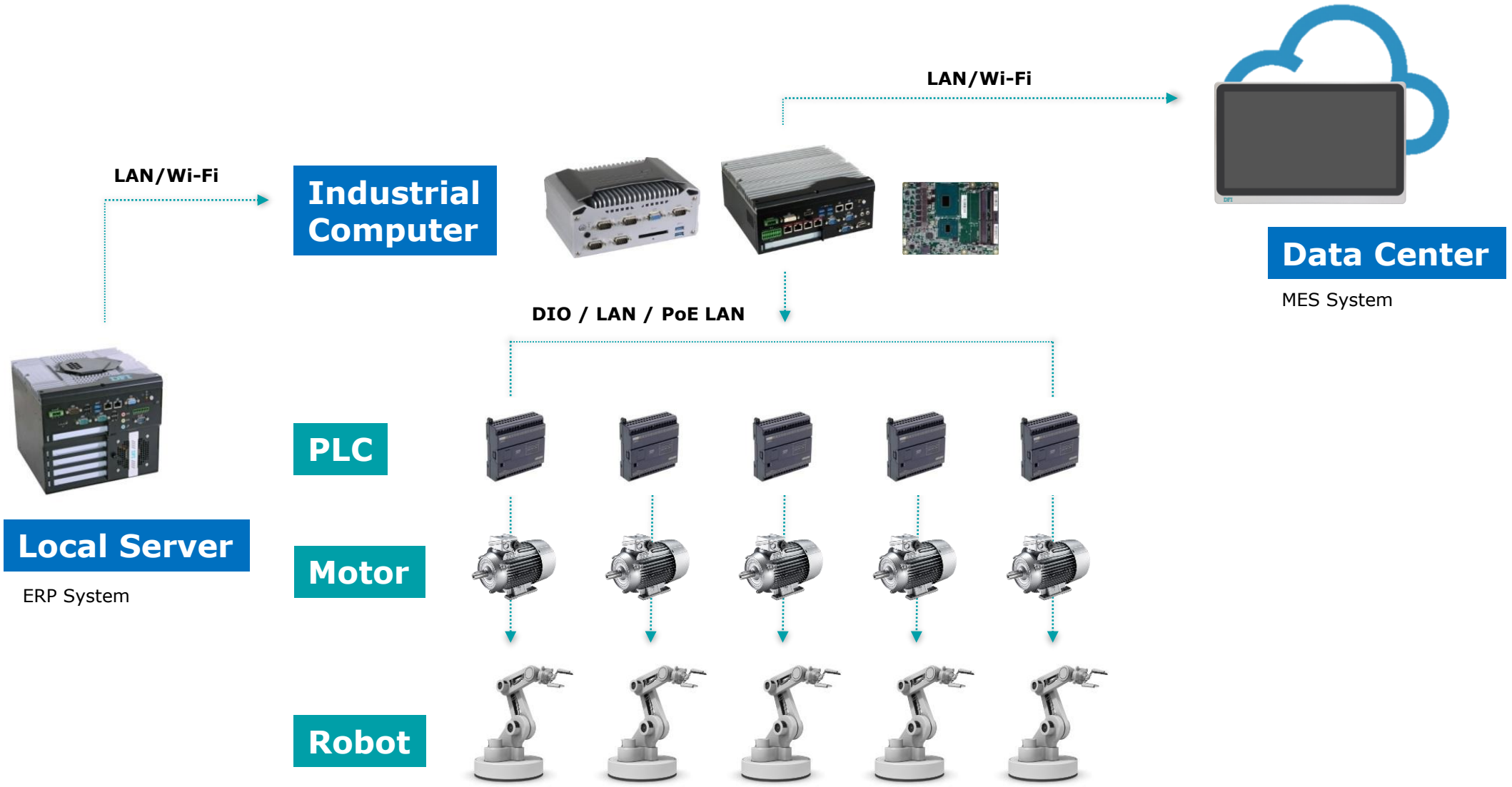
• Robot Control



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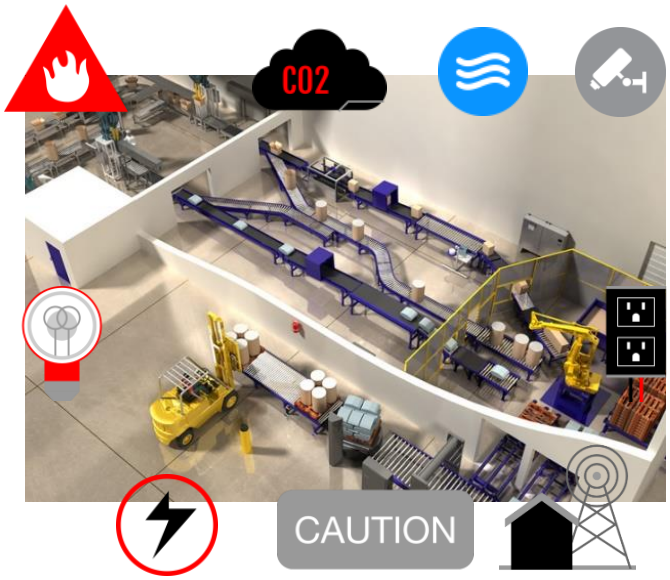
• Environment Monitoring



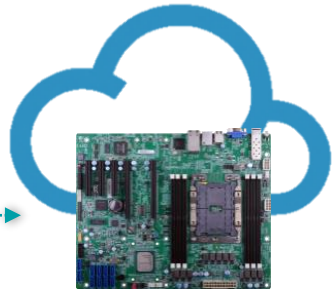
Camera

Shoot video and capture image in the factory

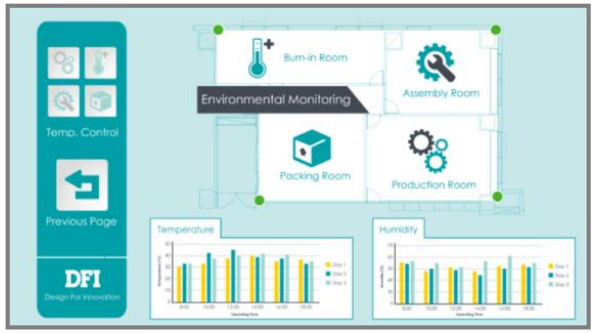
Wi-Fi / LTE / GSM/ LoRa

IoT Gateway

LAN/Wi-Fi



Server



Sensors

Collect environmental info of temperature, humidity, airflow, smoke and water

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Together from Idea to Solution

Intemo
Innovative Technology in Motion

DFI

Intemo and DFI share the same vision.

Intemo does not only have a lot of knowledge in embedded vertical markets, but also flexibility with great quality support to the client.

The synergy between DFI and Intemo not only provide a tailor-made solutions with long life support but also well-round service for your core business.

THANK YOU! See you at Booth No.2

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