JTAG Interface

Bespaar geld en tijd door tijdens het schema ontwerp al te visualiseren wat de test - en programmeer mogelijkheden zijn via de JTAG interface

JTAG Technologies B.V.

Peter van den Eijnden

peter@jtag.nl

Boundary-scan

Testing HW without firmware and without test pads

IEEE Std 1149.1 IEEE Standard Test Access Port and Boundary-Scan Architecture

Standard since 1990 and still evolving

A.k.a. JTAG (Joint Test Action Group)

Boundary-scan

At the basis boundary-scan is about

testing the presence of connections between components:

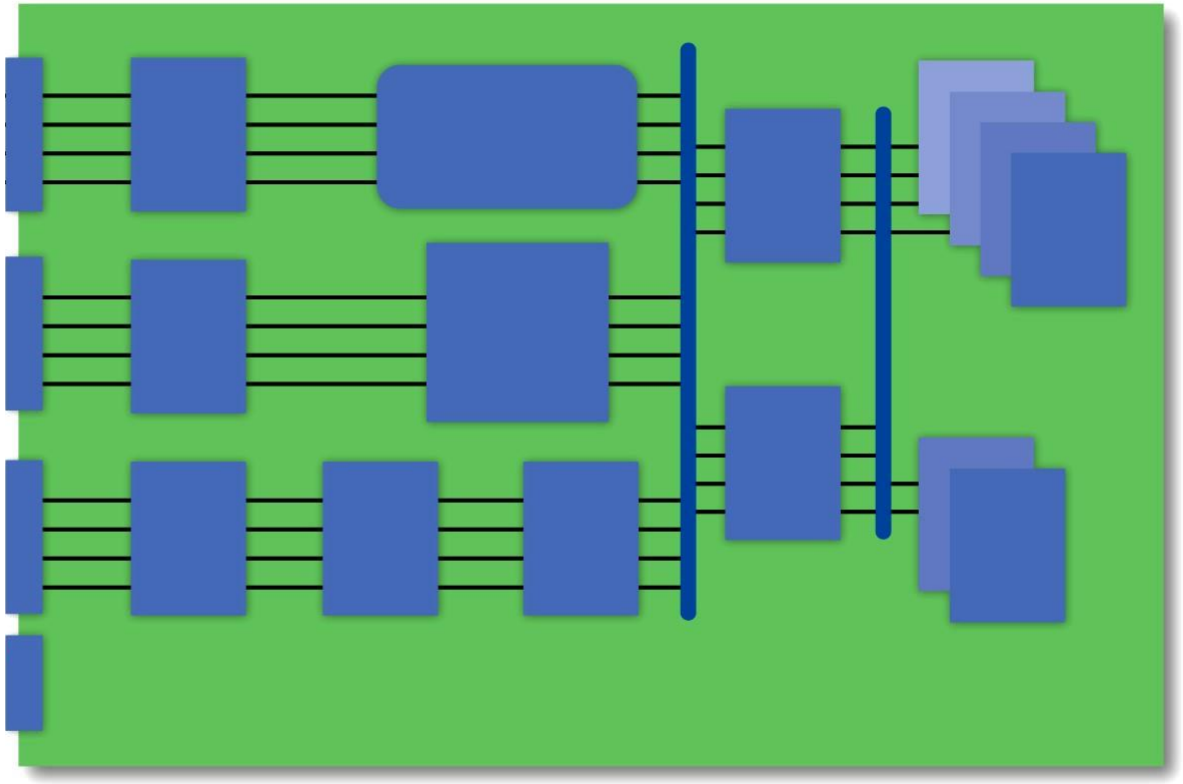
- At board level: connections between chips
- At module level: connections between boards
- At system level: connections between modules

Using (test) resources embedded in chips

Boundary-scan

Boundary-scan is also used for

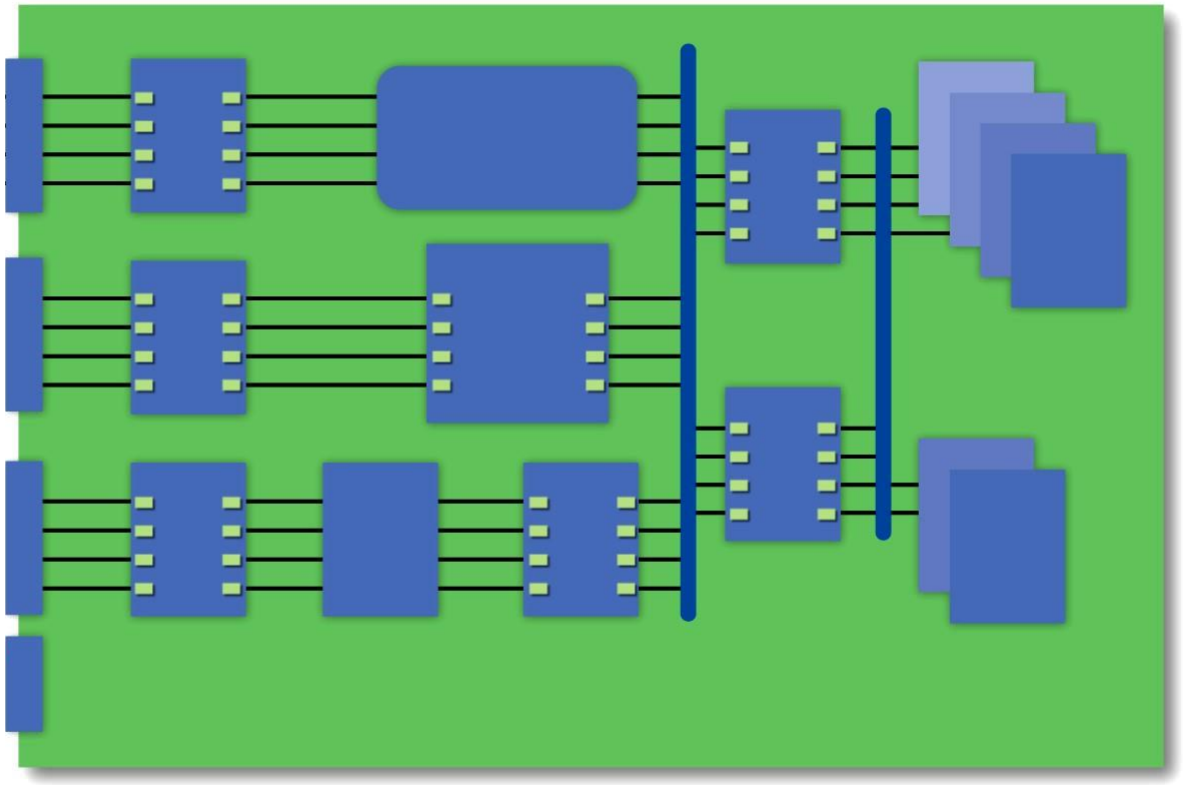
- In-system device programming
  (cPLD's, FPGA's, Microcontrollers, Flash memories and many special devices)
- Software debugging
- Others: Fine-tuning circuits, reading built-in sensors (eg temp), etc.



Devices Connections

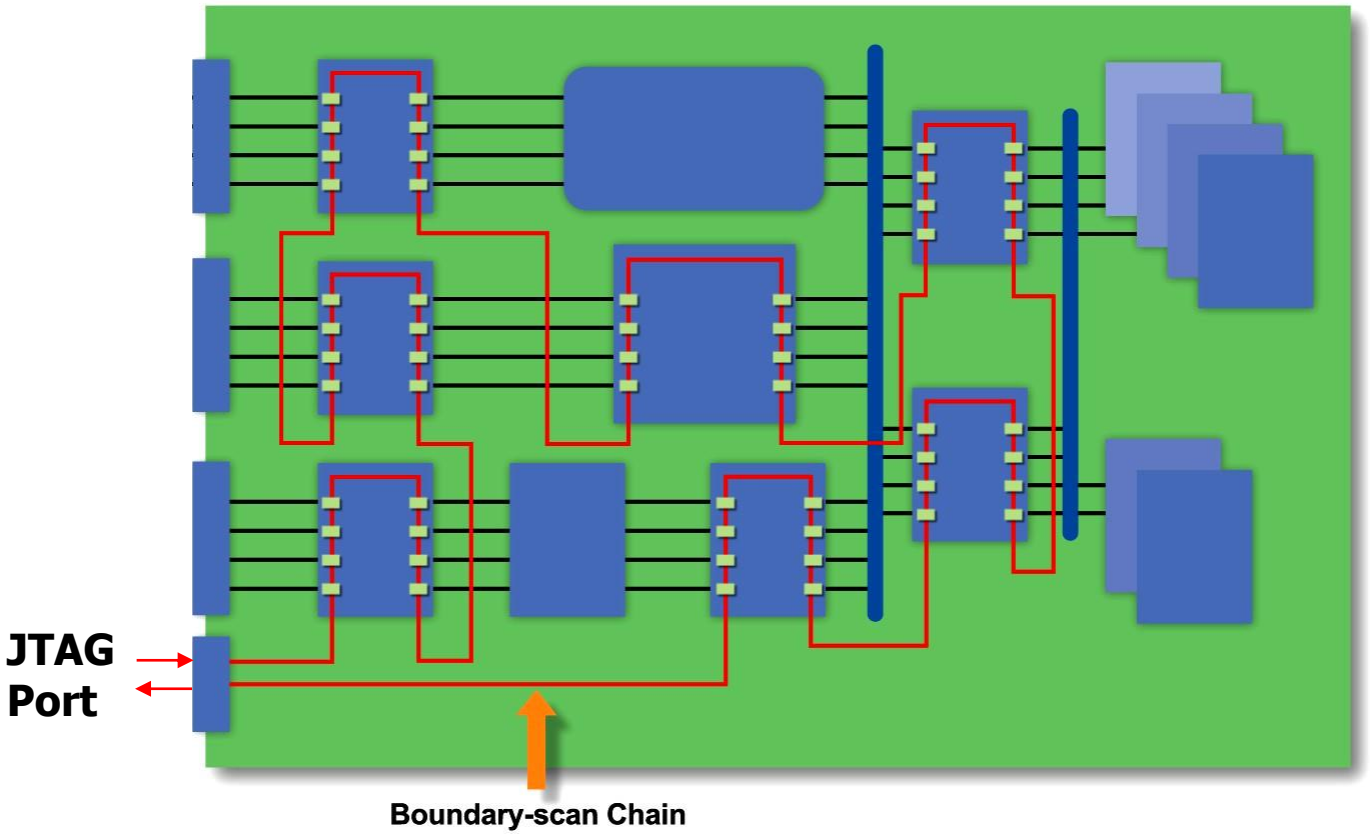
Check

- Presence
- Value
- Polarity
- Solder



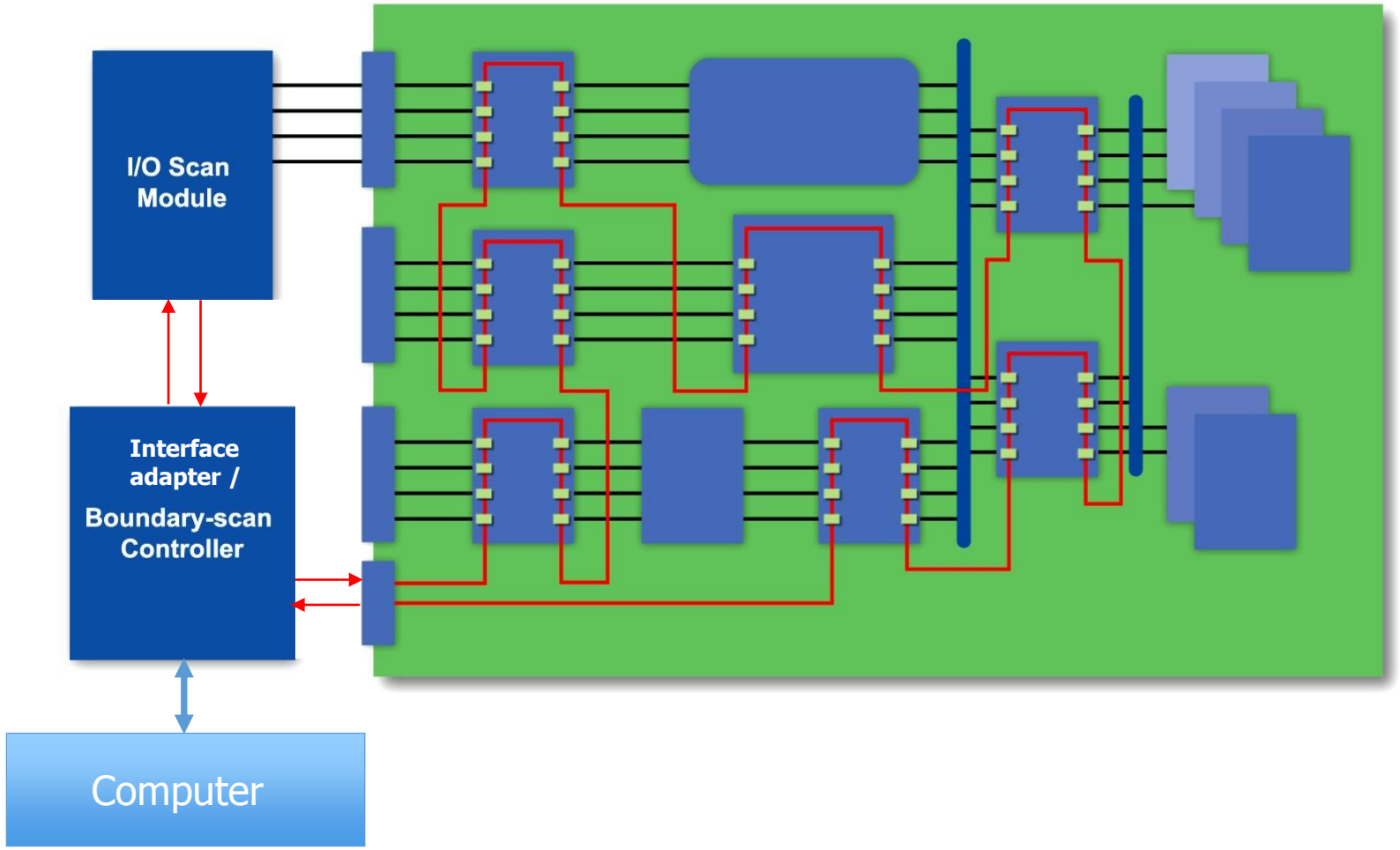
Control and monitor bscan device pins independent of chip's functionality

Devices Connections Boundary-scan cells



Access
all bscan pins
through
a serial chain

Devices Connections Boundary-scan cells



JTAG Capabilities

- ✓ Test Interconnections between Bscan pins
- ✓ Test through Connectors
- ✓ Resistor presence: Serial, Pull-up, Pull down
- ✓ Test LVDS connections
- ✓ Emulative testing
- ✓ At speed memory interconnection test
- ✓ Using Embedded instruments
- ✓ ISP of Flash memories, uC's, FPGA's, cPLD's, special devices

What can be used on your design?

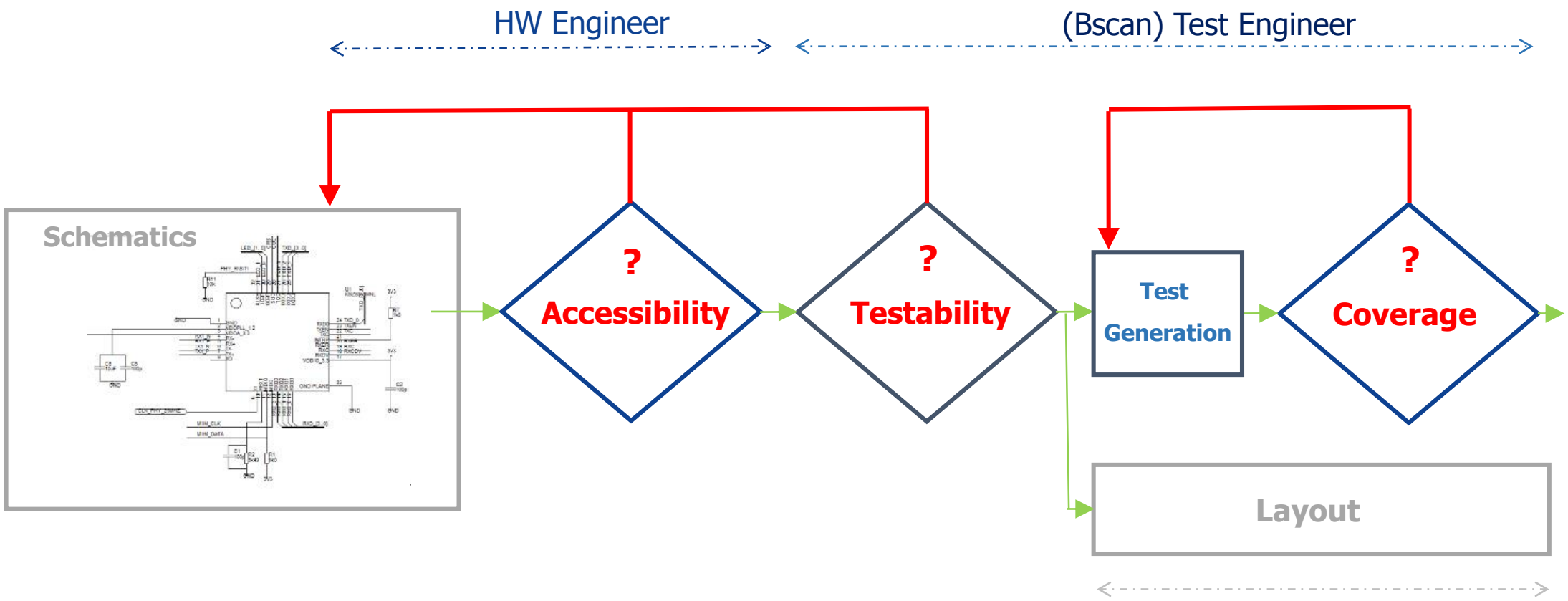
What does it take?

Bscan devices & DfT

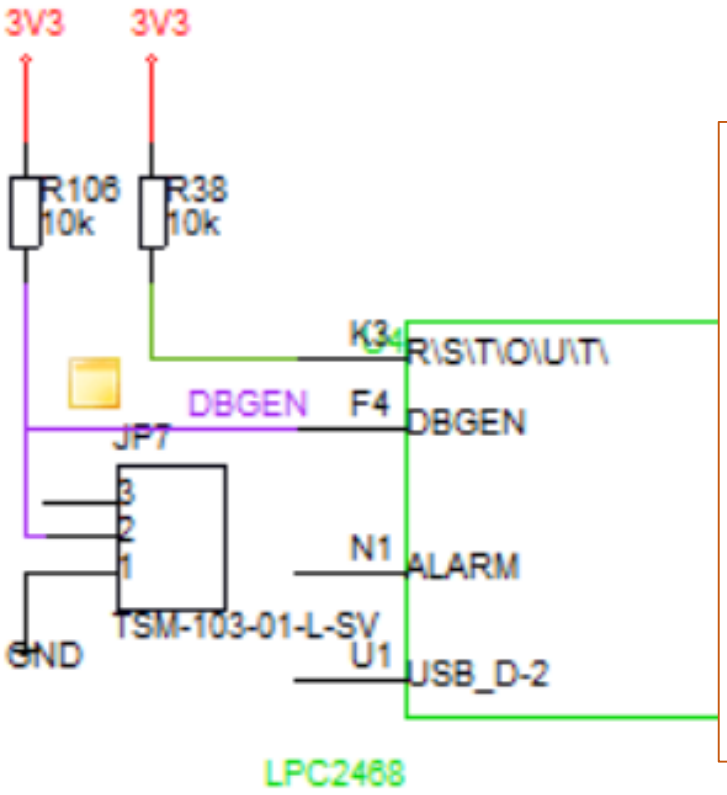
Definitions

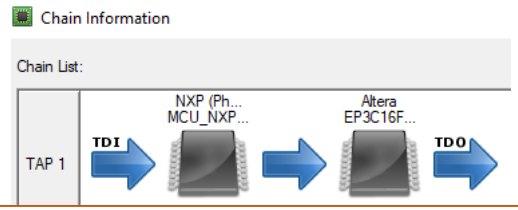
1. Accessibility via:
    - Boundary-Scan
    - Connector Pins
    - Test Points
2. Testability
    - Accessible, but testable? Drive and sense on a net?
    - Is it save to drive a value on an accessible net?
3. Coverage
    - Which potential production failures (Pres, Val, Pol, Sol) will be found by the total test strategy

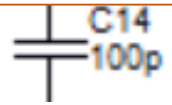
DFT analysis during schematic stage



Check Test possibilities during schematic stage







How?

- Test development house
- Test Analysis tool for various EDA tools

Test Points ?

Only If schematic analysis shows that you have

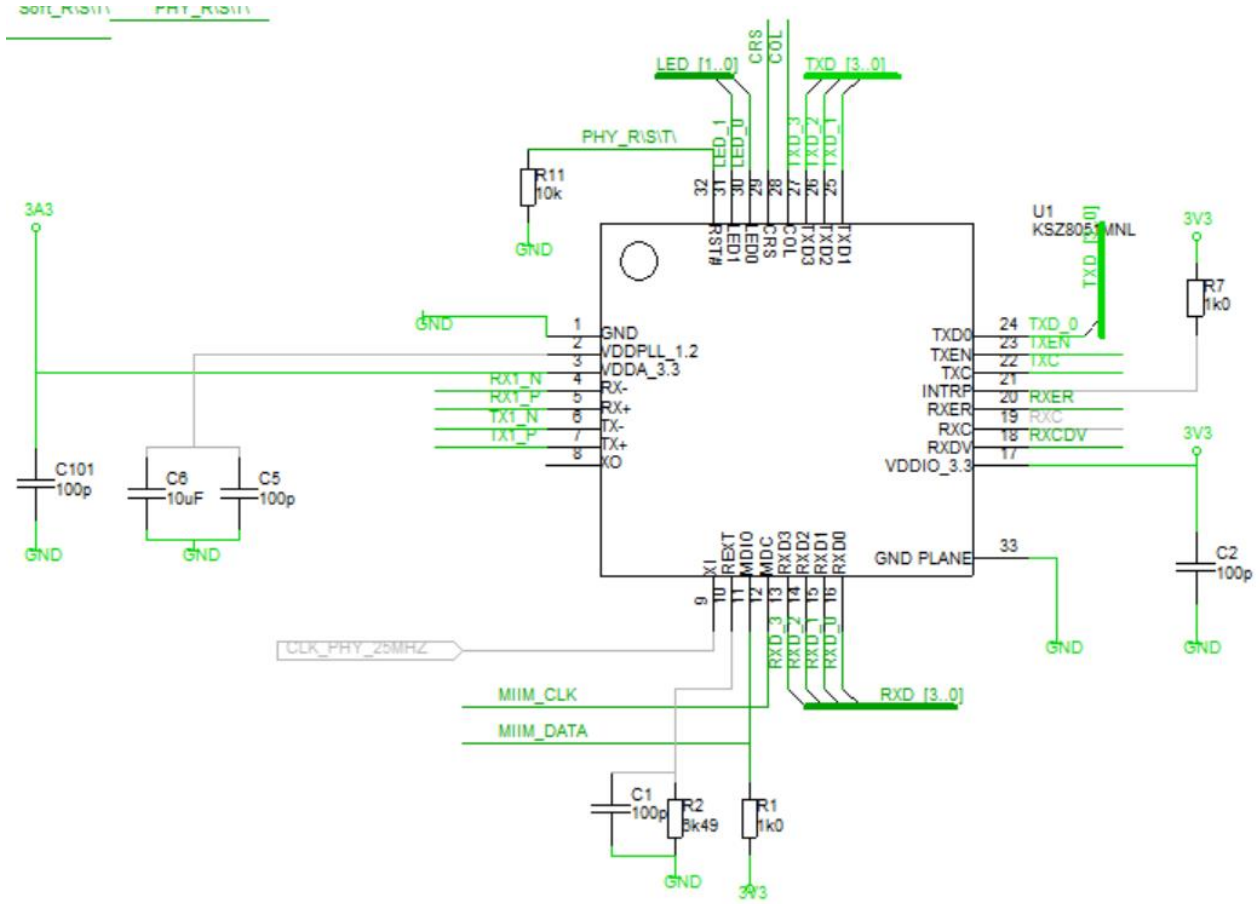
- a too low testability
- a too slow programming process

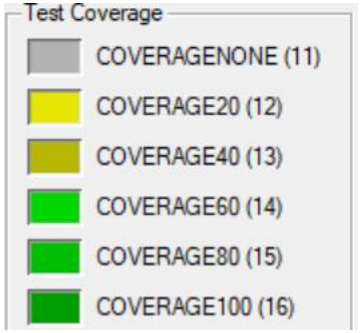
If so, then add to your schematics:

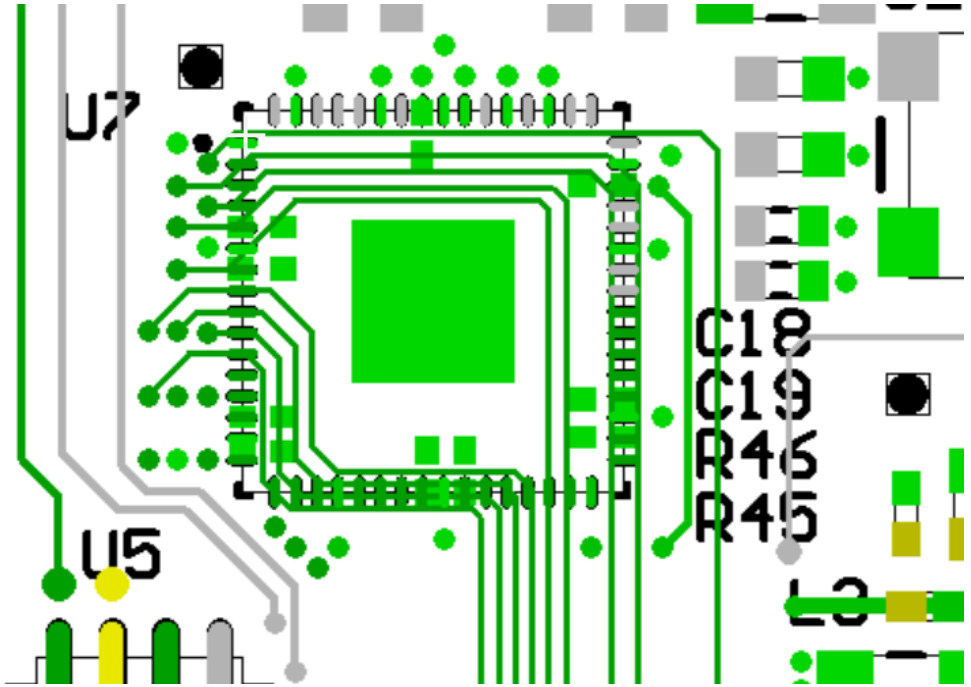
- TP Digital <n> <level>
- TP Analog <n> <voltage>

..and recalculate the testability

Visualize Coverage







I’m not using it for test because:

- Boundary-scan devices are more expensive
- It adds tracks
- It adds more work during design
- Investment in tools
- It is all new to me, I don’t have time to learn
- I only do one complex design per year, learning curve
- Our EMS uses other test methods for electrical test

Why not think again because:

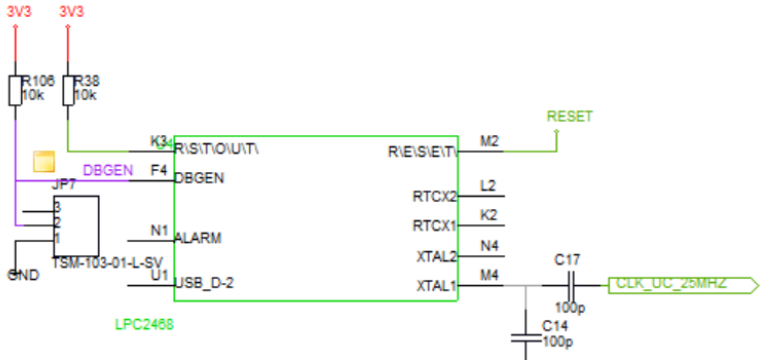
- FPGA’s , uC’s,… can NOT be purchased without it
- Only 5 to ~10, but minimizes number of Test Points
- Less Test Points placing, Quicker Prototype HW validation
- Some FOC Tools are on the market, Services, Temp. licenses
- Training on the job during your design process
- Out source analysis and Test pattern generation
- Flying Probe and ICT are more expensive & lower coverage

Summary: Benefits using JTAG

- € Testing HW without firmware
- € Minimizes number of design cycles
- € Minimizes number of Test Points
- € Tests are already available during prototype stage
- € High test coverage of more complex designs
- € Good failure localization
- € One interface for testing and programming
- € One test & ISP strategy for entire product life cycle
- € Simplifies tester configuration and fixture

JTAG Technologies B.V.
Boschdijk 50, Eindhoven
040 295 0870
www.jtag.com
www.jtaglive.com

Questions?



Demo's:

- Analysis of schematics with JTAGMaps
- Boundary-scan Application development station
- Boundary-scan stand-alone production station