De Boundary scan functies van een FPGA gebruiken als kern voor de HW validatie

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Subjects

- Introduction to modern Bscan
- Bscan capabilities on a FPGA based design example
- Suggested development process (DFT)

Validating HW without firmware and without test pads

IEEE 1149.1

Standard since 1991 and still evolving

A.k.a. JTAG (Joint Test Action Group)

Boundary scan 2-3

At the basis boundary-scan is about testing the presence of connections between components:

- At board level: connections between chips
- At module level: connections between boards
- At system level: connections between modules

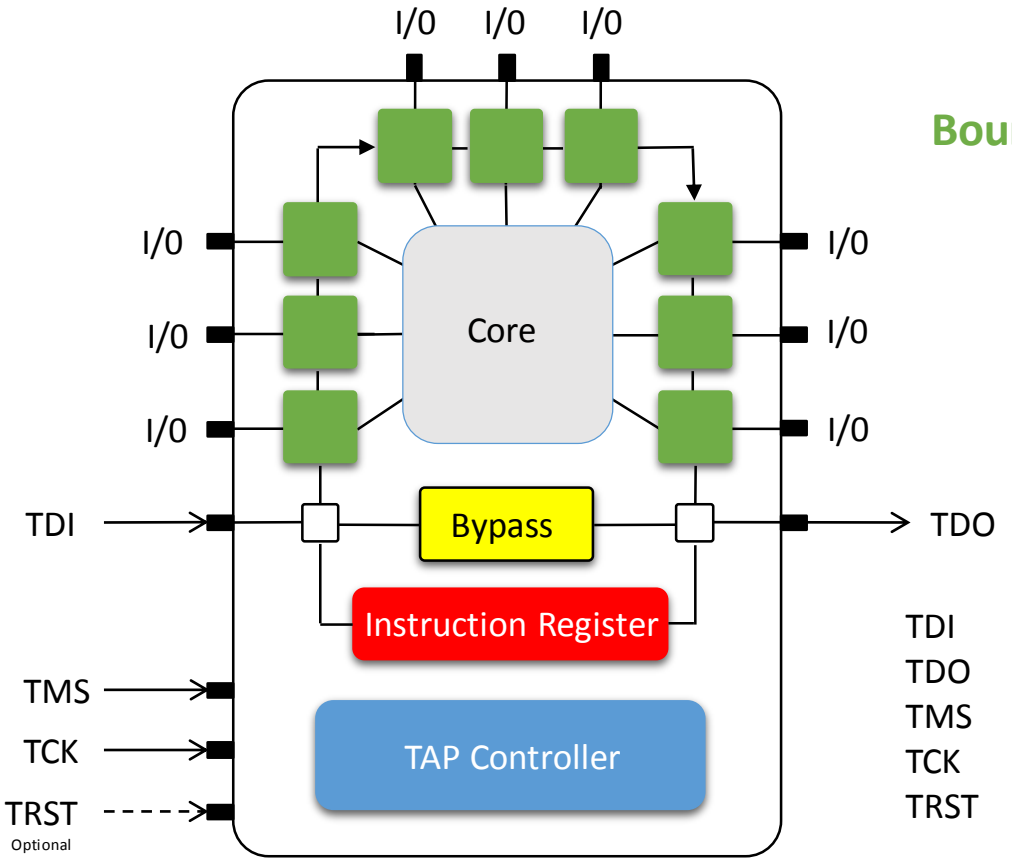
by using (test) resources already embedded in chips

Boundary scan 3-3

Boundary-scan is also used for:

- In-system device programming
  (cPLD's, FPGA's, Microcontrollers, Flash memories and many special devices)
- Software debugging
- Others: Fine-tuning circuits, reading built-in sensors (eg temp), etc.

Adding Boundary scan to a device



Boundary-Scan Register

TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
TCK	Test Clock
TRST	Test Reset

TAP (Test Access Port)
(JTAG)

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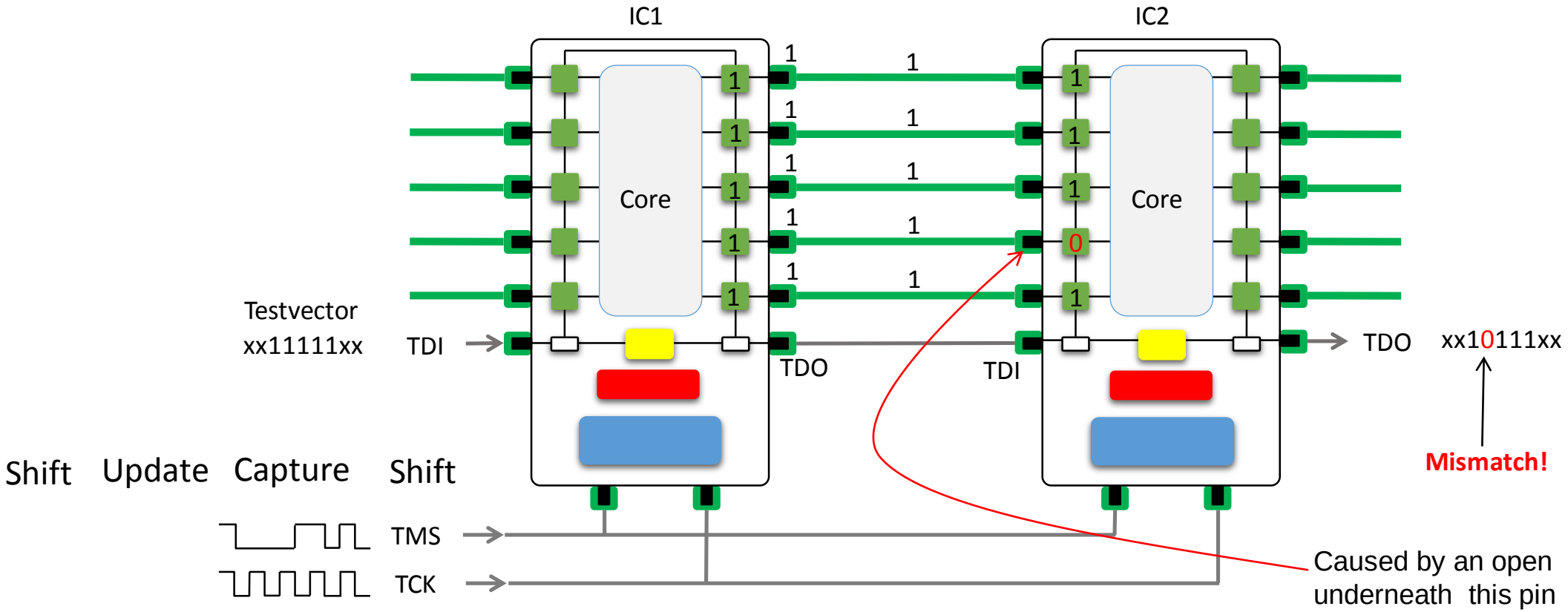
Testing interconnections



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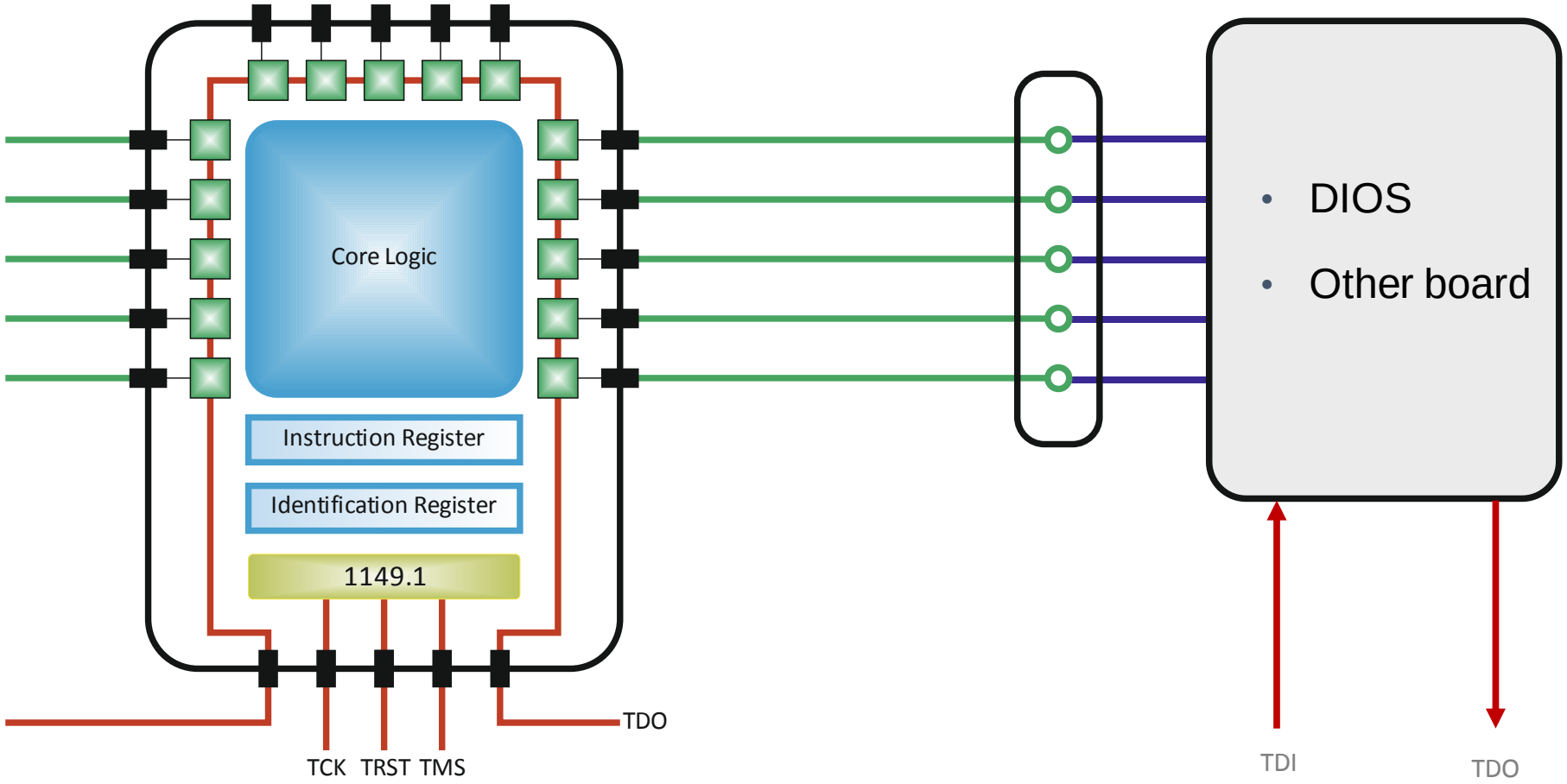
Testing through connectors 1 -2



Finds and locates
- ✓ Stuck @ 0
- ✓ Stuck @ 1
- ✓ Bridge
- ✓ Open

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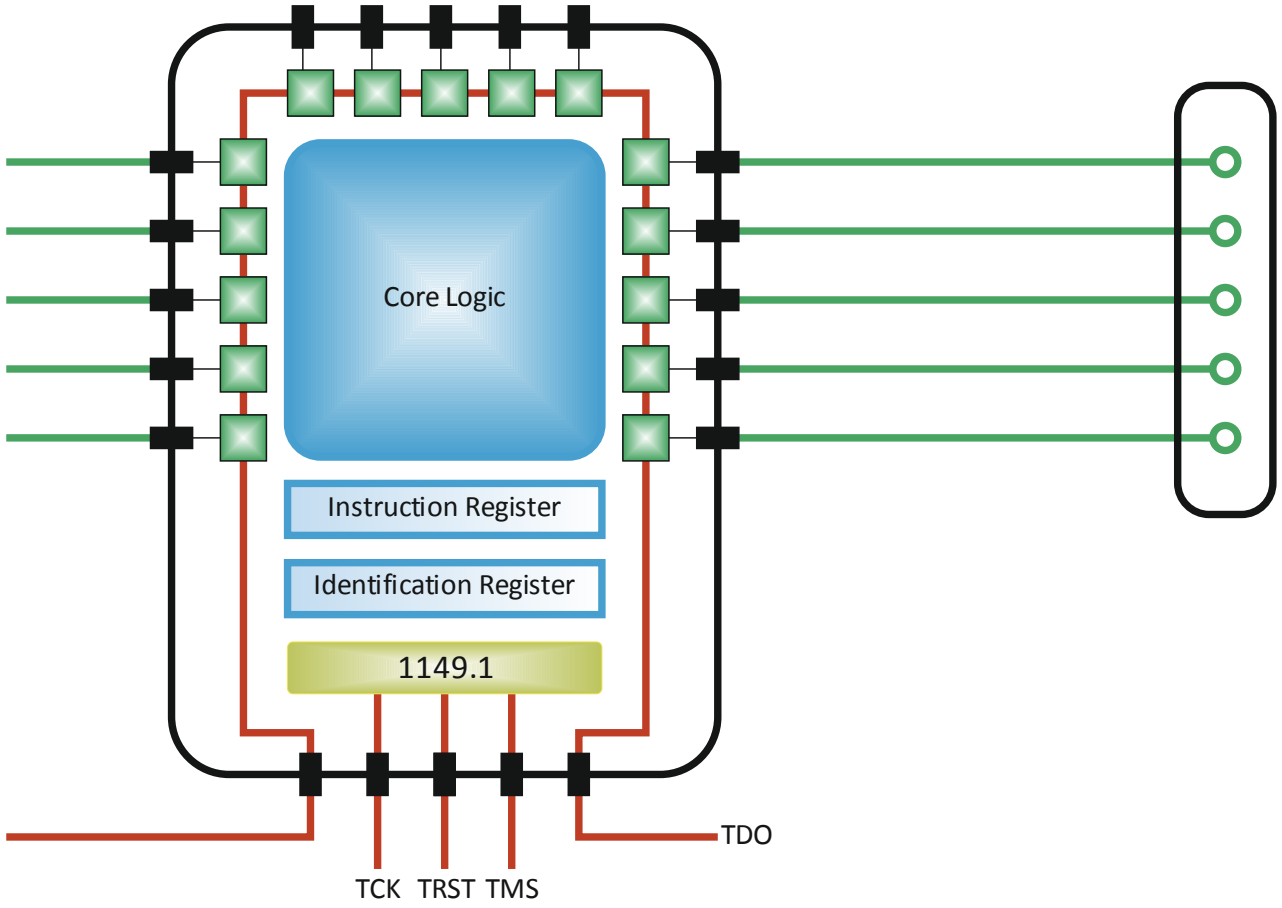
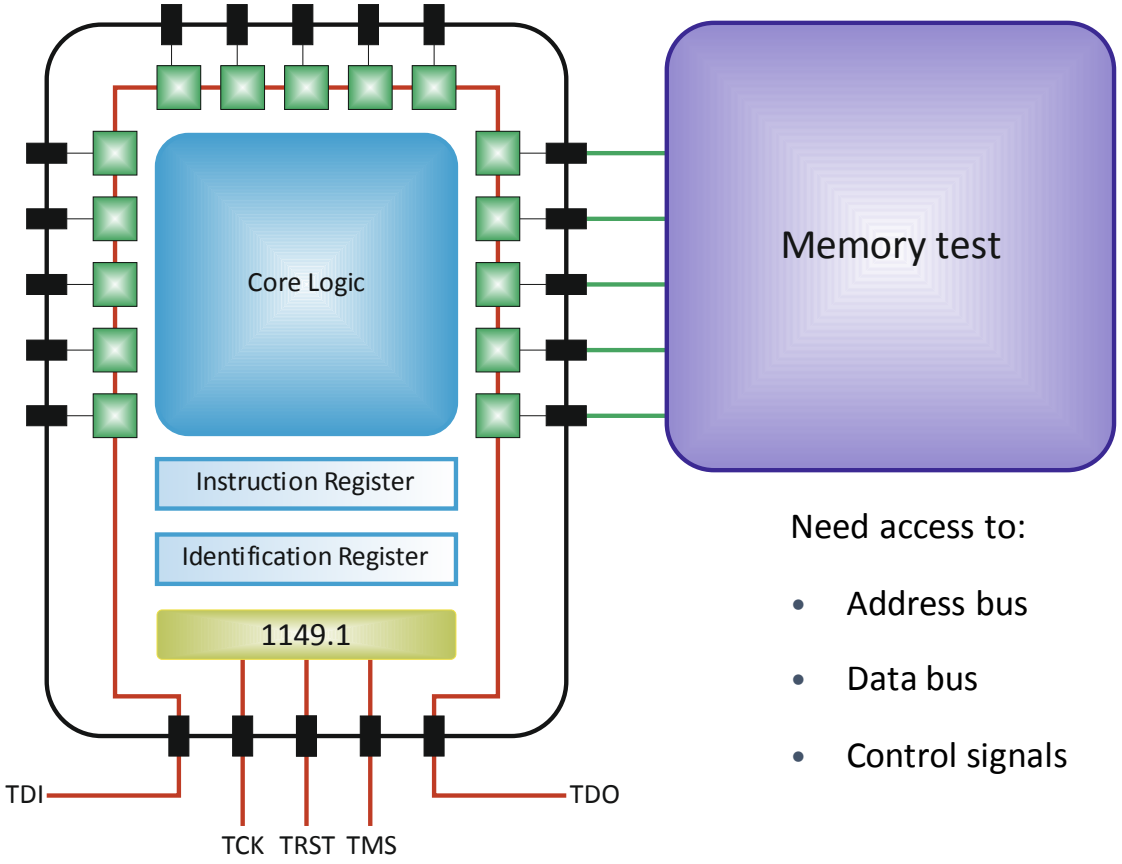
Testing through connectors 2 - 2



Finds and locates

- ✓ Stuck @ 0
- ✓ Stuck @ 1
- ✓ Bridge
- ○ Open

Testing Memory connections



Need access to:

- Address bus
- Data bus
- Control signals

Examples:

- SRAM
- DRAM
- SDRAM
- DDR2
- DDR3
- DDR4
- …

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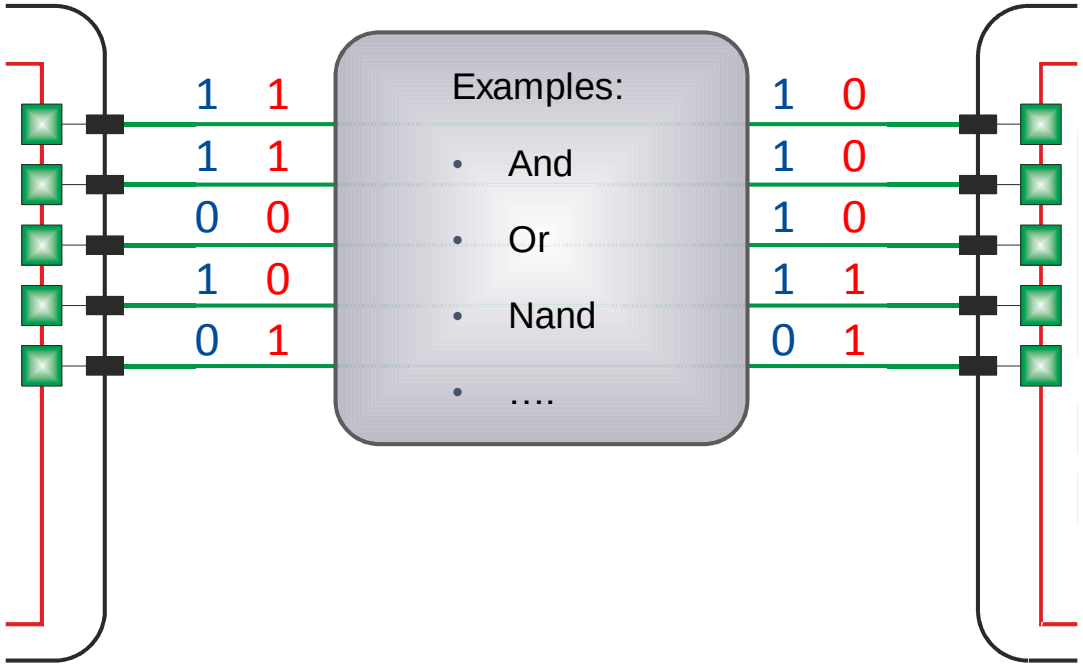
Testing connections through combinatorial logic



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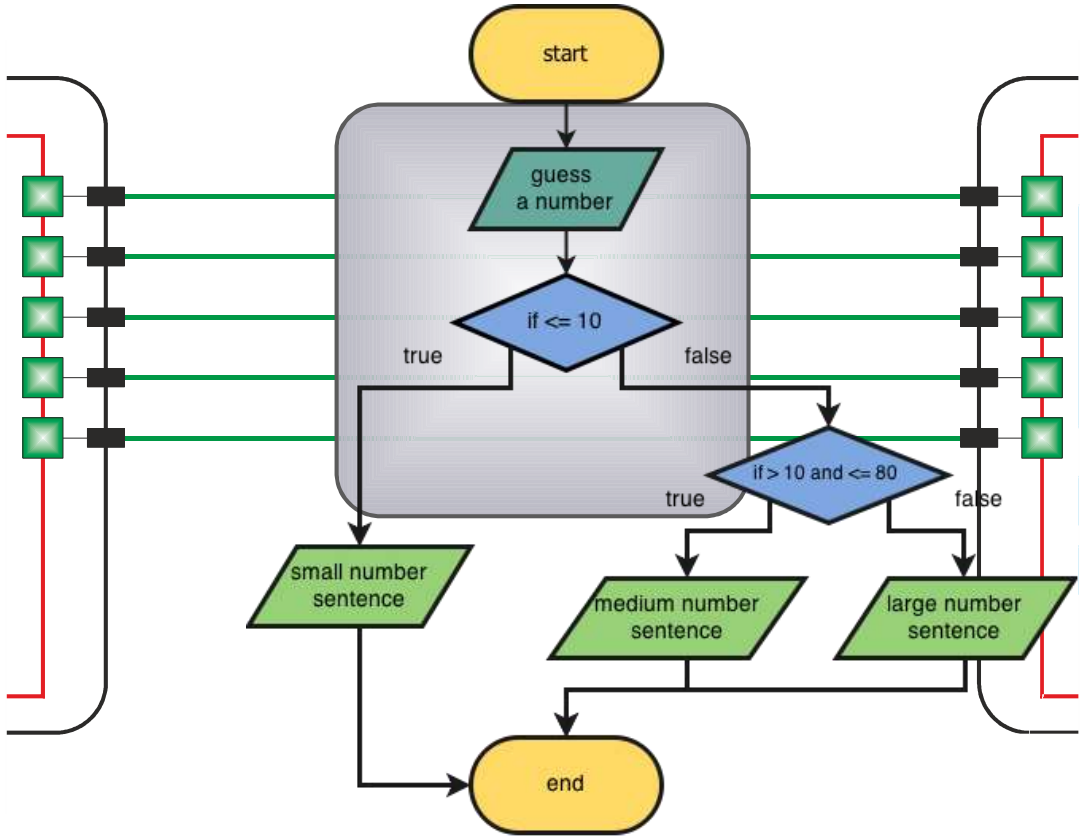
Testing connections through sequential logic



Examples:

- ADC / DAC
- I2C components
- Clock toggle test
- SPI components
- Calibration components
- RS232
- Ethernet chips
- Interactive applications

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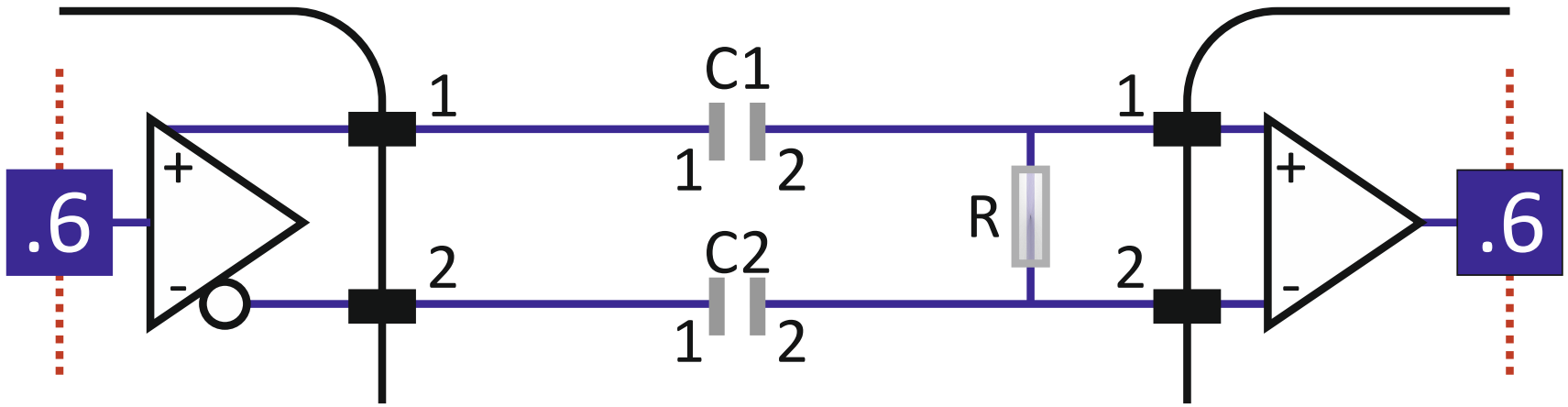
LVDS Interconnect test .6



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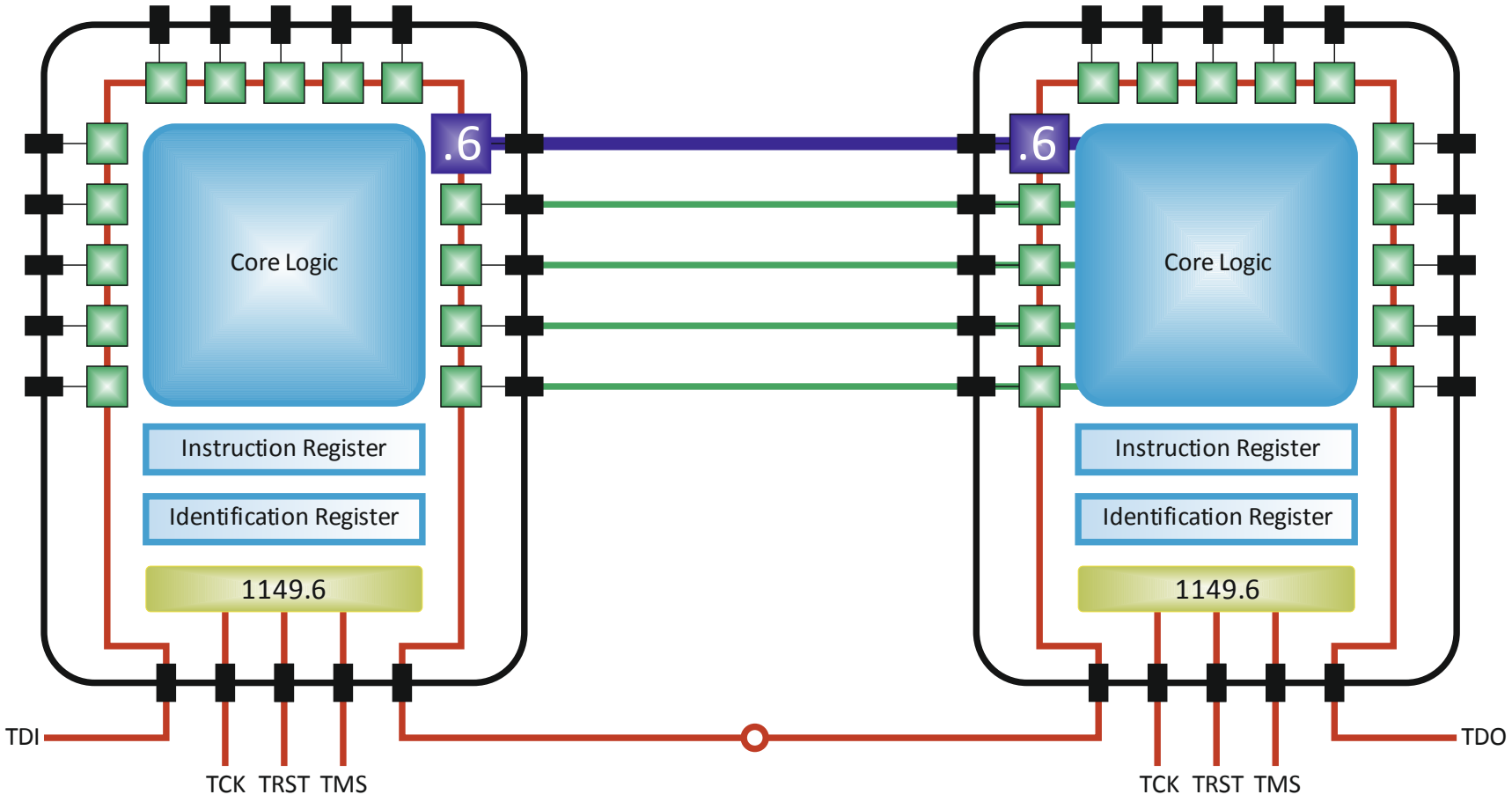
LVDS Interconnect test .6



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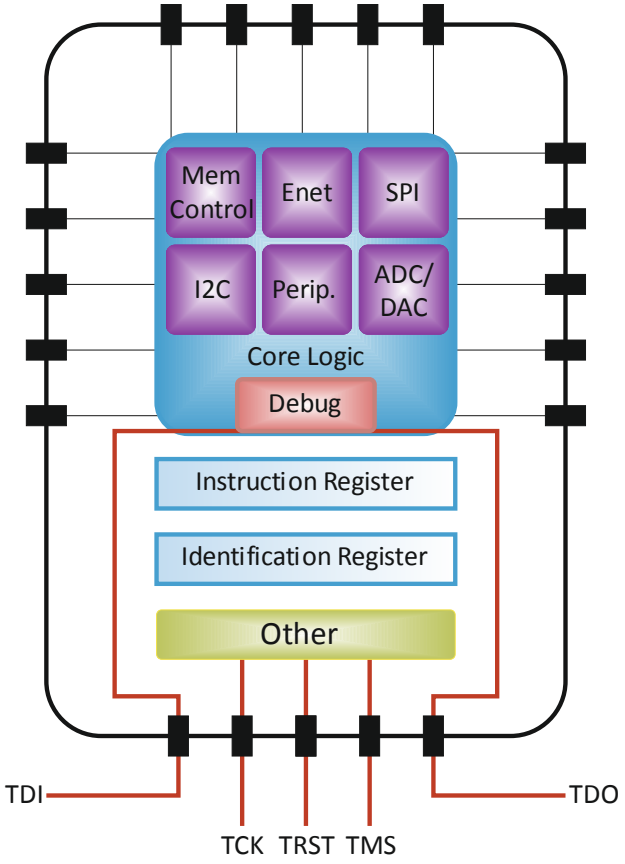
Using Debug & IP blocks for testing Peripherals



uC's:

- ARM
- Analog Devices
- Freescale
- Infineon
- Microchip
- Texas Instruments
- Xscale
- NXP
- ST
- Samsung

FPGA's:

- Intel / Altera
- Xilinx
- Actel
- Lattice

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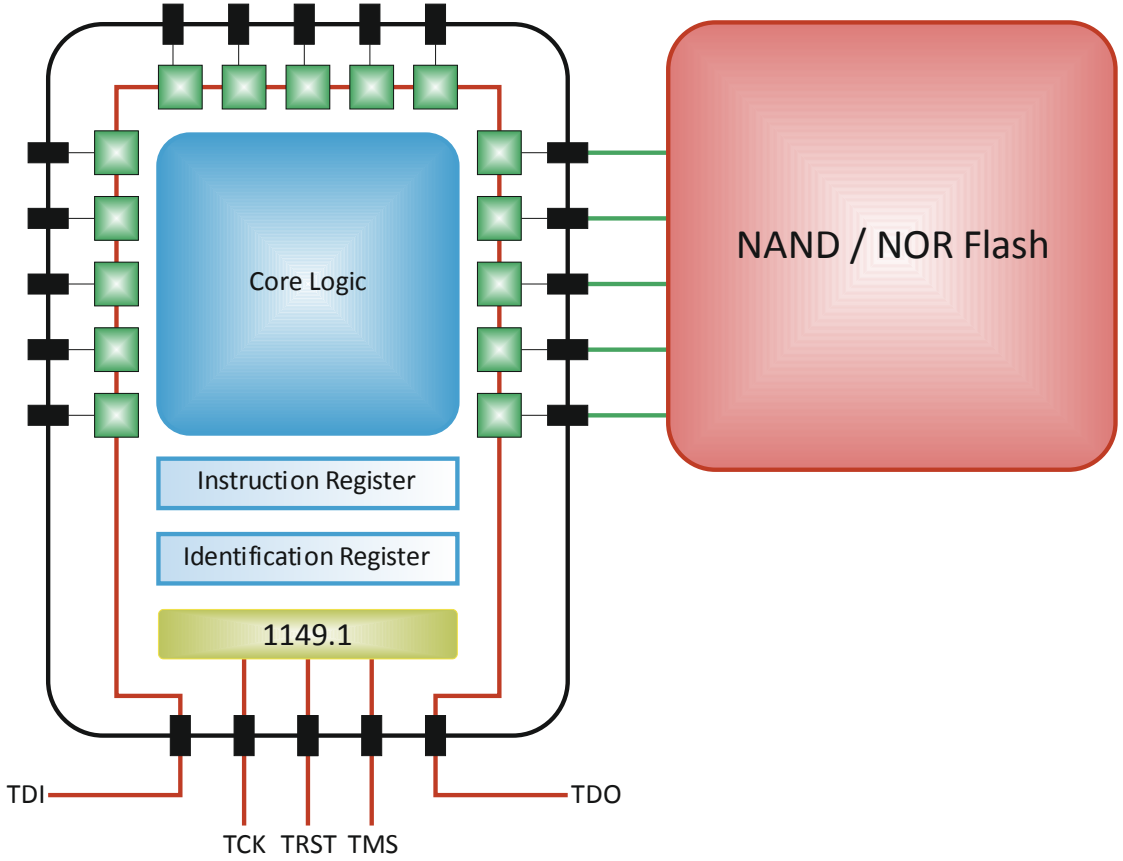
Programming Nand / Nor Flash



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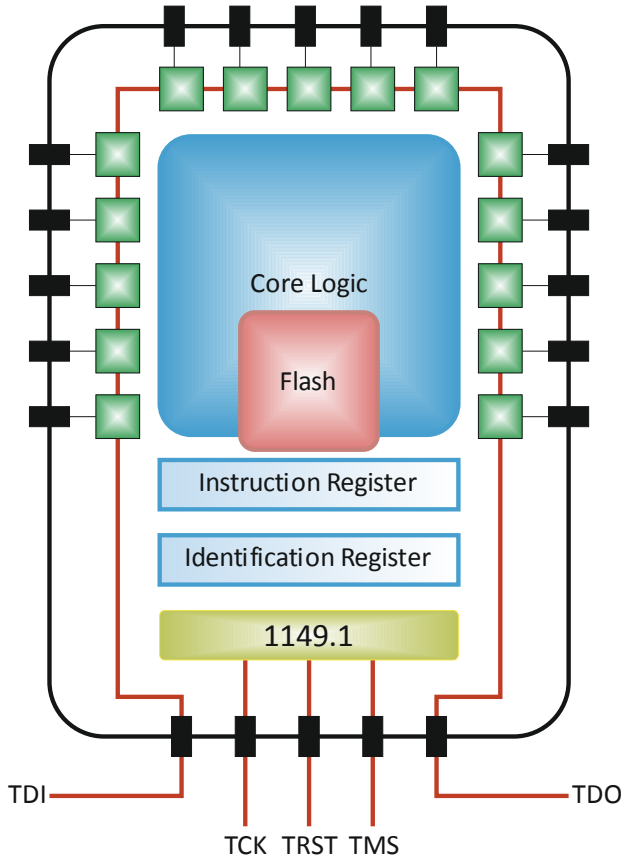
Programming uC's



- Analog Devices
- Atmel
- Cypress
- Freescale
- Infineon
- Microchip
- Nordic
- NXP
- Philips
- Renesas
- ST
- Silicon Labs
- TI
- ....

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Programming Logic

- JAM
- STAPL
- SVF
- Jedec
- IEEE 1532

- Actel
- Intel / Altera
- Lattice
- Xilinx

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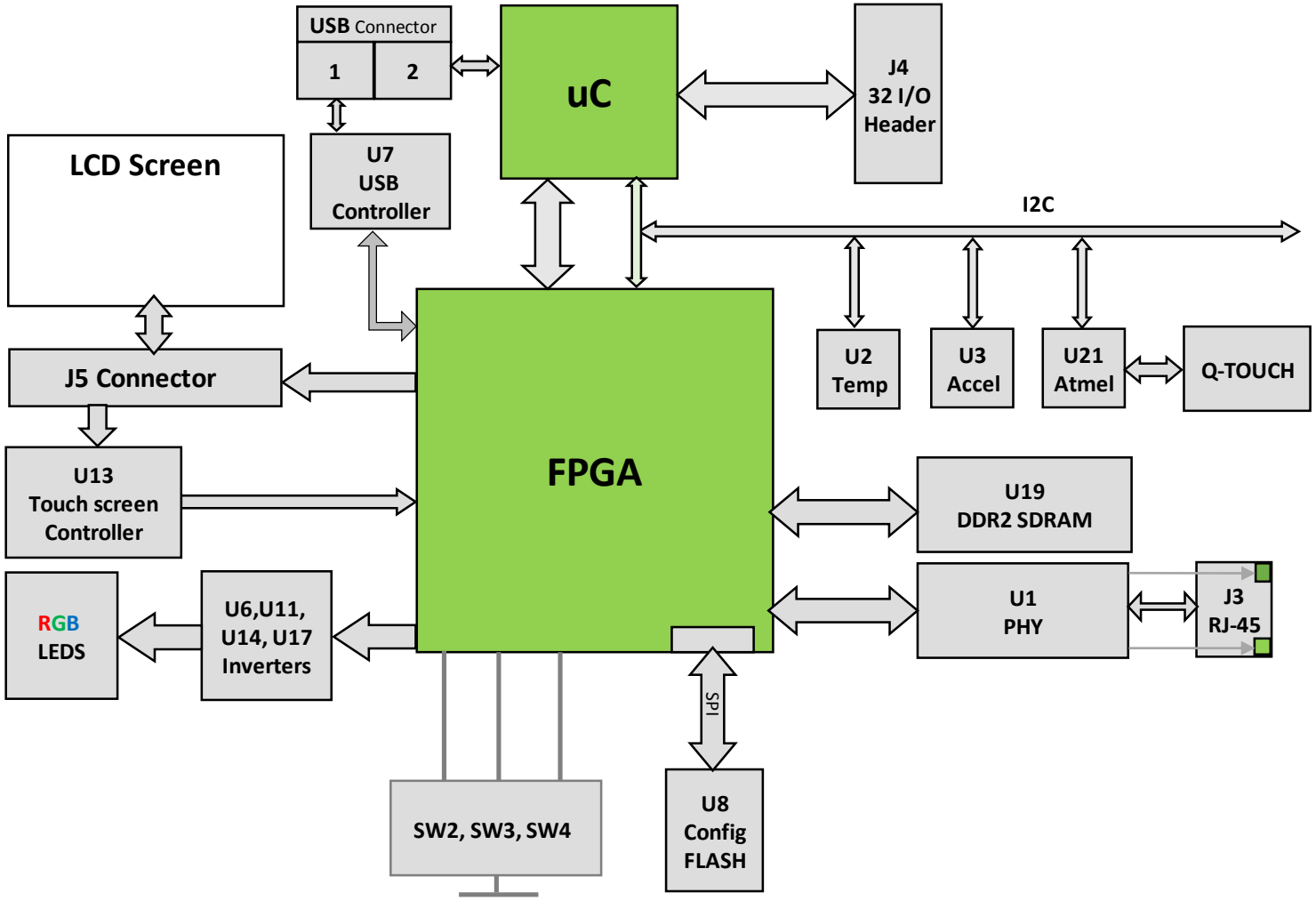
Design example FPGA based



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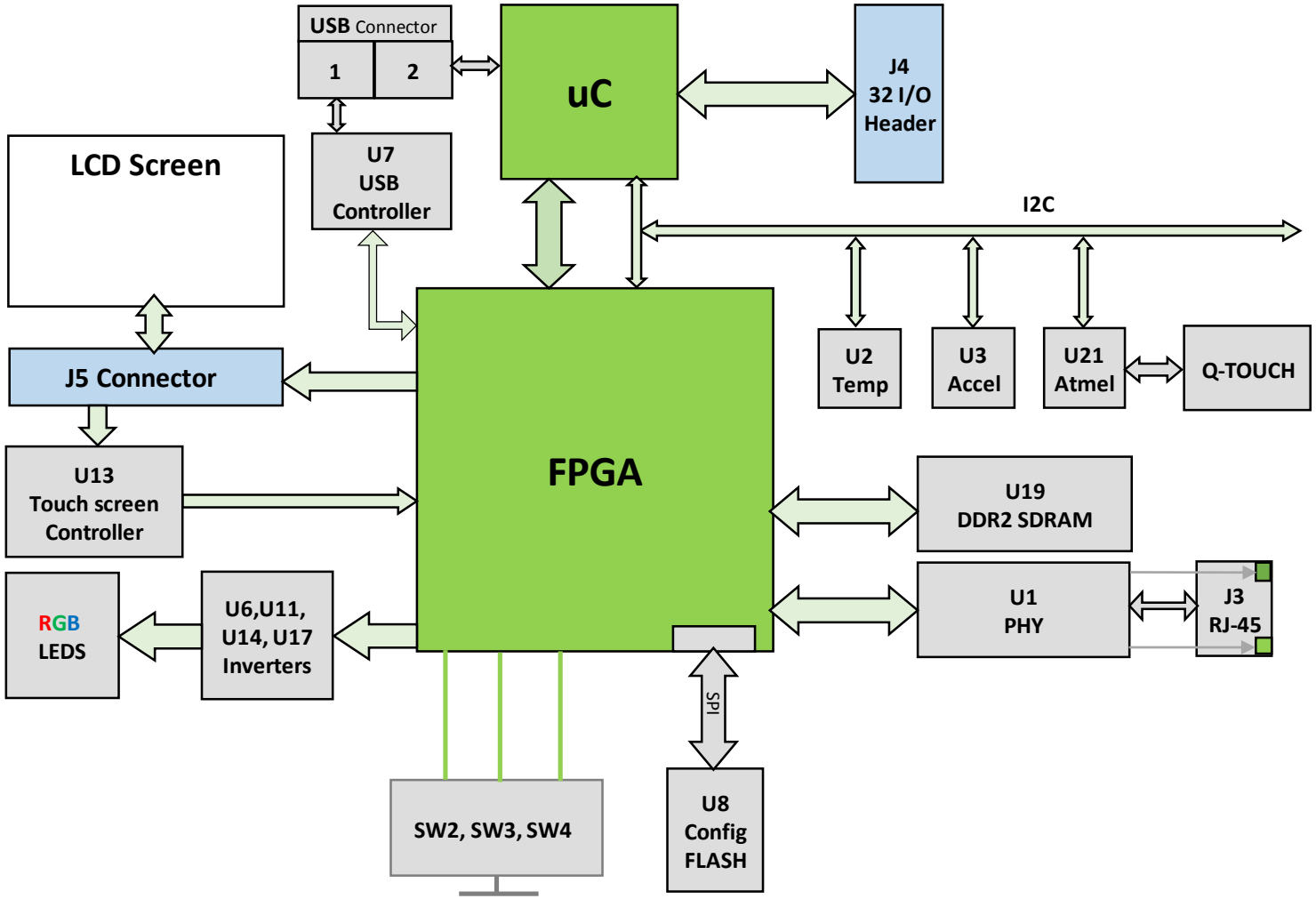
Bscan capabilities on FPGA based design example

What is applicable for your design?



- ✓ Interconnections between Bscan pins
- ✓ Testing through Connectors
- ✓ Resistors presence; Serial Pull-up / Pull down
- ✓ LVDS connections
- ✓ Emulative testing
- ✓ At speed memory interconnection test
- ✓ Using Embedded instruments
- ✓ ISP of Flash, uC, FPGA's, cPLD's

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Design For Test

Check as early as possible in the development process, what is the ….

- ✓ Accessibility via:
  1. Bscan pins
     a) Is the device IEEE 1149.1 compliant?
     b) Do all pins have bscan cells?
  2. Connectors pins
  3. Via test points in the schematics
  4. Via VIA's in the PCB layout (ODB++)
- ✓ Testability
- ✓ Programmability and programming times of the programmable devices
- ✓ Contactability of connectors and test points

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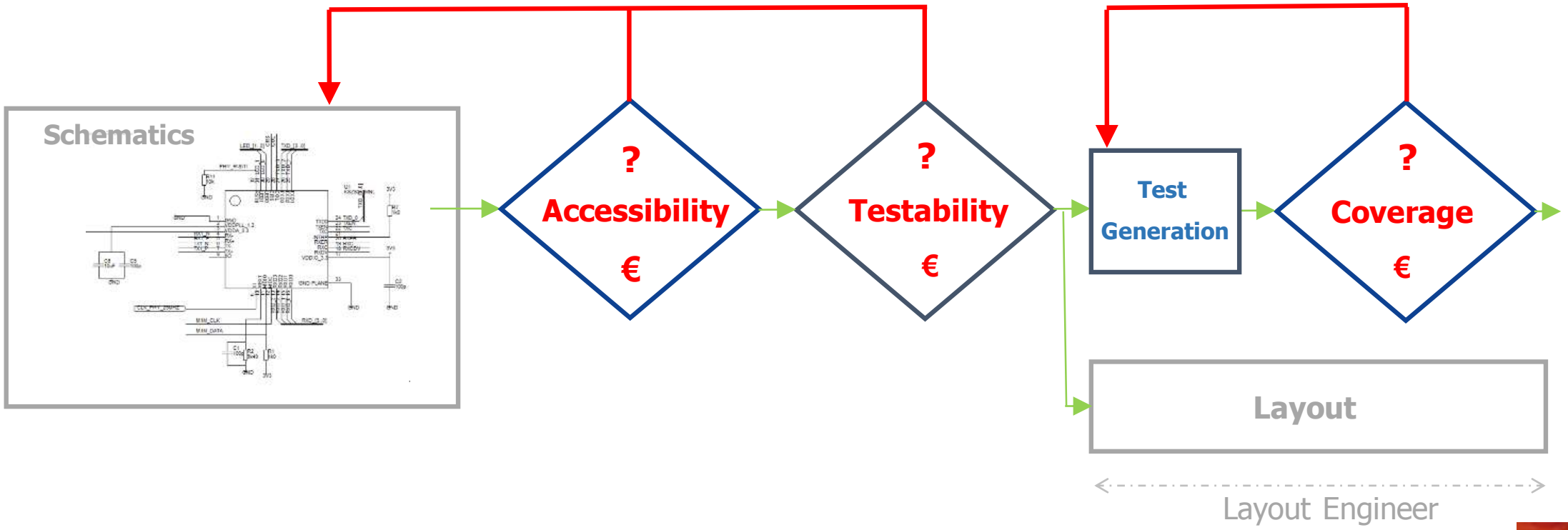
DFT analysis during schematic stage



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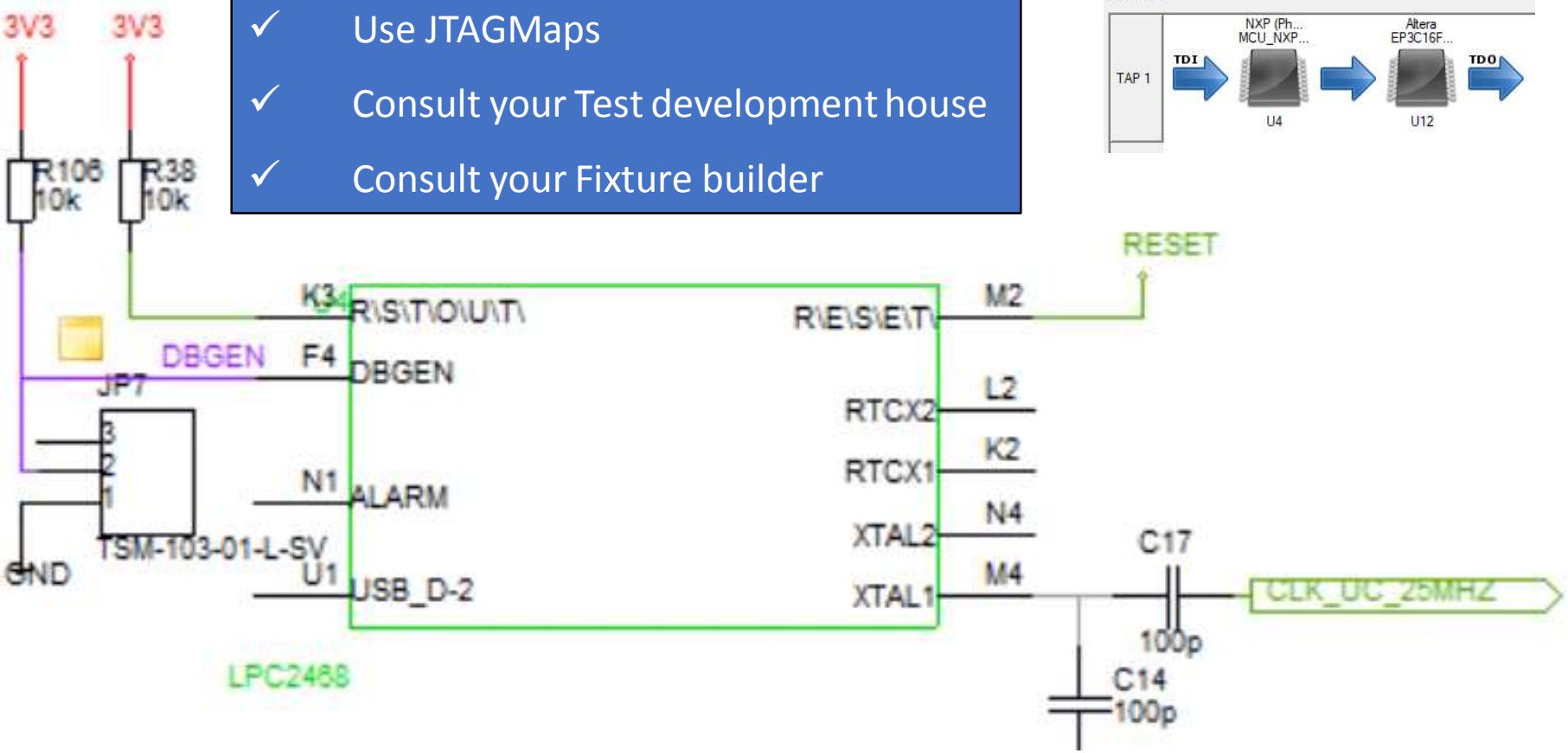
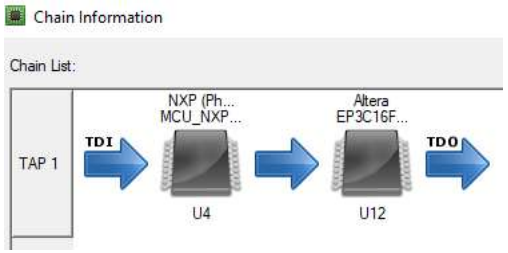
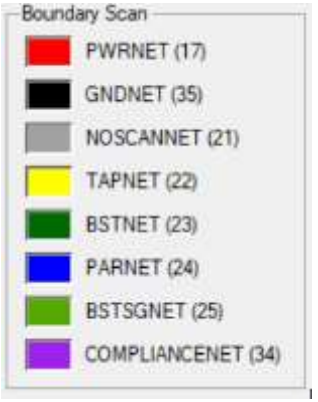
Check access during schematic capture!

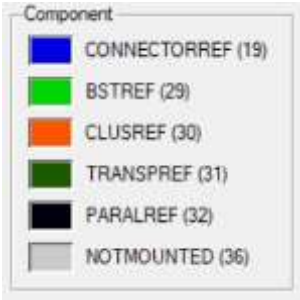
How?

- ✓ Use JTAGMaps
- ✓ Consult your Test development house
- ✓ Consult your Fixture builder









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Summary: Benefits using Boundary Scan

- € Testing HW without firmware
- € Minimizes number of design cycles
- € Minimizes number of Test Points
- € Tests are already available during prototype stage
- € High coverage of more complex designs
- € Good failure localization
- € One interface for testing and programming
- € One test & ISP strategy for all product life cycles
- € Simplifies tester configuration and cassette

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Answers to your questions:

- Visit our booth:
  - Explore your design on its Bscan capabilities
  - Demo:
    - ✓ JTAGMaps
    - ✓ JTAGLive
    - ✓ ProVision
- Send me an E-mail: rik@jtag.com

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