Speed-up Your FPGA-on-Board Design Flow

Bas Hassink

Senior Application Engineer

InnoFour

Agenda

- Presentation
  - IO Standards Effect Pin Assignment
  - Review IO standards and structures
  - Integration of IOPT in PCB design flow
- Demonstration

IO Standards Effect Pin Assignment

- Most common sources of FPGA failures or delays:

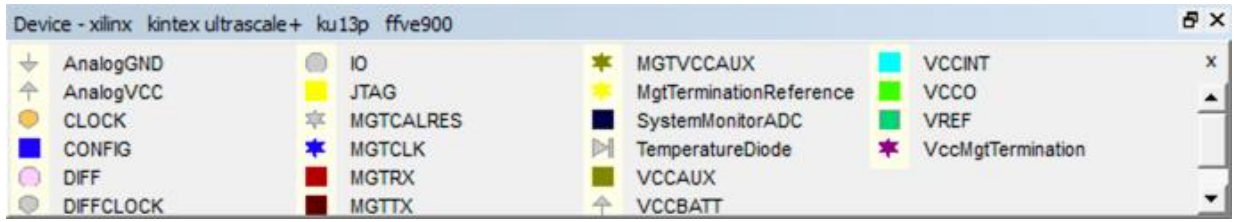
  #1 Timing Closure

  #2 High Speed Interfaces (PCIe, DDR3)

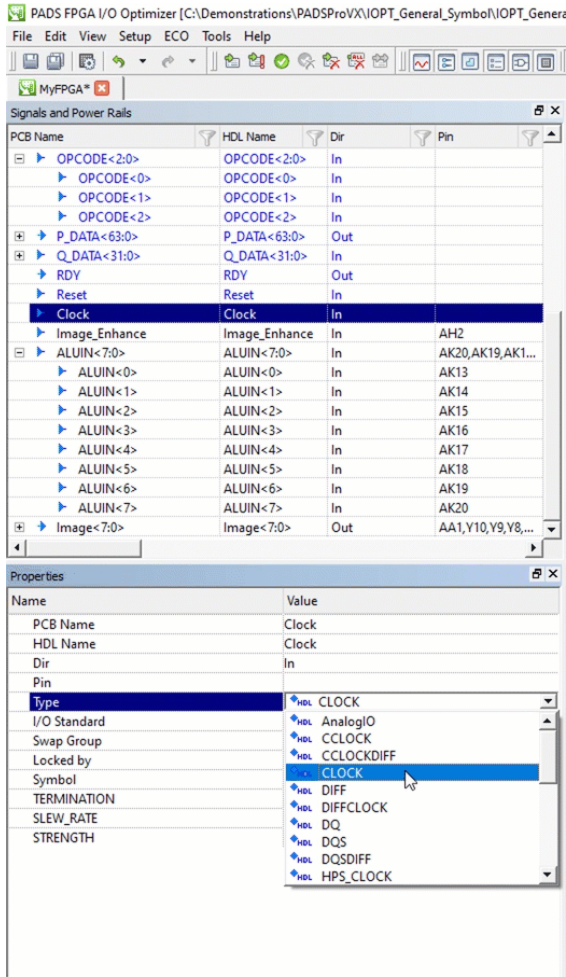
  #3 Pin assignment and I/O errors

IO Standards and Pin Assignments

- IO Standards vary greatly, even within one FPGA



- IO Organized in banks with one voltage reference.
  - +3.3, +2.5, +1.8 are common;
  - One bank may be different from the next.
- Single ended IO are LVTTL or LVCMOS, with many variations including HTL, SSTL, GTL, etc.
- Differential IO typically LVDS but also LVPECL, CML, etc.
- MOST IMPORTANT:
  Global nets are usually assigned to specific pins that can also be IO. PCB Layout must use these pins as clocks or reset if global nets are to be used

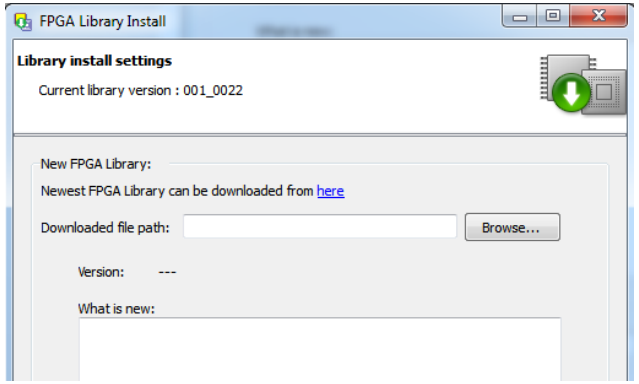


FPGA Device Support

- Mentor supports a comprehensive up-to-date library of FPGA vendor devices
  - Link to Support Center (https://support.sw.siemens.com/en-US/knowledge-base/MG593597) to download the latest IOPT FPGA library update

Where to download the latest I/O Optimizer library information.

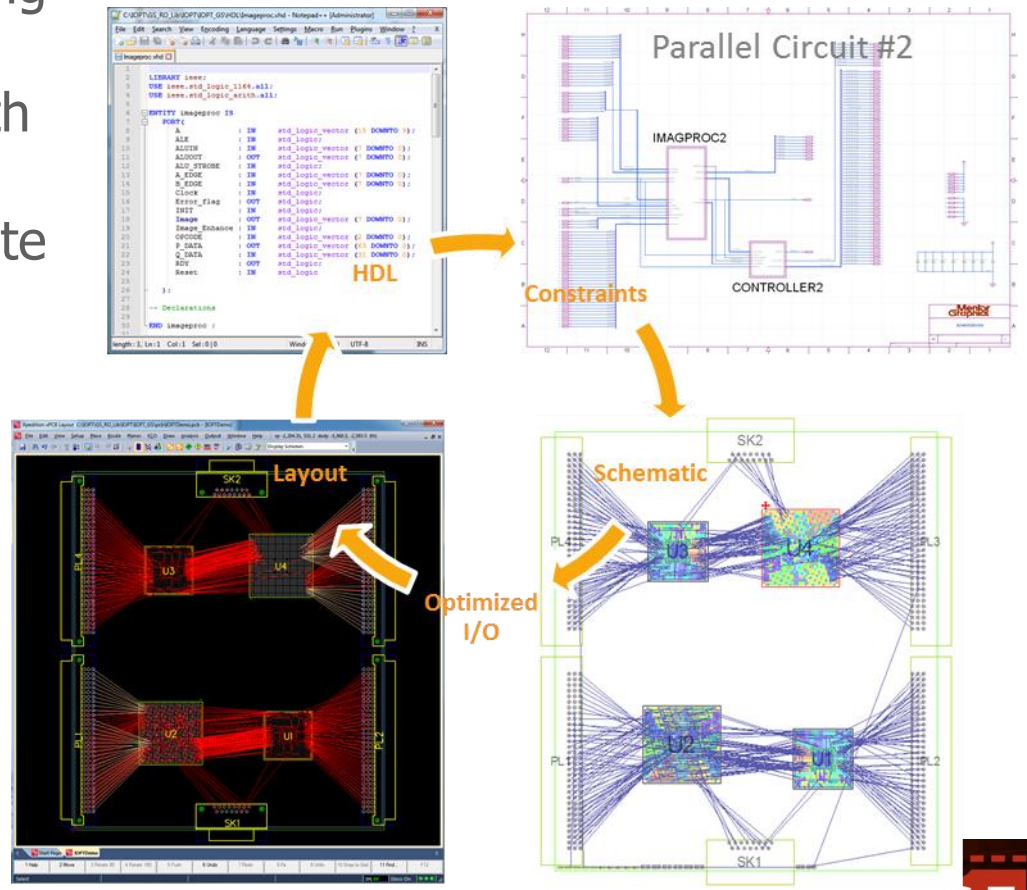
- To view the latest xDX IOPT library version number and the content of the library select **here** .
- To download the latest library as a zip file select **here** .
- To request a new device that is not already in the library complete the document **here** .



- Proactive monthly delivery of Vendor device family updates
- On-demand service support for the very latest devices
  - Average new device support delivery is 2 weeks
  - Free available to all VX.*.* customers on maintenance support contract
  - Covers pre-release and restricted devices where access is available

FPGA-on-Board Collaboration

- Bridging the domains of FPGA design and PCB design
  - Optimizes the FPGA IO in the Board context, resulting in easier and more efficient routing to the FPGA
  - Less netline cross overs - Less vias, Less trace length
  - Imports HDL, Vendor Constraints, CSV, Place & Route report and Schematic as the connectivity source
  - Exports HDL, Constraints, CSV for vendor validation



- Board Schematic Design:
  - Multi-FPGA I/O Optimization (unravel/swapping) adheres to vendor device IO Standard and Pin rules
  - Multi-Instances of one FPGA supported
  - Component placement can be forwarded to PCB

FPGA Source Data Management

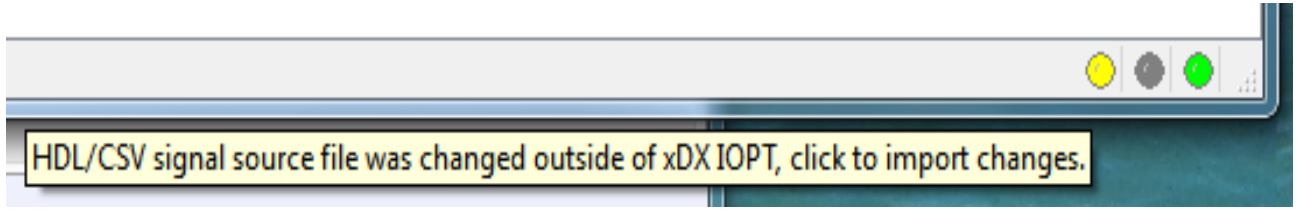
- Merge Connectivity
  - Preview of pending changes as the FPGA evolves
    - Opportunity to Accept/Reject new changes
  - When multiple sources change at once
    - HDL connectivity compared first
    - Followed by separate passes of Constraints, CSV, etc.
  - Opportunity to adjust IO Standard and Direction
  - xDX IOPT Notifies user when source data changes

Merge Connectivity: HDL

Action	PCB Name	HDL Name	Pins	Signal Type	IOStandard	Direction
MERGED						
ADDED						
☑		sramBW_n<4>		IO	2.5 V (Default)	Out
☑		sramBW_n<5>		IO	2.5 V (Default)	Out
☑		sramBW_n<6>		IO	2.5 V (Default)	Out
☑		sramBW_n<7>		IO	2.5 V (Default)	Out
☑		sramDQP<4>		IO	2.5 V (Default)	InOut
☑		sramDQP<5>		IO	2.5 V (Default)	InOut
☑		sramDQP<6>		IO	2.5 V (Default)	InOut
☑		sramDQP<7>		IO	2.5 V (Default)	InOut
REMOVED						
UNCHANGED						

Merge Connectivity: Pin report file

Action	PCB Name	HDL Name	Pins	Signal Type	IOStandard	Direction
MERGED						
☑	ADDR<0>	ADDR<0>	G11	IO	LVCMOS18	Out
Current	ADDR<0>	ADDR<0>		IO	LVCMOS18 (Default)	Out
Imported		ADDR<0>	G11		LVCMOS18	



Types mappir

☑	CLOCK	DIFF
☑	GND	AnalogTRTN
☑	GND	CLOCK
☑	GND	CONFIG
☑	GND	DIFF
☑	GND	JTAG
☑	VCC	CONFIG

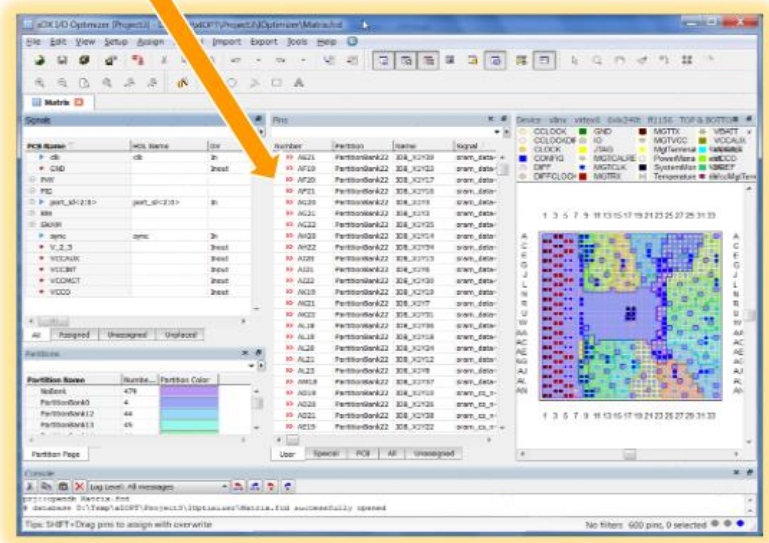
PIN TYPES	
A7	IO
ATTRIBUTES	
PCB Name	Error
HDL Name	Error
IOStandard	LVTTL
Direction	Out

FPGA-on-Board Signal Assignment

- Signal-to-Pin assignment is correct-by-construction adhering to the FPGA vendor IO Standard and Pin rules

Signals and Power Rails

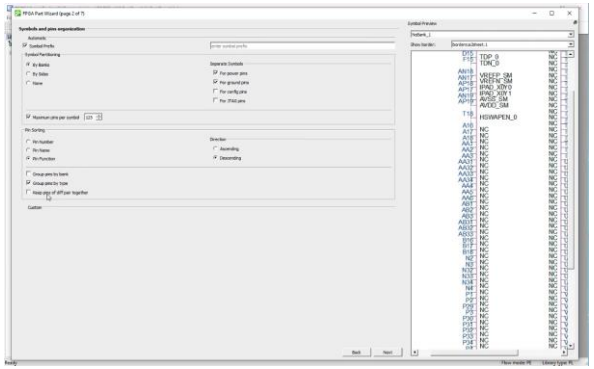
PCB Name	HDL Name	Dir	Pin	Partition	Type	I/O Standard
ALUOUT<7:0>	ALUOUT<7:0>	Out	E34,L34,J34...	XV4_Bank9	IO	LVCMOS25
B_EDGE<7:0>	B_EDGE<7:0>	In	AM2,AK3,...	XV4_Bank12	IO	LVCMOS25
Clock	Clock	In			IO	LVCMOS25
Error_flag	Error_flag	Out	K34	XV4_Bank9	IO	LVCMOS25
GND		Inout	A19,A27,A...		GND	
Image<7:0>	Image<7:0>	Out	AP26,AP21...	XV4_Bank7	IO	LVCMOS25
Image_Enhance	Image_Enhance	In	L1	XV4_Bank10	IO	LVCMOS25
INIT	INIT	In	L3	XV4_Bank10	IO	LVCMOS25
OPCODE<2:0>	OPCODE<2:0>	In	J5,K1,H5	XV4_Bank10	IO	LVCMOS25
P_DATA<63:0>	P_DATA<63:0>	Out	AK34,AK33...		IO	LVCMOS25
P_DATA<0>	P_DATA<0>	Out	AB33	XV4_Bank13	IO	LVCMOS25
P_DATA<1>	P_DATA<1>	Out	AA34	XV4_Bank13	IO	LVCMOS25
P_DATA<2>	P_DATA<2>	Out			IO	LVCMOS25
P_DATA<3>	P_DATA<3>	Out	T34	XV4_Bank13	IO	LVCMOS25
P_DATA<4>	P_DATA<4>	Out	V33	XV4_Bank13	IO	LVCMOS25

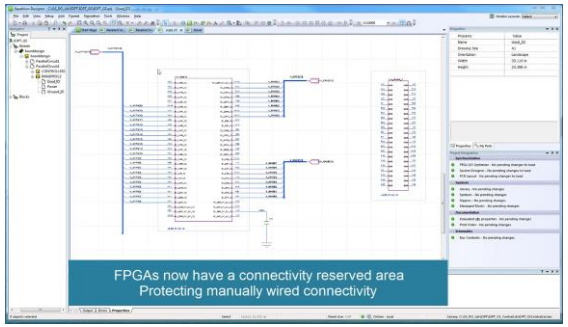


- Custom partitioning the device into functional symbol grouping instead of IO Banks
  - Merging IO Banks or create Partitions graphically
  - Provides flexibility and control in I/O Optimization

Pin Grouping & Partitioning

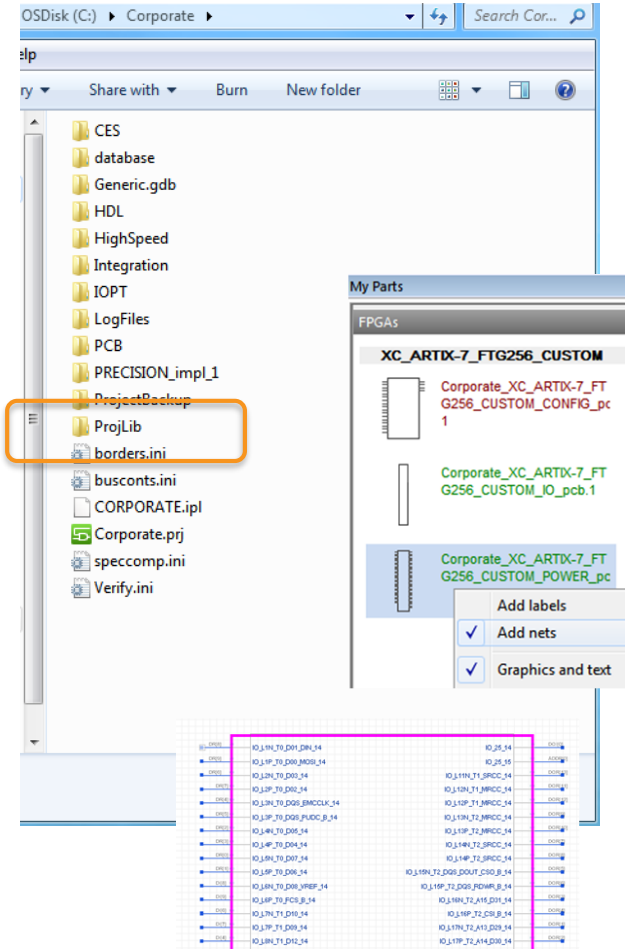
- Corporate Library Parts creation
  - Librarian uses the IOPT licensed *FPGA Part Wizard* to accurately and efficiently create the complex part
  - FPGA parts are instantiated from Designer Search or Databook
  - Design flow is easy-to-use, simple and error free
  - IOPT manages the rule driven pin assignment, pin swap & IO unravelling
  - Optimized FPGA IO is Back Annotated to Schematic symbol pin property instances
  - Unravel between partitions is available





Pin Grouping & Partitioning

- Customized Part Partitioning
  - Flexible process allowing the Part to be partitioned the designer requires e.g. Partitioned in to Schematic functions DDR3
  - IOPT Symbol Generator automatically creates the part & symbols and saved to the local design project library
    - Full Read/Write access by Engineers
    - Packager looks for the data first into Project Library, then to Central Library
    - Part Number must be unique
  - Optimized FPGA IO connectivity is synchronized with schematic using the Project Integration mechanism
  - FPGA parts are instantiated from Designer>MyParts>FPGA menu
  - Option to export/publish to the corporate library

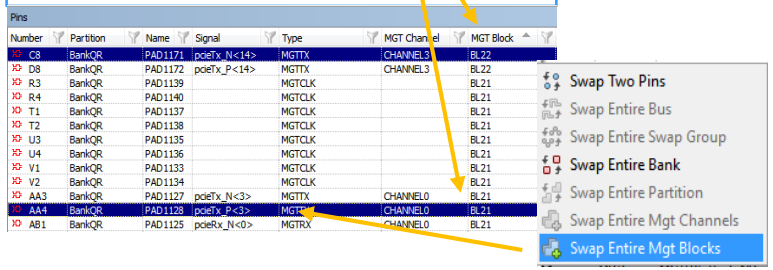


Symbol highlighted
Ready to update

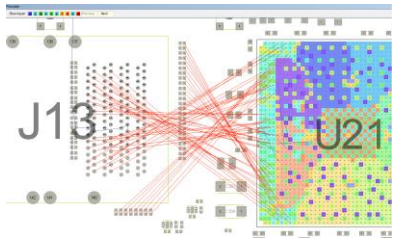
Multi-Giga Bit transceiver (MGT) signal group support

- Support for swapping whole channel and block structures of related MGT signals to improve board connectivity

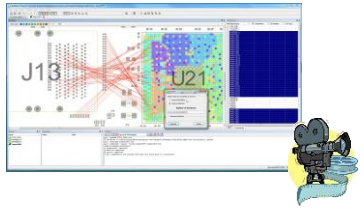
Two receiver signals from different blocks selected.



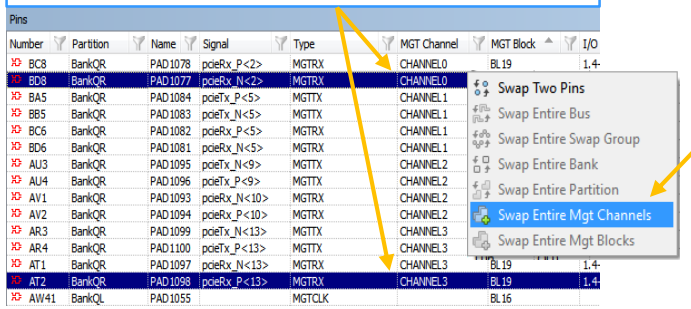
option "Swap Entire MGT Blocks" introduced to swap all receiver and transmitter differential signals together between blocks. This operation keeps related receiver and transmitter pairs together in a channel after swap to different block



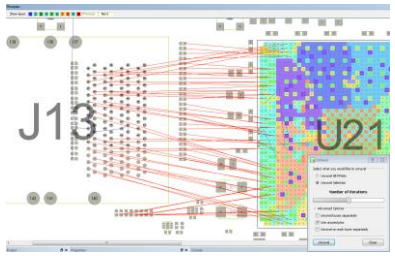
4 MGT channels loaded with transmitter and receiver signals.



Two receiver signals from different channels selected.



option "Swap Entire MGT Channels" introduced to swap receiver and transmitter differential signals together between channels.



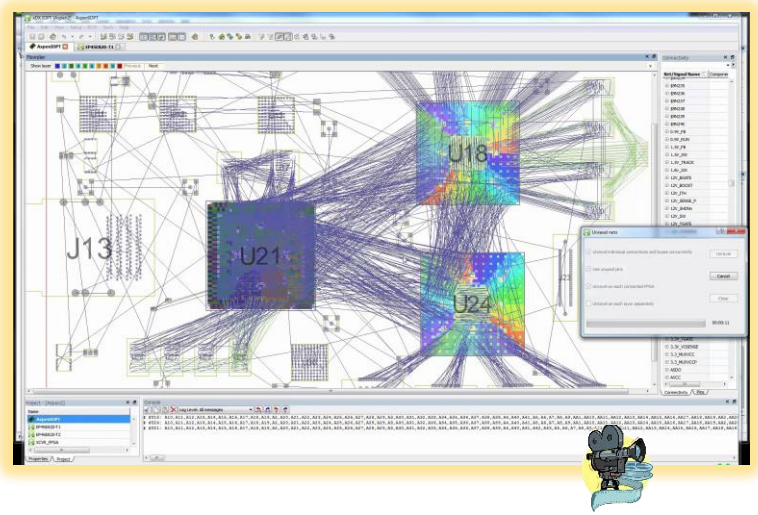
Unravel optimized connections by moving all signals from one channel to another keeping relationships between signals untouched.

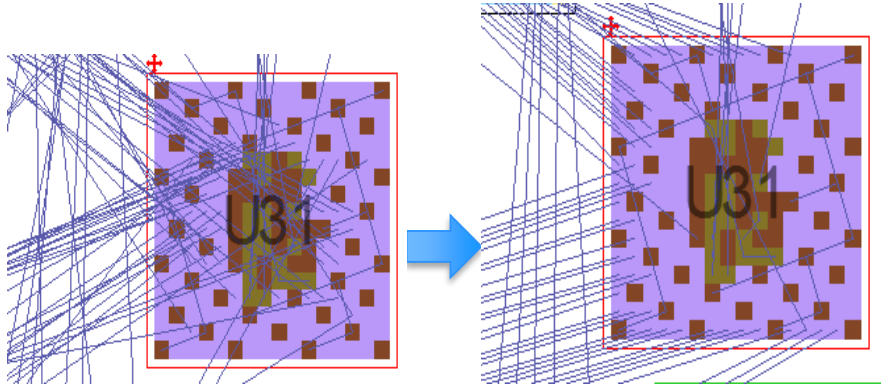
FPGA-on-Board I/O Optimization

- Integrated Floor Planner enables and multi-FPGA optimization in the context of a board layout
  - Simple pre-layout of placement before board exists
  - Multi-FPGA Unravel and selected group Pin Swap

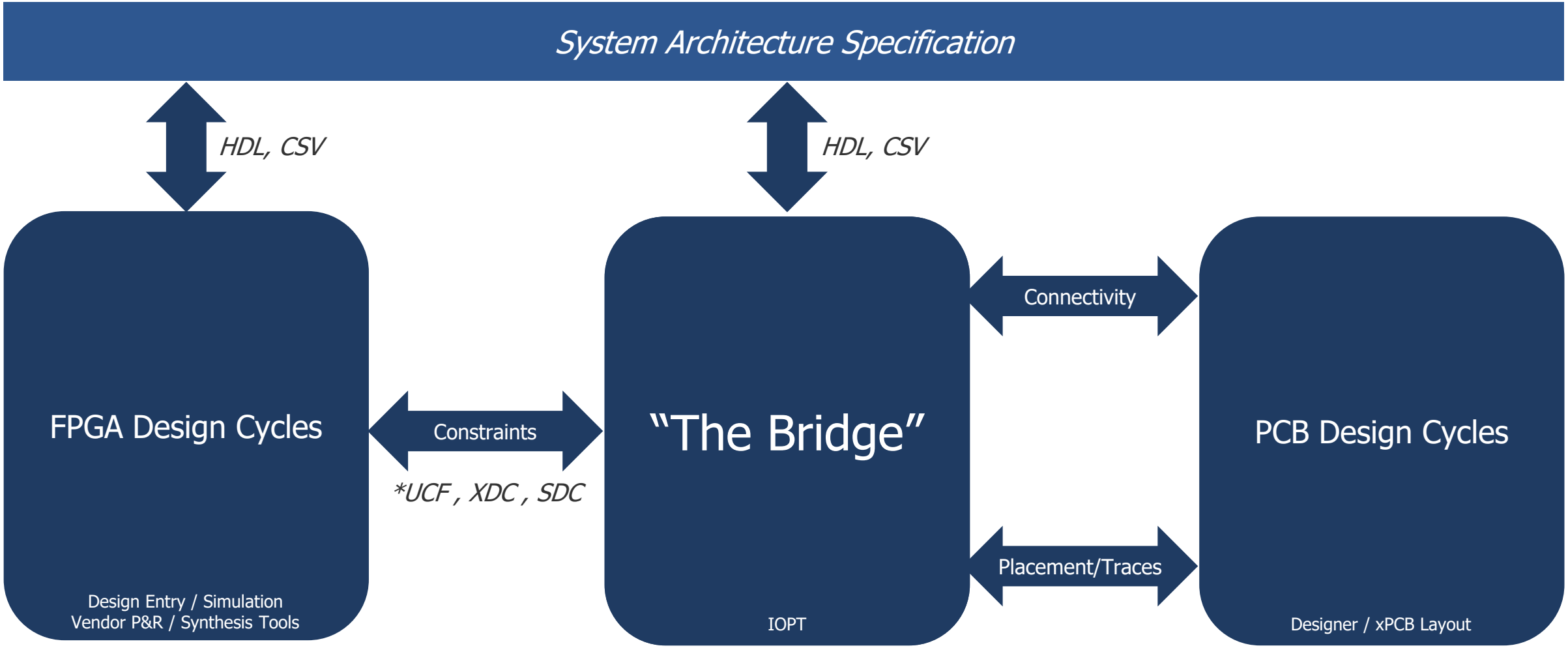
- IOPT manages all pin swapping adhering to vendor IO Standard device rules
  - Option to unravel signal across Partitions
  - Multi-Instances of one FPGA supported
  - Component placement forwarded to PCB

- IO Optimization results in:
  - Easier trace routing – less netline cross overs
  - Less vias, less trace length, Potential for less board layers



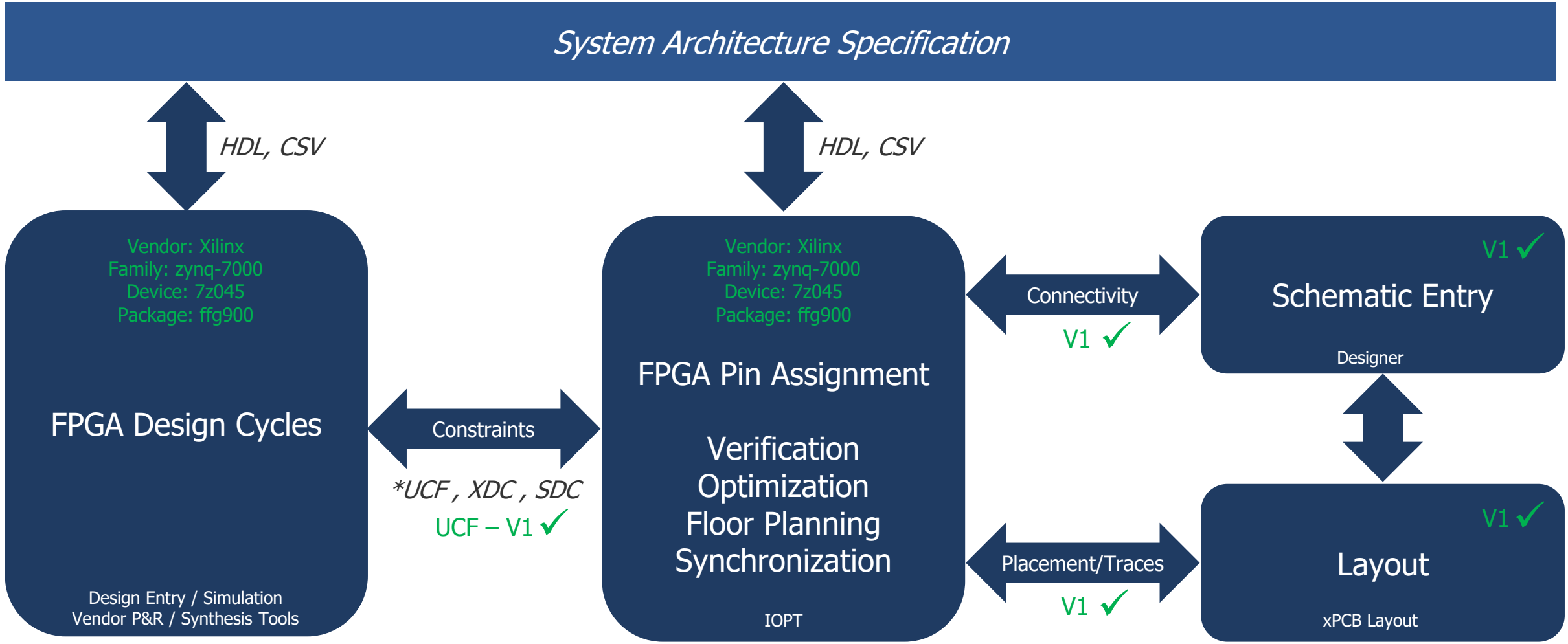


Demonstration: High Level Flow Overview



*Xilinx User Constraints file (UCF)
*Xilinx Design Constraints file (XDC)
*Synopsys Design Constraints file (SDC)

Demonstration: Current Design Status



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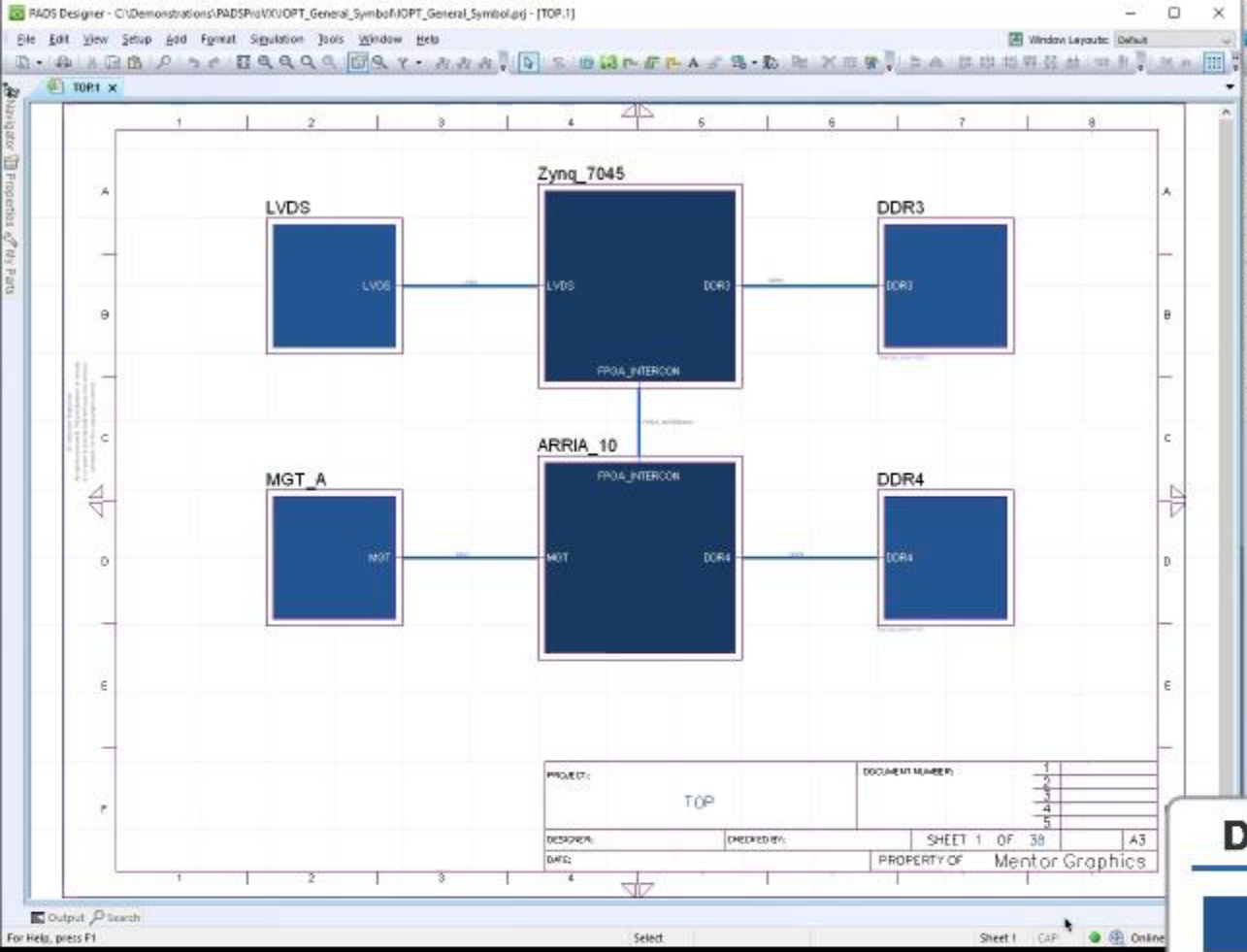

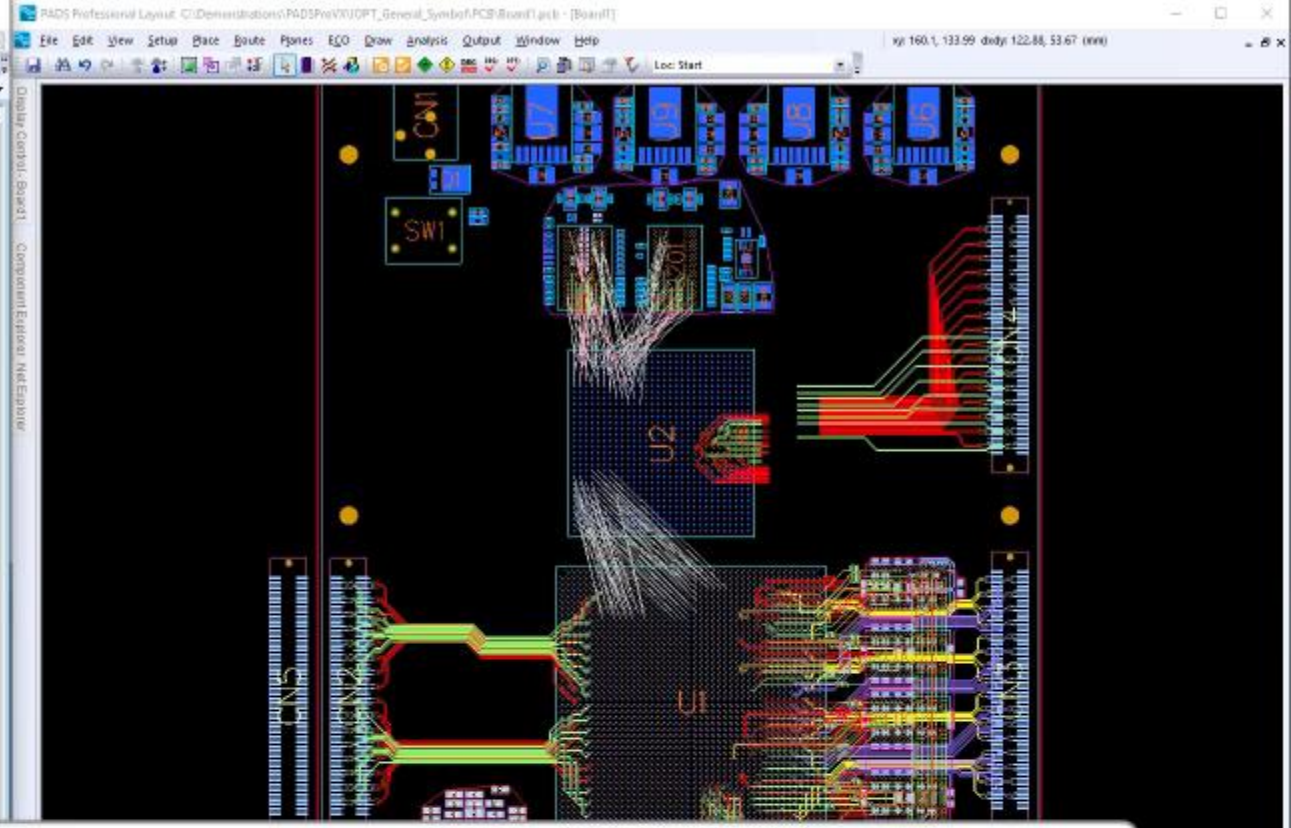

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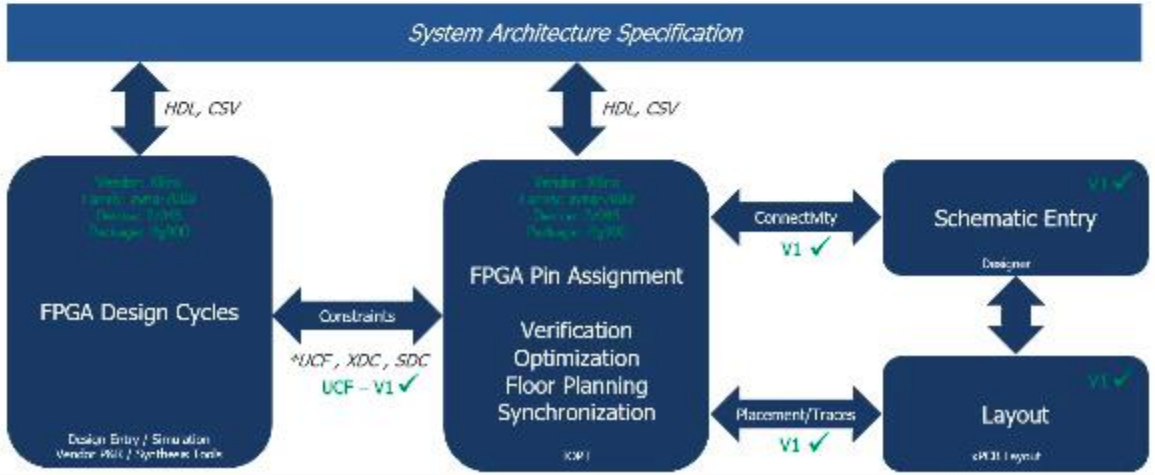


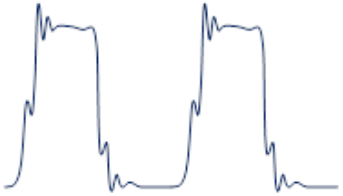
Value & Customer Benefits Summary

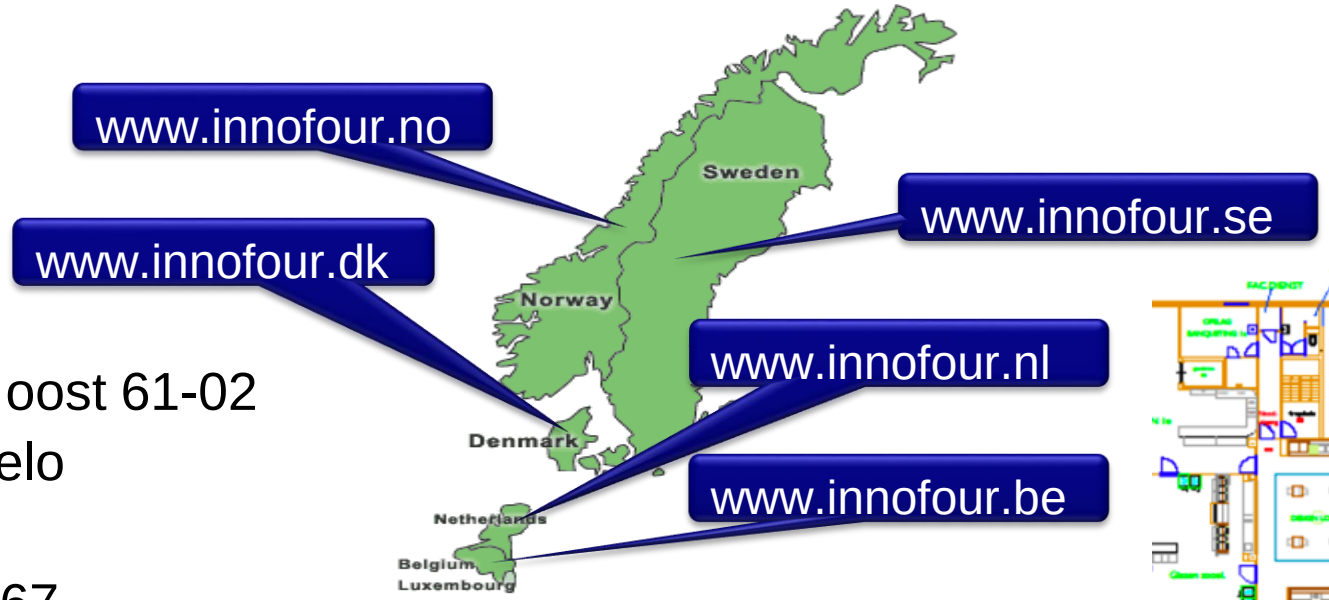
- Reduced design costs
  - Typically 50% reduction in design effort
    - Quote: "Schematics ready for PCB Layout from 10 months down to 5 months"
  - Reduced number of layers and vias means lower manufacturing costs

- Shorter design time cycle
  - Typically 30-40% less design cycle time
    - Quote: "Pin assignment effort reduced from 4-8 weeks per FPGA to 1-2 weeks per FPGA including time to compile the FPGA to check design rules"

- Minimized design errors
  - Correct-by-construction FPGA Vendor rules-driven I/O assignment, guaranteed error-free pin assignments
  - Auto-synchronization of HDL-PCB designs
  - By using prequalified or auto generated symbols

- Improved signal quality
  - 50% less trace length, 20% fewer vias means "cleaner" signals and increased timing budget
    - Every via on a trace is a discontinuity.





InnoFour

twentepoort oost 61-02
7609 rg almelo
netherlands
kvk 0817 4767

☏ + 31 (0)546 45 45 30
🖷 + 31 (0)546 45 30 06
info@innofour.com
www.innofour.com