Applying Fast and Frequent Link Health Evaluation for Root Cause Analysis and Real-World Simulation

Today’s Speakers

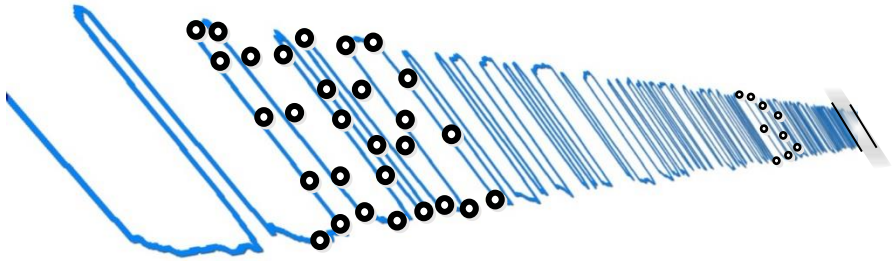
John Marrinan, Director Applications Engineers, Tektronix

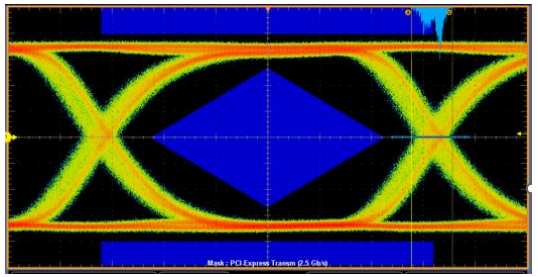
John is the director of application engineers for Tektronix in EMEA. John has over 16 years experience in the T&M industry and is an expert in signal integrity measurements for high-speed communication

Agenda

- Speaker Introduction
- Quick Introduction To A Margin Test
- Tx Testing Applications (25 min)
    - BIOS Settings & Interoperability
    - Re-Driver Gain Design & Interoperability
    - Riser Card Impacts
- Conclusions and Summary

What is a Margin Test?

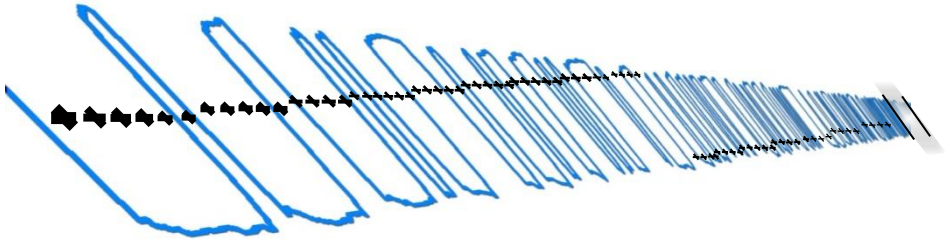


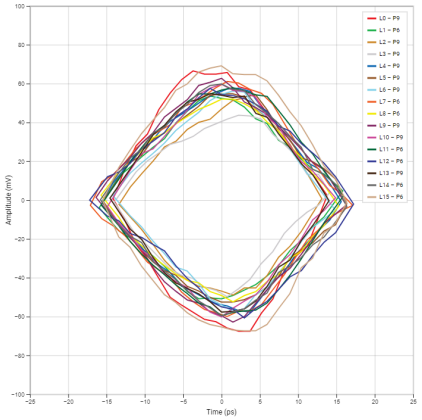


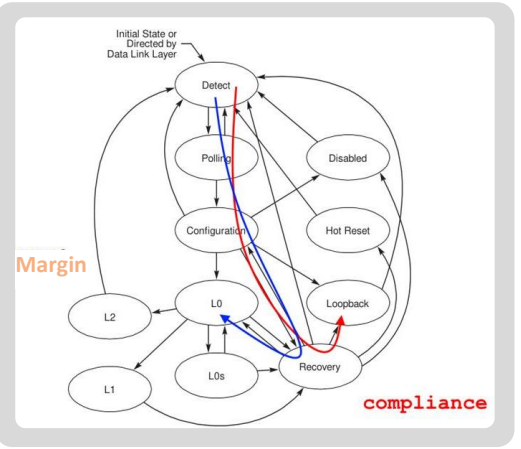
- Real Time Measurements works in Compliance mode of the State Machine under controlled setting
- Margin Measurements works in L0 State under normal operating condition

Real Time Scopes Test

High Resolution Sample but in batches.
Precision waveforms for accurate signal integrity measurement but slow and expensive.





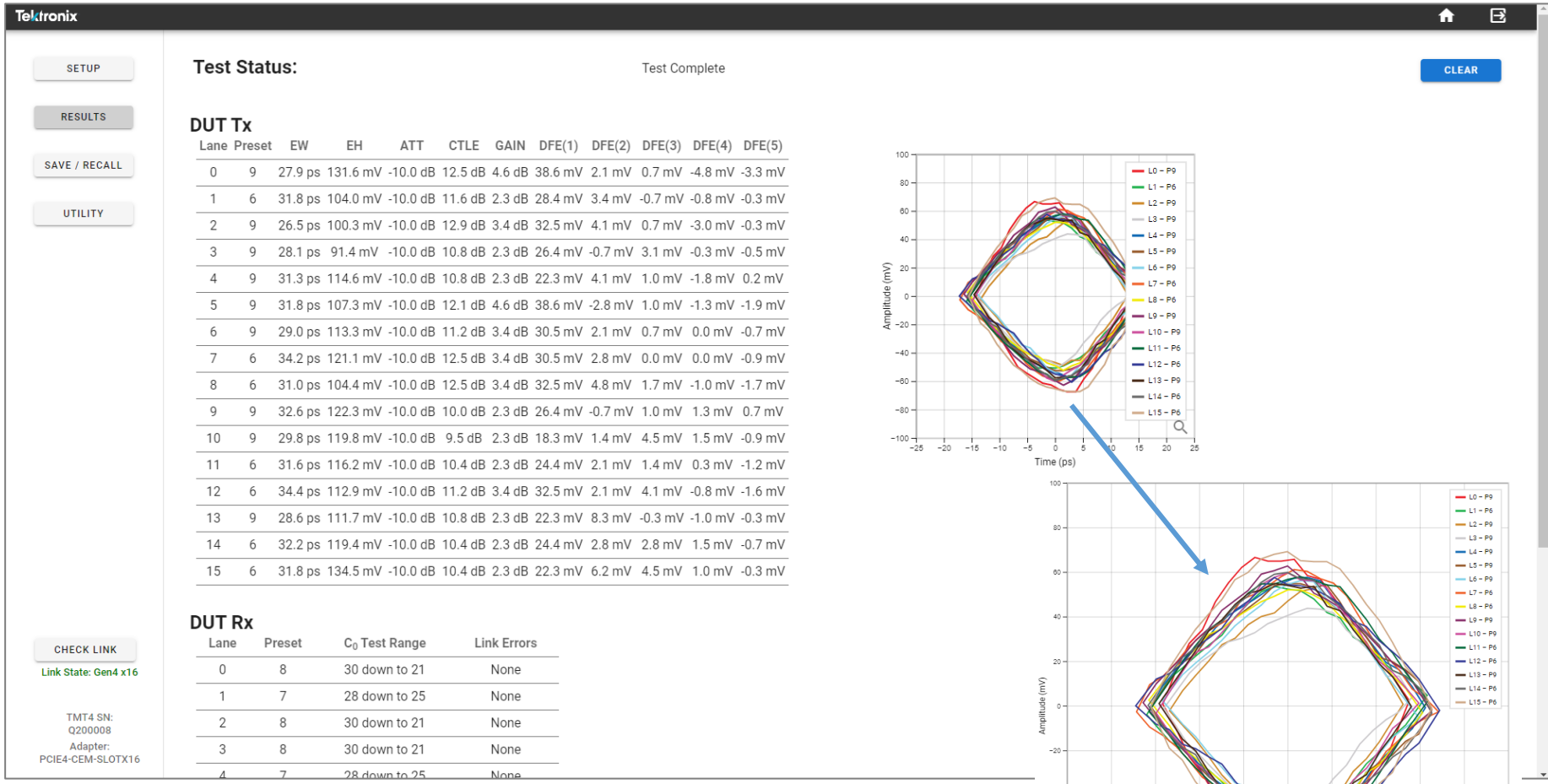


Margin Test

Every bit but missing information (similar to BERT eye).
Very fast results in a live link situation but with less accuracy

Types of Margin Tests – The Quick Scan

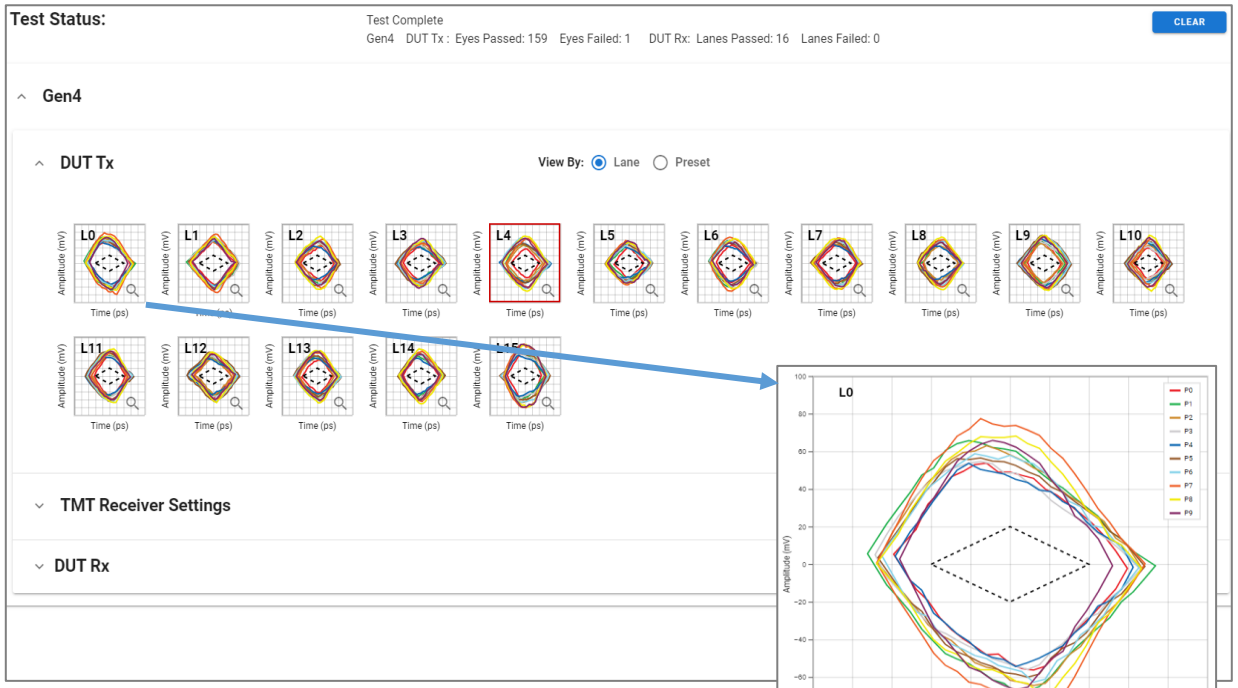
1. DUT and Margin Tester **train naturally** and negotiate presets for **Tx test**
   - Display eye diagram & link training parameters
2. DUT and Margin Tester **train naturally** and negotiate presets for **Rx Test**
   - Display outputs of Rx test range and link errors by lane/preset combination



Est. Test Time for Gen4 x16 DUTs: **2-4 minutes**

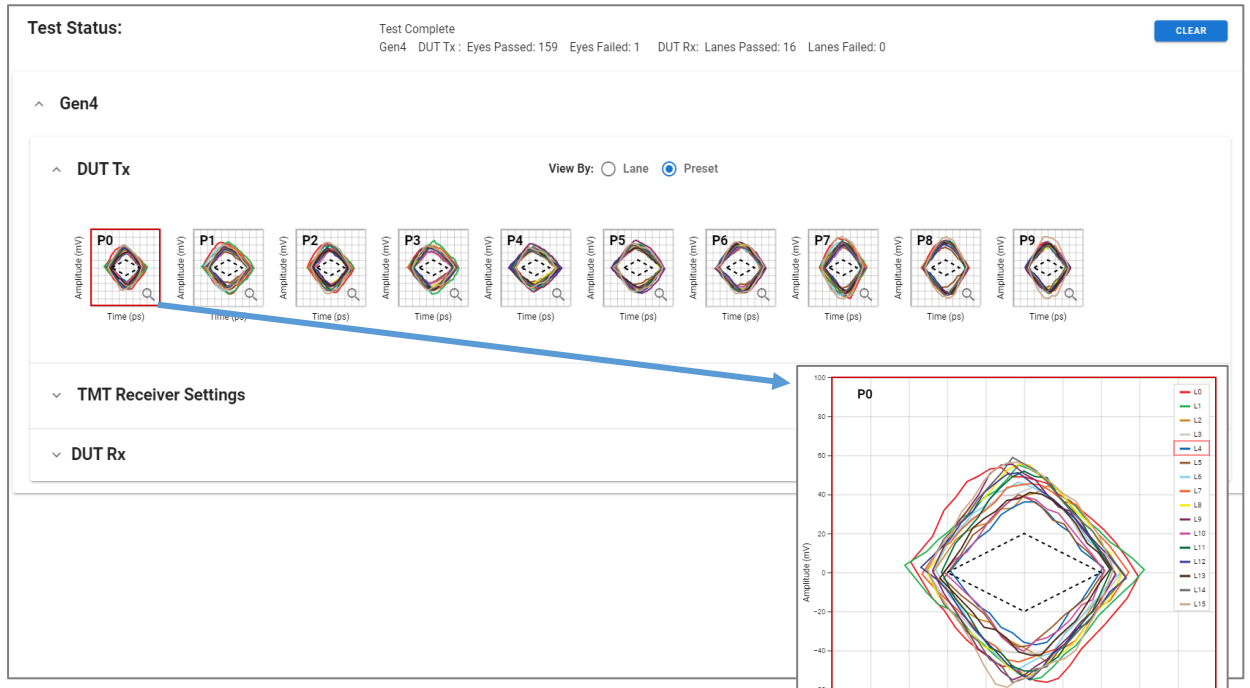
Types of Margin Tests - The Custom Scan

Presets Plotted Per Lane



1. Scanned all presets on all lanes
   - 160 combinations
2. All presets plotted together for each lane
3. Very clear that there are **lane to lane variations**

Lanes Plotted Per Preset



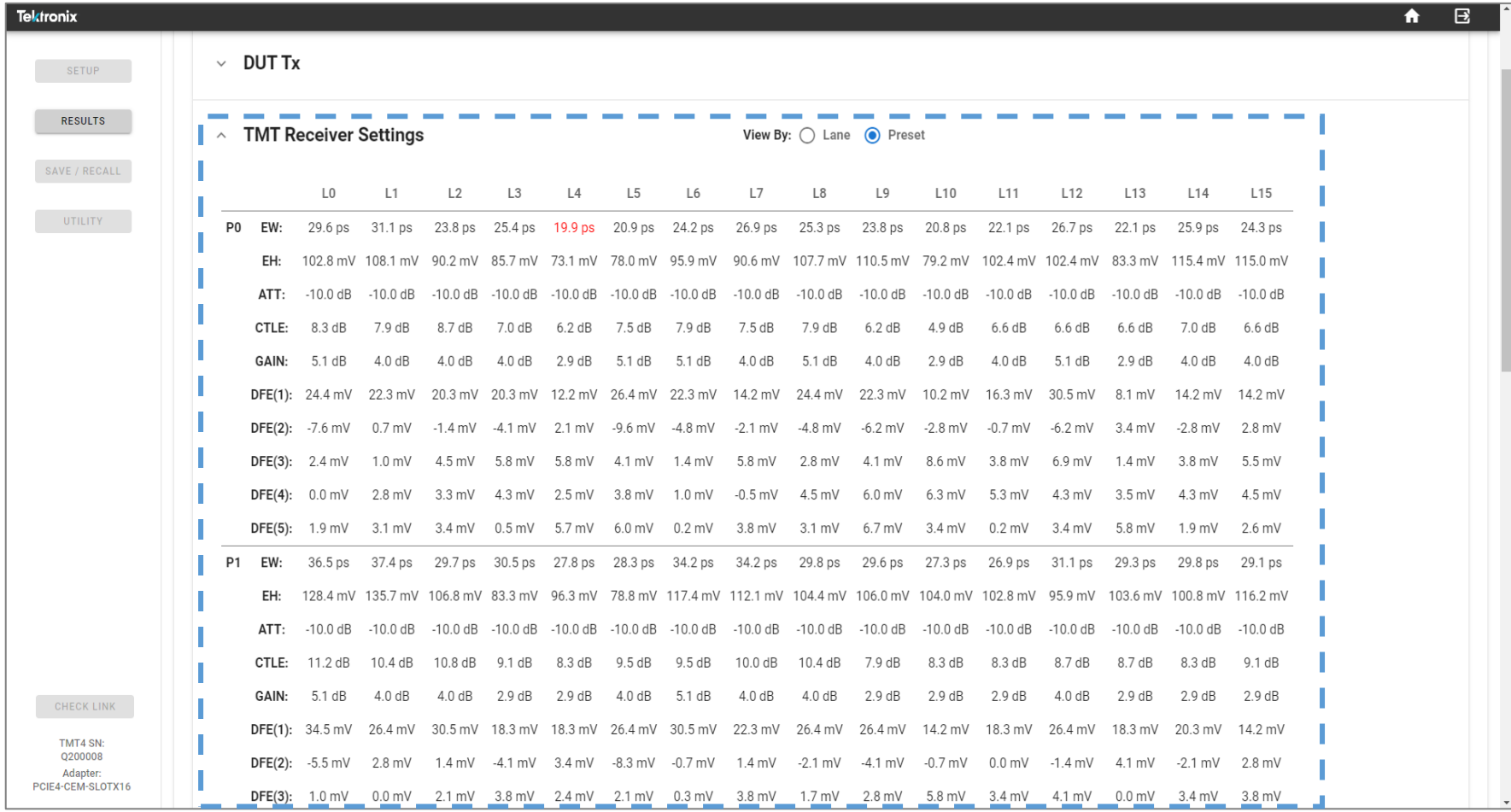
1. Scanned all presets on all lanes
   - 160 combinations
2. All lanes plotted together for each preset
3. Alternative view makes the lane-to-lane variations even clearer

Est. Test Time for Gen4 x16 DUTs: **25-30 minutes**

Custom Scan: Link Training Parameters

1

- Custom Scan by its nature of forcing setting has the ability to visualize all train Link parameters of the DUT transmitters in each Preset / Lane combination:
  - **Eye Width**
  - **Eye Height**
  - **Attenuation**
  - **Variable Gain**
  - **CTLE Boost**
  - **DFE Taps 1-5**



		L0	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15
P0	EW:	29.6 ps	31.1 ps	23.8 ps	25.4 ps	19.9 ps	20.9 ps	24.2 ps	26.9 ps	25.3 ps	23.8 ps	20.8 ps	22.1 ps	26.7 ps	22.1 ps	25.9 ps	24.3 ps
	EH:	102.8 mV	108.1 mV	90.2 mV	85.7 mV	73.1 mV	78.0 mV	95.9 mV	90.6 mV	107.7 mV	110.5 mV	79.2 mV	102.4 mV	102.4 mV	83.3 mV	115.4 mV	115.0 mV
	ATT:	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB
	CTLE:	8.3 dB	7.9 dB	8.7 dB	7.0 dB	6.2 dB	7.5 dB	7.9 dB	7.5 dB	7.9 dB	6.2 dB	4.9 dB	6.6 dB	6.6 dB	6.6 dB	7.0 dB	6.6 dB
	GAIN:	5.1 dB	4.0 dB	4.0 dB	4.0 dB	2.9 dB	5.1 dB	5.1 dB	4.0 dB	5.1 dB	4.0 dB	2.9 dB	4.0 dB	5.1 dB	2.9 dB	4.0 dB	4.0 dB
	DFE(1):	24.4 mV	22.3 mV	20.3 mV	20.3 mV	12.2 mV	26.4 mV	22.3 mV	14.2 mV	24.4 mV	22.3 mV	10.2 mV	16.3 mV	30.5 mV	8.1 mV	14.2 mV	14.2 mV
	DFE(2):	-7.6 mV	0.7 mV	-1.4 mV	-4.1 mV	2.1 mV	-9.6 mV	-4.8 mV	-2.1 mV	-4.8 mV	-6.2 mV	-2.8 mV	-0.7 mV	-6.2 mV	3.4 mV	-2.8 mV	2.8 mV
	DFE(3):	2.4 mV	1.0 mV	4.5 mV	5.8 mV	5.8 mV	4.1 mV	1.4 mV	5.8 mV	2.8 mV	4.1 mV	8.6 mV	3.8 mV	6.9 mV	1.4 mV	3.8 mV	5.5 mV
	DFE(4):	0.0 mV	2.8 mV	3.3 mV	4.3 mV	2.5 mV	3.8 mV	1.0 mV	-0.5 mV	4.5 mV	6.0 mV	6.3 mV	5.3 mV	4.3 mV	3.5 mV	4.3 mV	4.5 mV
	DFE(5):	1.9 mV	3.1 mV	3.4 mV	0.5 mV	5.7 mV	6.0 mV	0.2 mV	3.8 mV	3.1 mV	6.7 mV	3.4 mV	0.2 mV	3.4 mV	5.8 mV	1.9 mV	2.6 mV
P1	EW:	36.5 ps	37.4 ps	29.7 ps	30.5 ps	27.8 ps	28.3 ps	34.2 ps	34.2 ps	29.8 ps	29.6 ps	27.3 ps	26.9 ps	31.1 ps	29.3 ps	29.8 ps	29.1 ps
	EH:	128.4 mV	135.7 mV	106.8 mV	83.3 mV	96.3 mV	78.8 mV	117.4 mV	112.1 mV	104.4 mV	106.0 mV	104.0 mV	102.8 mV	95.9 mV	103.6 mV	100.8 mV	116.2 mV
	ATT:	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB	-10.0 dB
	CTLE:	11.2 dB	10.4 dB	10.8 dB	9.1 dB	8.3 dB	9.5 dB	9.5 dB	10.0 dB	10.4 dB	7.9 dB	8.3 dB	8.3 dB	8.7 dB	8.7 dB	8.3 dB	9.1 dB
	GAIN:	5.1 dB	4.0 dB	4.0 dB	2.9 dB	2.9 dB	4.0 dB	5.1 dB	4.0 dB	4.0 dB	2.9 dB	2.9 dB	2.9 dB	4.0 dB	2.9 dB	2.9 dB	2.9 dB
	DFE(1):	34.5 mV	26.4 mV	30.5 mV	18.3 mV	18.3 mV	26.4 mV	30.5 mV	22.3 mV	26.4 mV	26.4 mV	14.2 mV	18.3 mV	26.4 mV	18.3 mV	20.3 mV	14.2 mV
	DFE(2):	-5.5 mV	2.8 mV	1.4 mV	-4.1 mV	3.4 mV	-8.3 mV	-0.7 mV	1.4 mV	-2.1 mV	-4.1 mV	-0.7 mV	0.0 mV	-1.4 mV	4.1 mV	-2.1 mV	2.8 mV
	DFE(3):	1.0 mV	0.0 mV	2.1 mV	3.8 mV	2.4 mV	2.1 mV	0.3 mV	3.8 mV	1.7 mV	2.8 mV	5.8 mV	3.4 mV	4.1 mV	0.0 mV	3.4 mV	3.8 mV

Agenda

- Speaker Intros
- Quick Introduction of TMT4 Margin Tester (5 min)
- Example Tx Testing Applications (25 min)
  - BIOS Settings & Interoperability
  - Re-Driver Gain Design & Interoperability
  - Riser Card Impacts
- Conclusions and Summary

Original vs Updated BIOS Settings

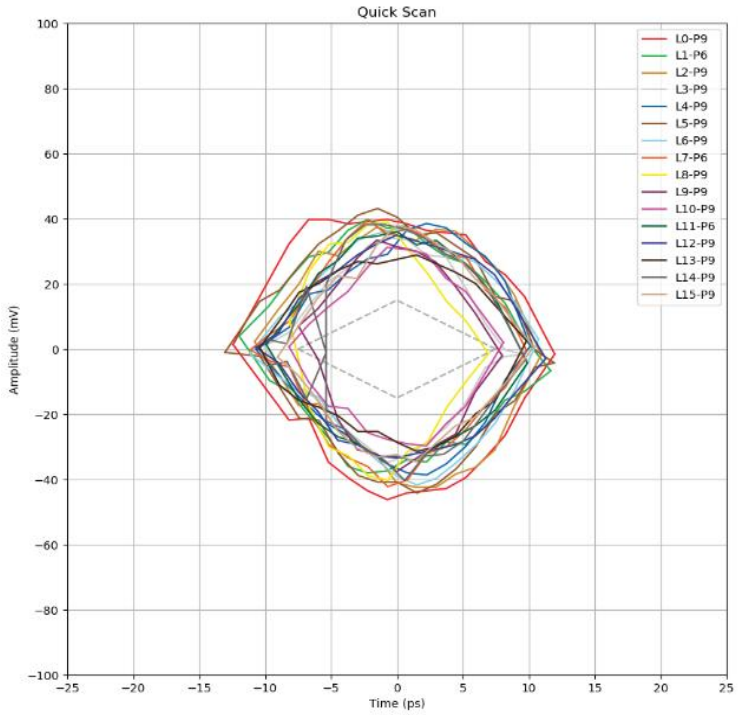
A motherboard manufacturer had a board that was passing compliance but wanted to improve the eye height and width by adjusting BIOS settings.

After adjusting the BIOS, we compared changes for the first 4 lanes and the system still passed compliance with little change in eye height and width. However, with the new BIOS settings they saw more interoperability issues that with the original settings:

		Compliance Test Results							
Lane	Preset	Original BIOS Settings			Updated BIOS Settings			Delta (Old to New)	
		Eye Height	Eye Width	Result	Eye Height	Eye Width	Result	Eye Height	Eye Width
4	8	68.843 mV	28.394 ps	Pass	68.737 mV	27.586 ps	Pass	-0.106 mV	-0.808 ps
2	8	71.164 mV	27.968 ps	Pass	73.628 mV	28.575 ps	Pass	2.464 mV	0.606 ps
2	7	79.190 mV	22.086 ps	Pass	80.360 mV	21.812 ps	Pass	1.170 mV	-0.273 ps
1	8	82.233 mV	29.086 ps	Pass	77.147 mV	29.218 ps	Pass	-5.086 mV	0.132 ps
1	7	86.544 mV	22.721 ps	Pass	85.649 mV	23.772 ps	Pass	-0.894 mV	1.051 ps
1	6	50.349 mV	32.812 ps	Pass	49.421 mV	33.261 ps	Pass	-0.927 mV	0.449 ps
0	8	71.097 mV	29.982 ps	Pass	70.482 mV	29.697 ps	Pass	-0.614 mV	-0.285 ps
0	7	78.126 mV	24.648 ps	Pass	77.035 mV	25.551 ps	Pass	-1.091 mV	0.902 ps
0	6	41.237 mV	33.345 ps	Pass	40.164 mV	32.964 ps	Pass	-1.073 mV	-0.381 ps

Identify Original BIOS Settings Using Quick Scan

To draw more insight into the issue, a Margin Tester was used to scan the 16-lane bus as a live link partner and trained to naturally negotiated presets, with the results below:



TMT4 Margin Tester Results

lane	preset	eye_width	eye_height	att	vga	ctle	dfe1	dfe2	dfe3	dfe4	dfe5
4	6	22.32	67.03	-6.58	2.28	6.61	26.4	-8.25	9.28	2.75	4.29
2	9	22.15	85.72	-10	1.71	5.77	22.34	-14.44	6.53	3.75	3.43
1	9	20.99	83.69	-8.86	2.28	7.45	24.37	-5.5	6.18	2.75	2.92
0	9	22.86	92.63	-8.86	2.28	6.61	28.43	-10.32	7.9	3	3.95

Updated BIOS Presets

Lane	Preset
4	8
2	8
2	7
1	8
1	7
1	6
0	8
0	7
0	6

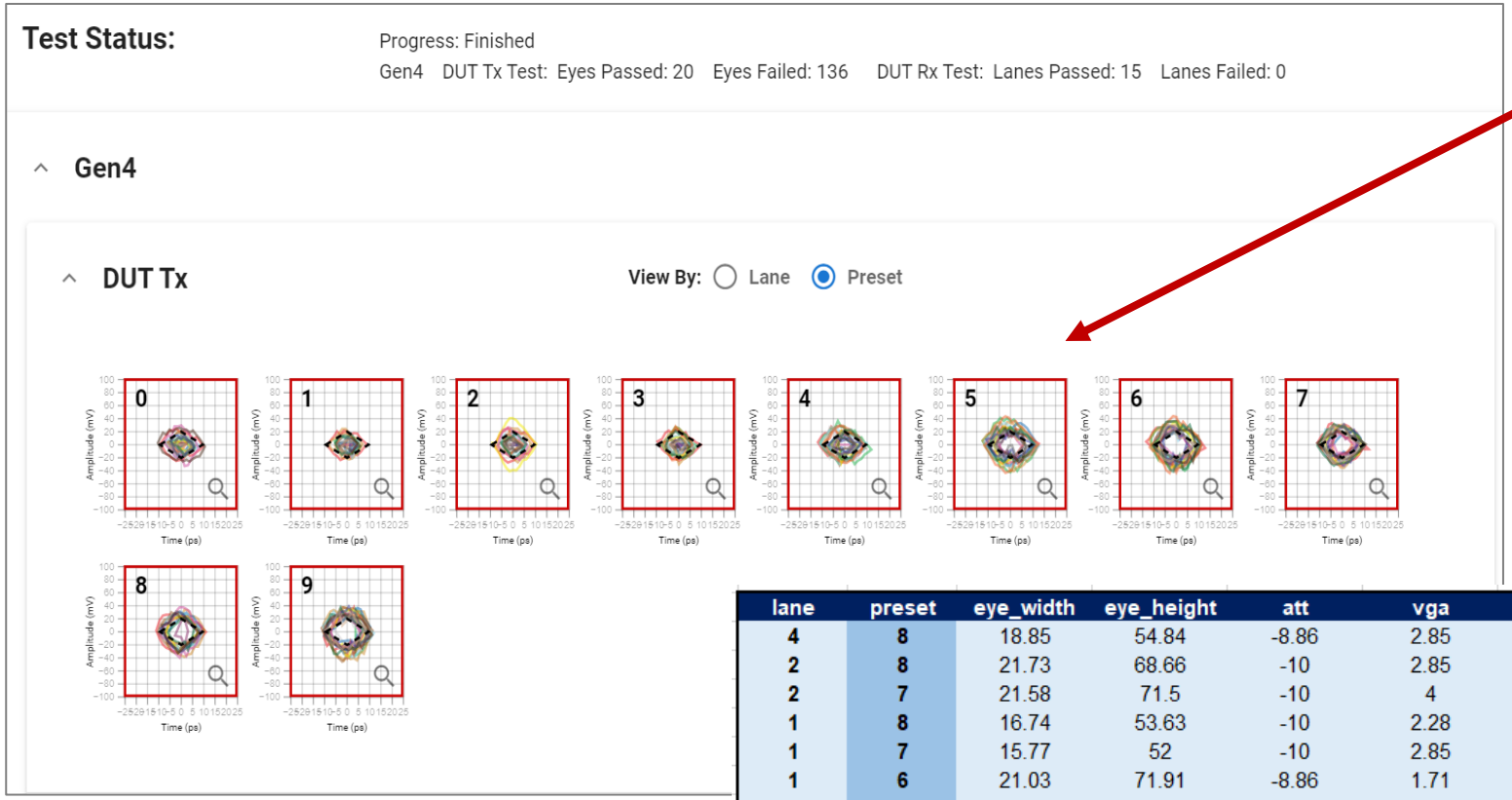
DUT did not naturally train to any of the presets eventually updated in the BIOS

Equalization was heavily used to form the link – especially DFE 1 where each lane pushed the tap to ~half of its typical range

	dfe1	dfe2	dfe3	dfe4	dfe5
Low	-55.0 mV	-44.0 mV	-22.0 mV	-16.0 mV	-11.0 mV
High	55.0 mV	43.0 mV	21.7 mV	15.8 mV	10.8 mV

Understand Preset Performance For BIOS Settings Using A Custom Scan

Next the Margin Tester was used for a custom scan to look at the specific lanes and presets of interest:



Overall, the DUT Tx link eyes looks generally poor across the entire design;

Shows why vendor was generally interested in tuning P6-P9.

Equalization even worse on some of the settings that would eventually be updated. Especially high use of DFE taps 1, 2, 5.

lane	preset	eye_width	eye_height	att	vga	ctle	dfe1	dfe2	dfe3	dfe4	dfe5
4	8	18.85	54.84	-8.86	2.85	3.67	30.46	-14.44	7.9	6	6.18
2	8	21.73	68.66	-10	2.85	3.67	28.43	-17.19	3.78	6.75	4.98
2	7	21.58	71.5	-10	4	2.83	44.68	-16.5	2.75	8.25	6.01
1	8	16.74	53.63	-10	2.28	3.67	22.34	-12.38	5.5	6	4.29
1	7	15.77	52	-10	2.85	2.83	30.46	-13.75	4.81	6.5	4.98
1	6	21.03	71.91	-8.86	1.71	7.87	22.34	-10.32	3.78	2.75	1.89
0	8	22.32	67.44	-10	1.71	3.67	30.46	-15.82	4.46	4	6.01
0	7	23.62	67.44	-10	2.85	2.83	36.56	-16.5	3.78	5.75	8.07
0	6	25.05	62.97	-8.86	1.71	6.19	30.46	-13.75	5.15	3.75	3.26

Original BIOS Settings – Inspect Particular Lanes

Next the Margin Tester was used for a custom scan to look at the specific lanes and presets of interest:

Lane	Preset	Original BIOS Settings		
		Eye Height	Eye Width	Result
4	8	68.843 mV	28.394 ps	Pass
2	8	71.164 mV	27.968 ps	Pass
2	7	79.190 mV	22.086 ps	Pass
1	8	82.233 mV	29.086 ps	Pass
1	7	86.544 mV	22.721 ps	Pass
1	6	50.349 mV	32.812 ps	Pass
0	8	71.097 mV	29.982 ps	Pass
0	7	78.126 mV	24.648 ps	Pass
0	6	41.237 mV	33.345 ps	Pass

lane	preset	eye_width	eye_height	att	vga	ctle	dfe1	dfe2	dfe3	dfe4	dfe5
4	8	18.85	54.84	-8.86	2.85	3.67	30.46	-14.44	7.9	6	6.18
2	8	21.73	68.66	-10	2.85	3.67	28.43	-17.19	3.78	6.75	4.98
2	7	21.58	71.5	-10	4	2.83	44.68	-16.5	2.75	8.25	6.01
1	8	16.74	53.63	-10	2.28	3.67	22.34	-12.38	5.5	6	4.29
1	7	15.77	52	-10	2.85	2.83	30.46	-13.75	4.81	6.5	4.98
1	6	21.03	71.91	-8.86	1.71	7.87	22.34	-10.32	3.78	2.75	1.89
0	8	22.32	67.44	-10	1.71	3.67	30.46	-15.82	4.46	4	6.01
0	7	23.62	67.44	-10	2.85	2.83	36.56	-16.5	2.78	5.75	8.07
0	6	25.05	62.97	-8.86	1.71	6.19	30.46	-13.75	5.15	3.75	3.26

Lane	Preset	Compliance Test		TMT4		Delta	
		Eye Height	Eye Width	Eye Height	Eye Width	Eye Height	Eye Width
4	8	68.843 mV	28.394 ps	54.84 mV	18.85 ps	-14.003	-9.544
2	8	71.164 mV	27.968 ps	68.66 mV	21.73 ps	-2.504	-6.238
2	7	79.190 mV	22.086 ps	71.5 mV	21.58 ps	-7.69	-0.506
1	8	82.233 mV	29.086 ps	53.63 mV	16.74 ps	-28.603	-12.346
1	7	86.544 mV	22.721 ps	52 mV	15.77 ps	-34.544	-6.951
1	6	50.349 mV	32.812 ps	71.91 mV	21.03 ps	21.561	-11.782
0	8	71.097 mV	29.982 ps	67.44 mV	22.32 ps	-3.657	-7.662
0	7	78.126 mV	24.648 ps	67.44 mV	23.62 ps	-10.686	-1.028
0	6	41.237 mV	33.345 ps	62.97 mV	25.05 ps	21.733	-8.295

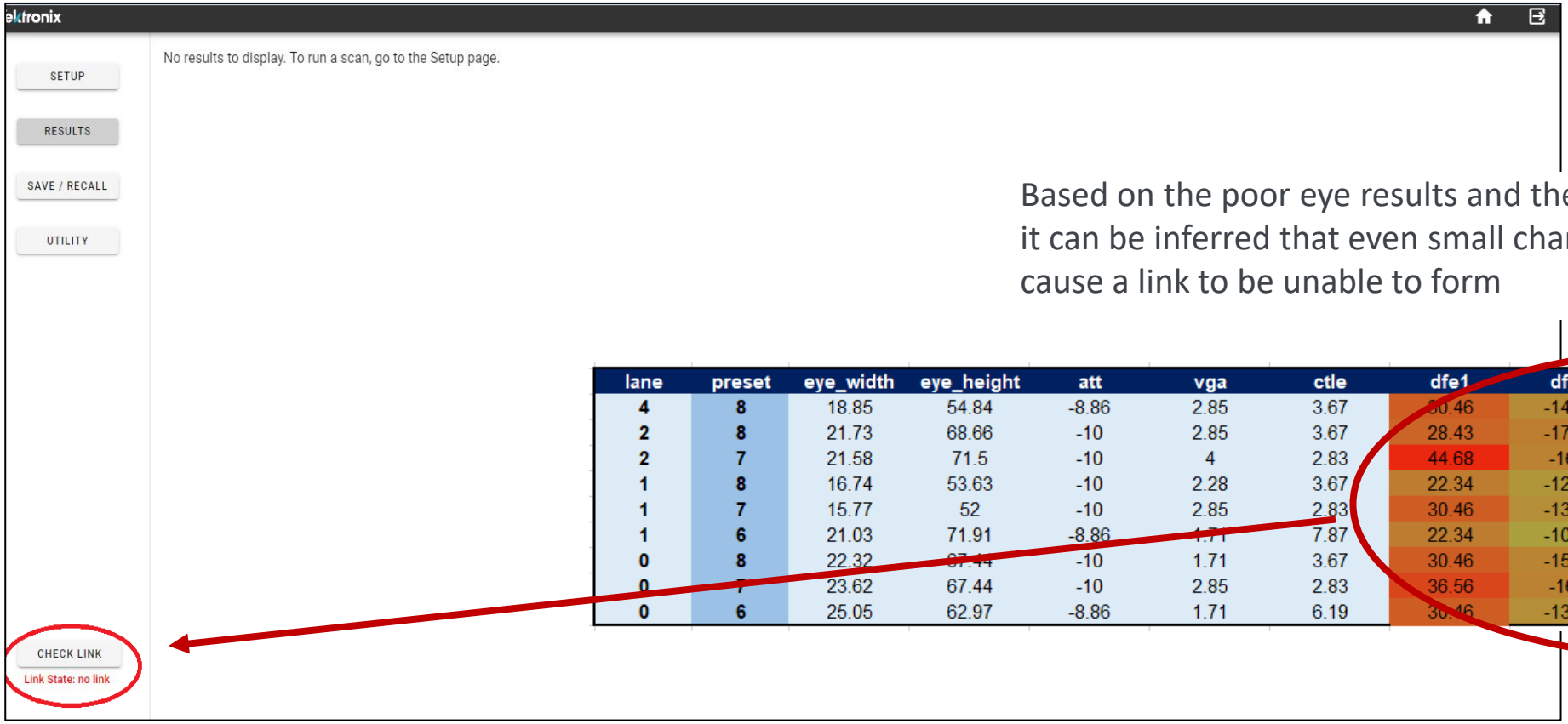
Lane 1 P7 and P8 showed significantly worse results than compliance results;

These lanes are not behaving as well in a live link test

Some especially bad areas – the Margin Tester receivers are working hard to form a link with this DUT

Updated BIOS Settings

When the Margin Tester was used to scan the device with updated BIOS settings, it was unable to even form a link (expected outcome).



Based on the poor eye results and the heavy use of equalization, it can be inferred that even small changes in BIOS settings could cause a link to be unable to form

lane	preset	eye_width	eye_height	att	vga	ctle	dfe1	dfe2	dfe3	dfe4	dfe5
4	8	18.85	54.84	-8.86	2.85	3.67	30.46	-14.44	7.9	6	6.18
2	8	21.73	68.66	-10	2.85	3.67	28.43	-17.19	3.78	6.75	4.98
2	7	21.58	71.5	-10	4	2.83	44.68	-16.5	2.75	8.25	6.01
1	8	16.74	53.63	-10	2.28	3.67	22.34	-12.38	5.5	6	4.29
1	7	15.77	52	-10	2.85	2.83	30.46	-13.75	4.81	6.5	4.98
1	6	21.03	71.91	-8.86	1.71	7.87	22.34	-10.32	3.78	2.75	1.89
0	8	22.32	67.44	-10	1.71	3.67	30.46	-15.82	4.46	4	6.01
0	7	23.62	67.44	-10	2.85	2.83	36.56	-16.5	3.78	5.75	8.07
0	6	25.05	62.97	-8.86	1.71	6.19	30.46	-13.75	5.15	3.75	3.26

Conclusions

1. **In about 35 minutes of testing, the user was able to learn more about the health of their PCIe design in a live link and determine that, in general, the design is right on the edge of interoperability issues.**

2. **PCIe compliant devices can still have interop issues, and it can often be difficult to resolve once you've passed compliance.**

3. **Results from the Original BIOS settings quickly shows that the equalization across the lanes and presets of interest was heavily used.**

   This outcome likely explains why even subtle updates to the BIOS led to much larger interop issues than the original BIOS settings.

A Real Time Measurement Could Take Several Days and a Skilled SI Engineer to Capture Similar Comparative Results. A Margin Test Saves Time and Expensive Resources in The Lab

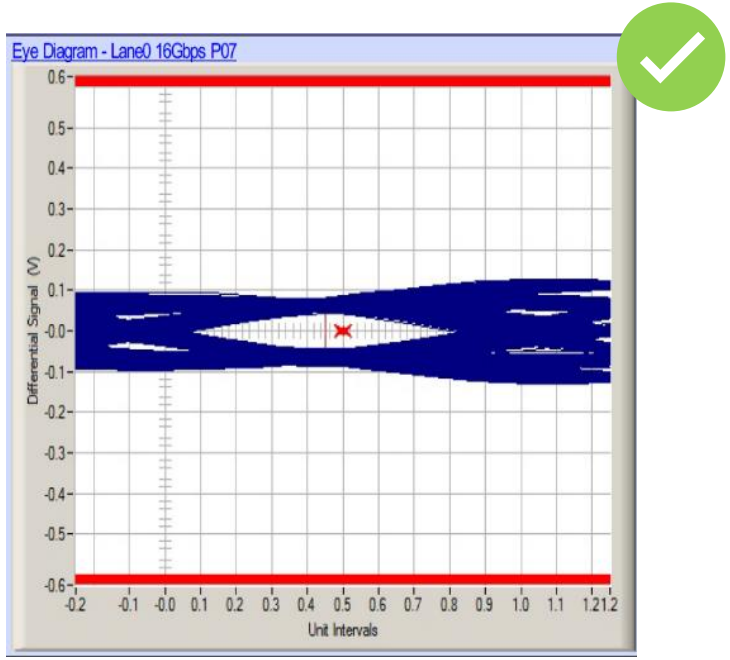
Agenda

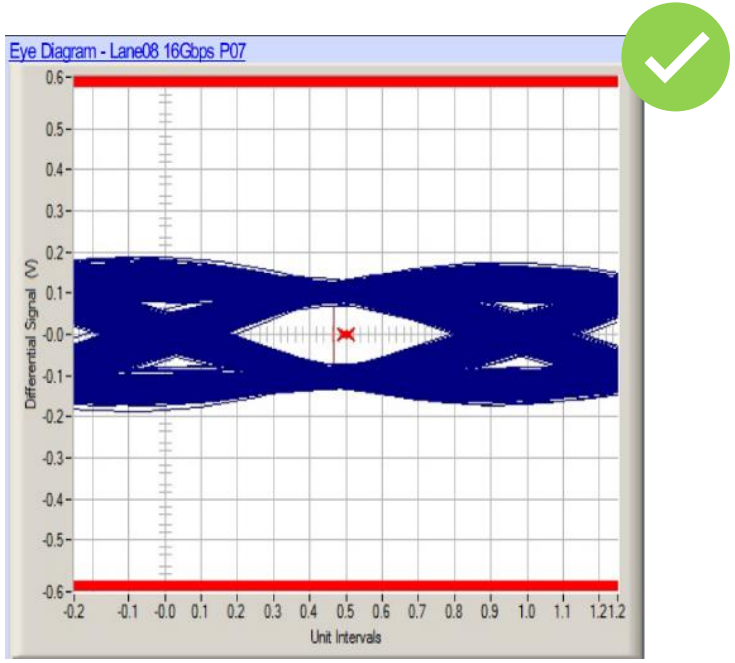
- Speaker Intros
- Quick Introduction of TMT4 Margin Tester (5 min)
- Tx Testing Applications (25 min)
  - BIOS Settings & Interoperability
  - Re-Driver Gain Design & Interoperability
  - Riser Card Impacts
- Conclusions and Summary

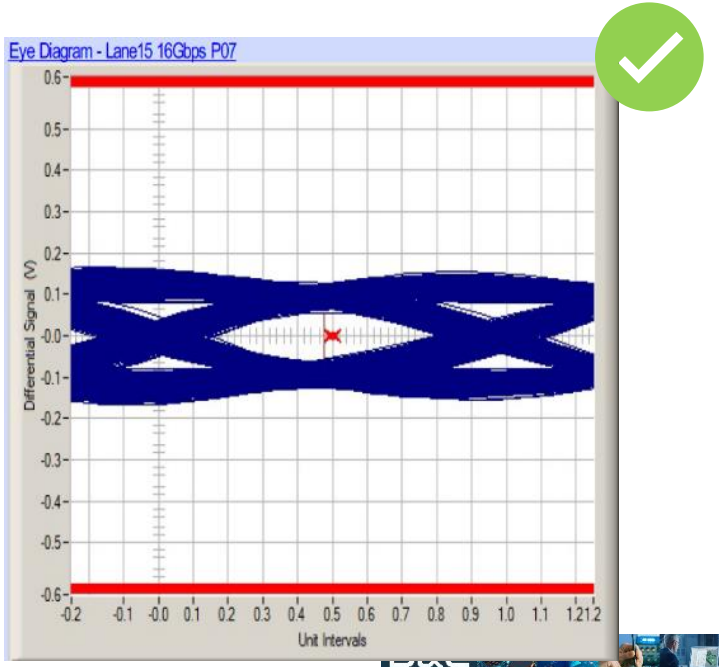
Investigating Gen 4 Re-Driver Design Issue

A motherboard manufacturer was attempting to resolve an issue they were seeing with their re-driver gain setup.

They had used the reference design from their silicon vendor and were seeing passing results using Real Time Scope and PCIe Sign Test as shown in the diagrams below for lanes 0, 8, and 15.







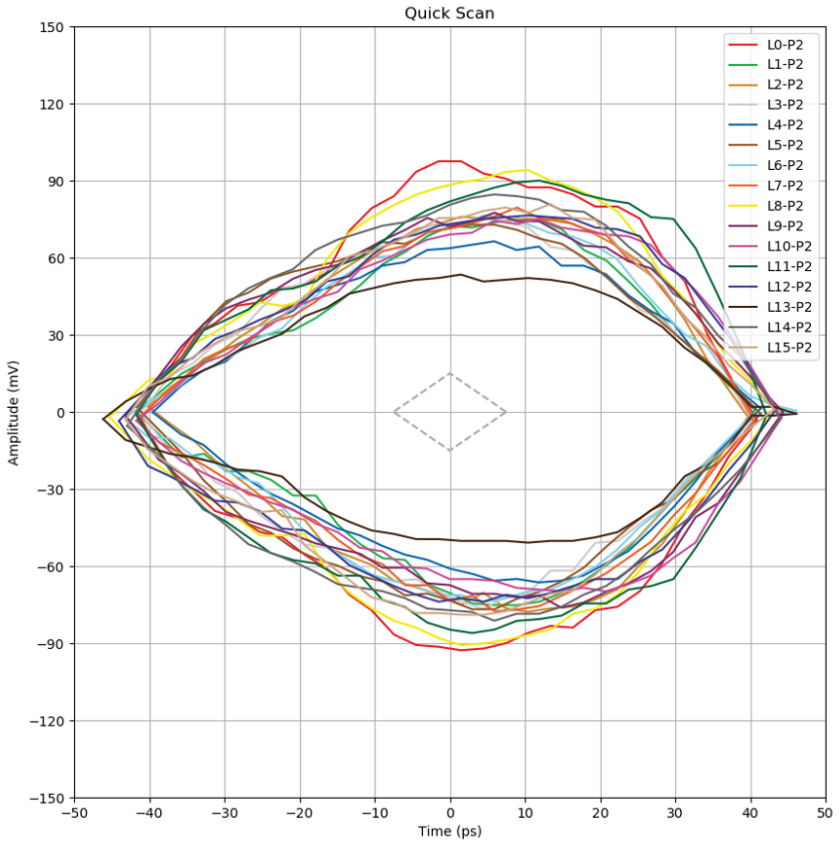
Margin Tester Results – Scanning at Gen 4

Despite these passing results, the manufacturer has been experiencing interoperability issues that they were unable to root-cause.

Using a Margin Tester at Gen 4 speeds, they also ran into interop issues:

Margin Tester Results – Gen 3

To try to draw insight into the interop issues, the Margin Tester was used to run a Quick Scan at Gen 3 speeds. It was able to link and test at Gen 3. Results and insights below:



lane	preset	eye_width	eye_height	att	vga	ctle	dfe1	dfe2	dfe3	dfe4	dfe5
0	2	82.6	190.3	-8.86	2.28	3.67	-2.04	0	7.21	1	1.71
1	2	82.3	150.3	-8.86	1.71	4.51	-12.19	8.25	5.15	0.25	0.68
2	2	79.9	153.0	-10	1.14	4.09	-6.1	0.68	2.06	1	0.85
3	2	81.5	152.3	-8.86	1.14	4.09	-10.16	1.37	1.03	-2	2.75
4	2	80.9	132.0	-7.72	1.14	3.25	4.06	4.12	2.4	1.5	3.78
5	2	83.0	149.6	-8.86	1.14	3.67	-2.04	3.43	3.78	2	3.26
6	2	89.3	150.3	-8.86	1.14	3.25	2.03	1.37	2.06	-0.25	3.26
7	2	82.2	156.4	-7.72	1.14	3.67	0	2.06	3.09	-0.25	2.92
8	2	88.5	182.1	-7.72	0	2	-18.29	-4.82	-1.04	-3.25	1.03
9	2	87.5	148.3	-5.43	0.57	2	-12.19	-4.13	-0.69	-3.25	-0.69
10	2	85.9	144.2	-7.72	0	2	-14.22	[illegible]	-1.38	-1.75	0.34
11	2	83.9	172.0	-7.72	0	2	-20.32	-3.44	-3.44	-1.25	-2.07
12	2	87.3	149.0	-7.72	0.57	2	-2.04	0.68	[illegible]	-2.25	1.2
13	2	92.3	103.6	-8.86	0	2	-2.04	3.43	-2.41	-1.5	-0.52
14	2	87.0	165.9	[illegible]	0	2	-8.13	-2.75	-1.04	[illegible]	0.51
15	2	86.3	157.1	-7.72	0.57	2	-8.13	6.87	2.4	-1.25	1.03

Equalization of lanes 8-11 and eye height of lane 13 indicate potential issues with the back 8 lanes of the re-driver design

Lane 13 eye almost half the height of Lane 0 eye

Higher levels of DFE 1 equalization for lanes 8-11 compared to all other lanes

Conclusions

1. **In just 5 minutes of testing, the user was able to identify that the problems with their re-driver setup likely lies in the back 8 lanes of their re-driver setup.**

2. **The Margin Tester also replicated the interoperability issues that were seen at Gen 4 speeds, but, with a quick Gen 3 test, were able to identify lanes 8-11 and 13 as the primary lanes of interest for causing their interop issues at Gen 4 speeds.**

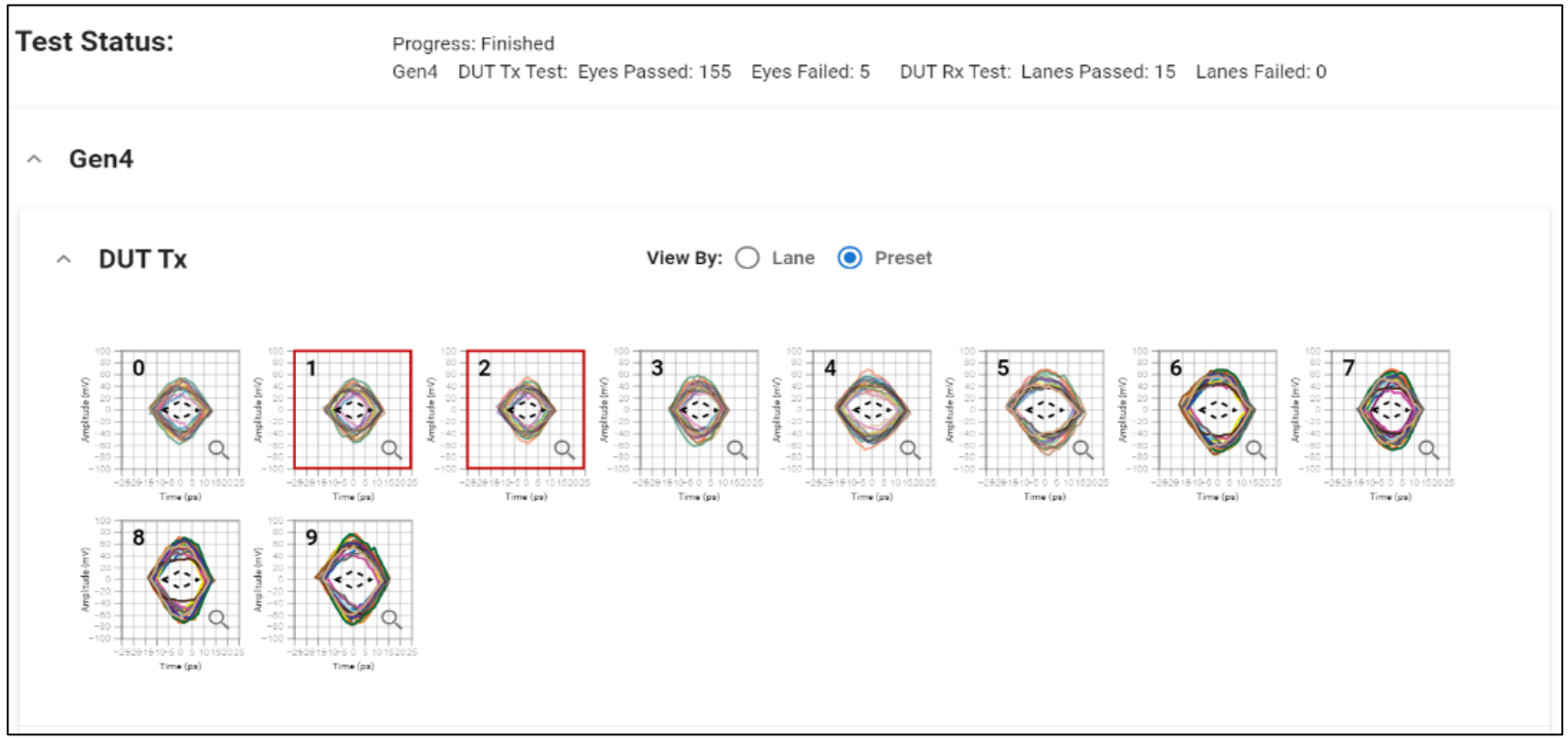
Here a Margin Test Has Very Quickly Found The Location of The Problem and Given The Design Team The Direction on Where To Investigate Root Cause Using Real Time Measurement, Simulation, or Firmware Settings

Agenda

- Speaker Intros
- Quick Introduction of TMT4 Margin Tester (5 min)
- Tx Testing Applications (25 min)
  - BIOS Settings & Interoperability
  - Re-Driver Gain Design & Interoperability
  - Riser Card Impacts
- Conclusions and Summary

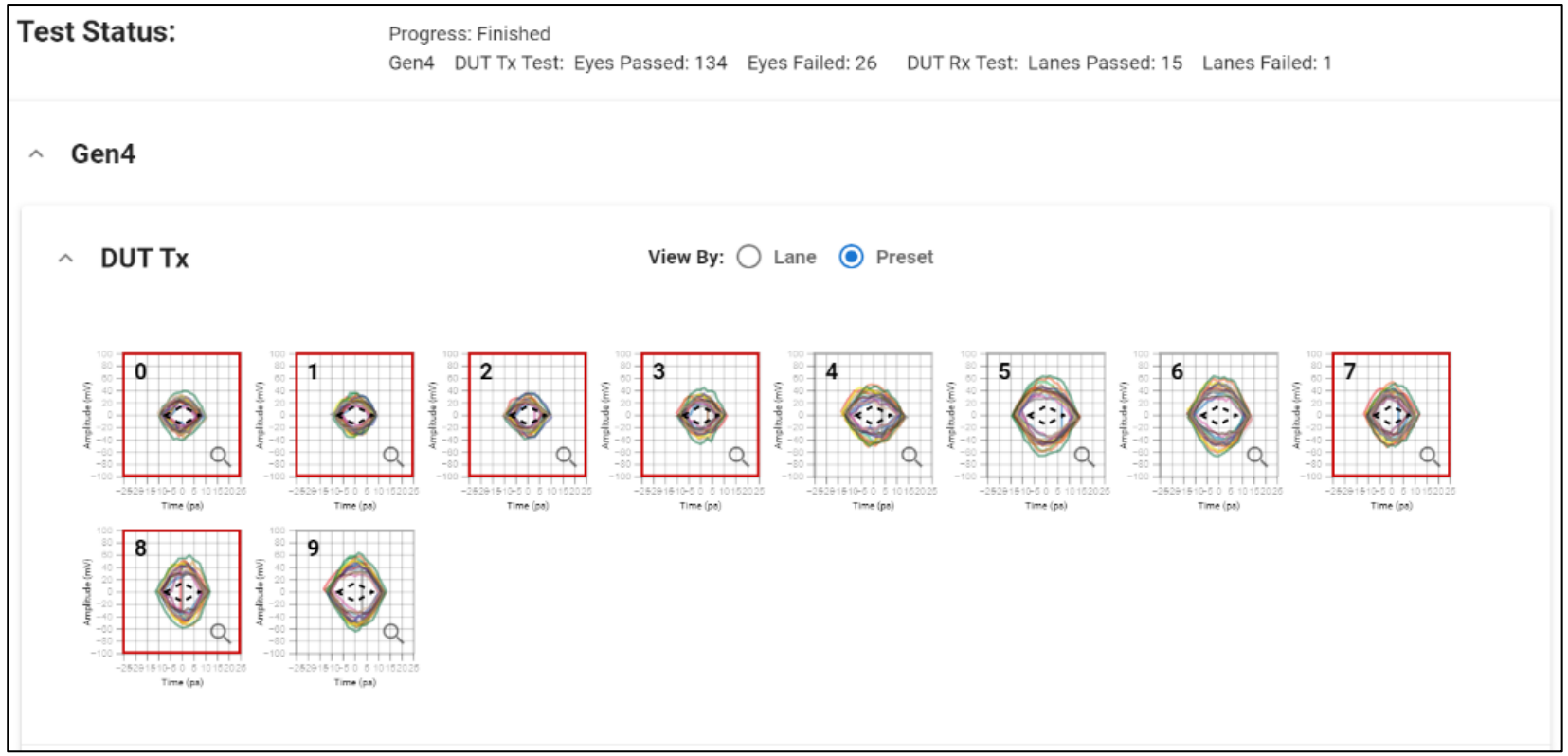
Custom Scan – No Riser Card in Signal Path

In order to demonstrate the impact of riser cards on signal integrity, a Margin Tester was hooked up to a DUT with and without a riser card in the signal path. A screenshot of the custom scan without the riser card is below:



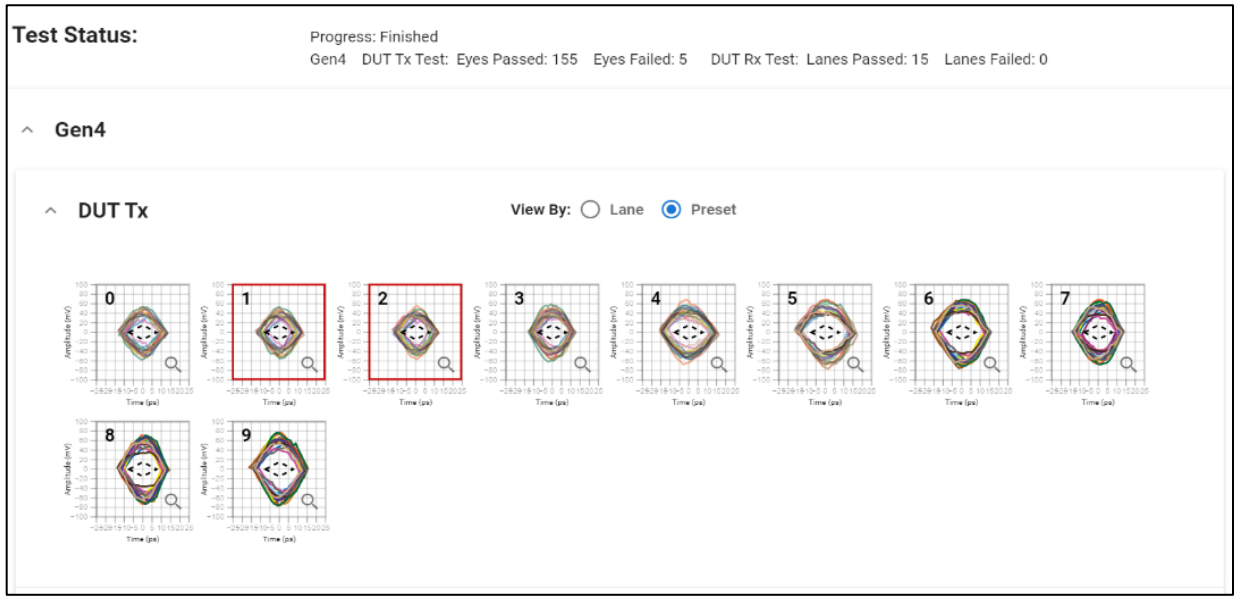
Custom Scan – Riser Card in Signal Path

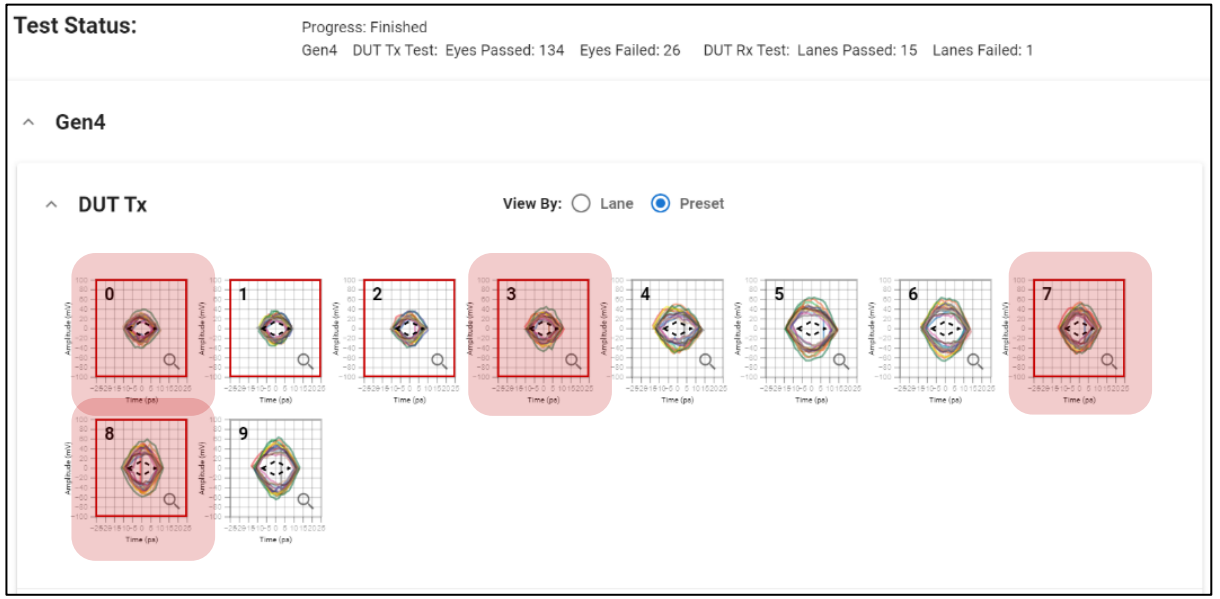
After the custom scan without the riser card, a riser card was added to the signal path to show a quick visual representation of the impact. The results of the custom scan with the riser card in the signal path is below:



Comparison: No Riser Card vs Riser Card

Putting the two scans side by side, it can easily be seen that there was noticeable signal degradation from the addition of the riser card. Eye diagrams generally got smaller, and it pushed some to fail using the same pass/fail mask:





Conclusions

1. **In just 60 minutes of testing, a user can see the impacts of a riser card on the live link DUT Tx eye diagrams across 160 lane-preset combinations.**

2. **Without even looking at receiver settings, it is clear to the user just by coming eye diagrams that there are noticeable impacts from the riser cards.**

   Using the same pass/fail mask, 20 more eyes failed with the riser cards than without, and all eyes were noticeably smaller across presets.

Agenda

- Speaker Intros
- Quick Introduction of TMT4 Margin Tester (5 min)
- Tx Testing Applications (25 min)
  - BIOS Settings & Interoperability
  - Re-Driver Gain Design & Interoperability
  - Riser Card Impacts
- Conclusions and Summary

Conclusions and Key Learnings

1. Margin Testing is a brand-new category of T&M measurements focused on time to insight and ease of use in High-Speed Serial Interfaces

2. There are several applications where there is a need for a new category of test equipment to:

    1) Draw more insight into interoperability issues
    2) Track DUT link health progress over design phases
    3) Investigate how different DUTs perform in a live link
    4) Evaluate the effect of certain riser cards on the link
    5) Quickly estimate Tx and Rx link health

Tektronix®

Thank you for joining!