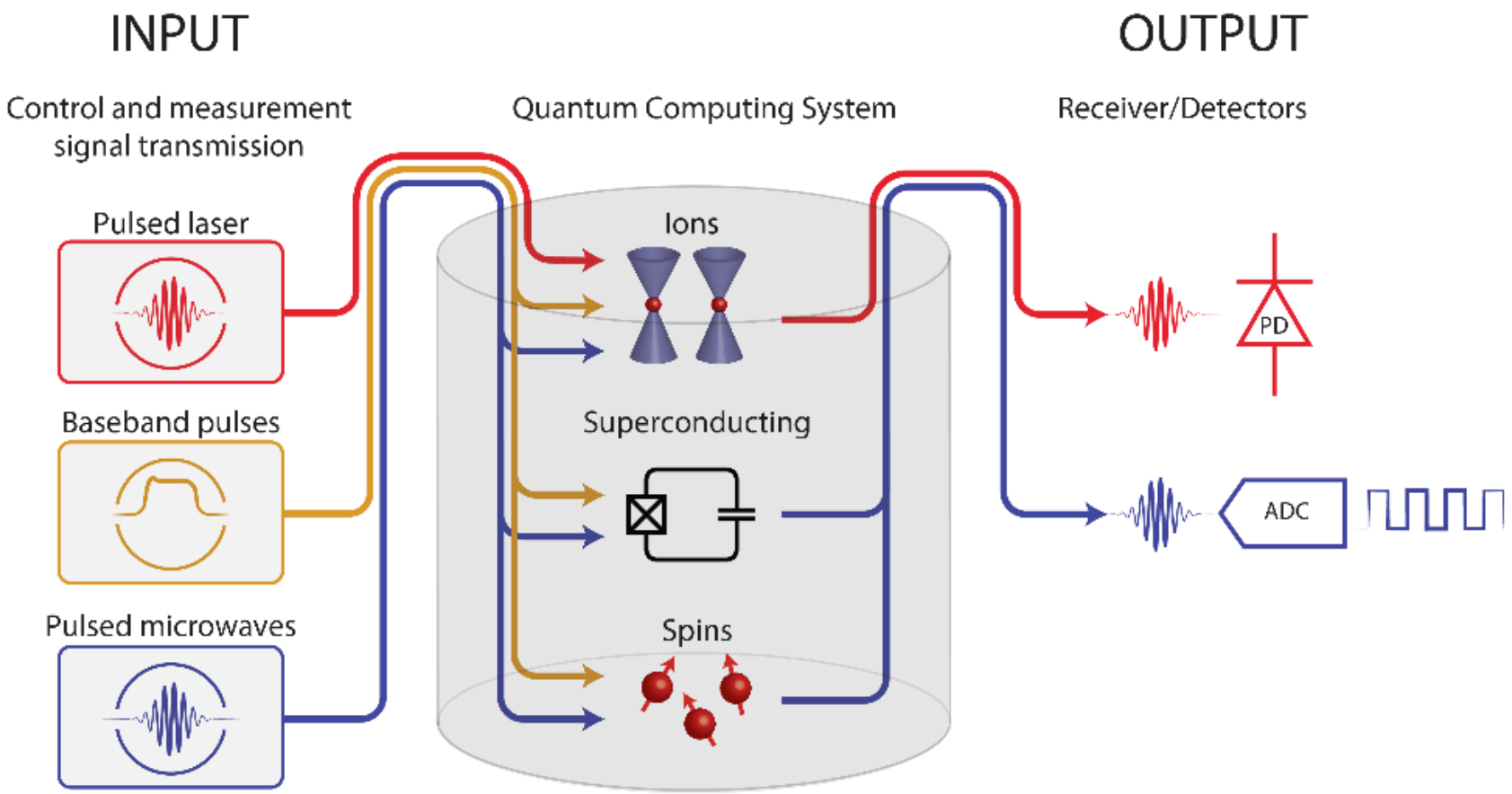
FPGA IP Designs for Multiqubit Control System

- Control of Quantum Systems
- Current Challenges:
  - Synchronization and Dynamic Flow Control
  - Efficient Signal Generation
  - Real-Time Signal Processing
- Future Work

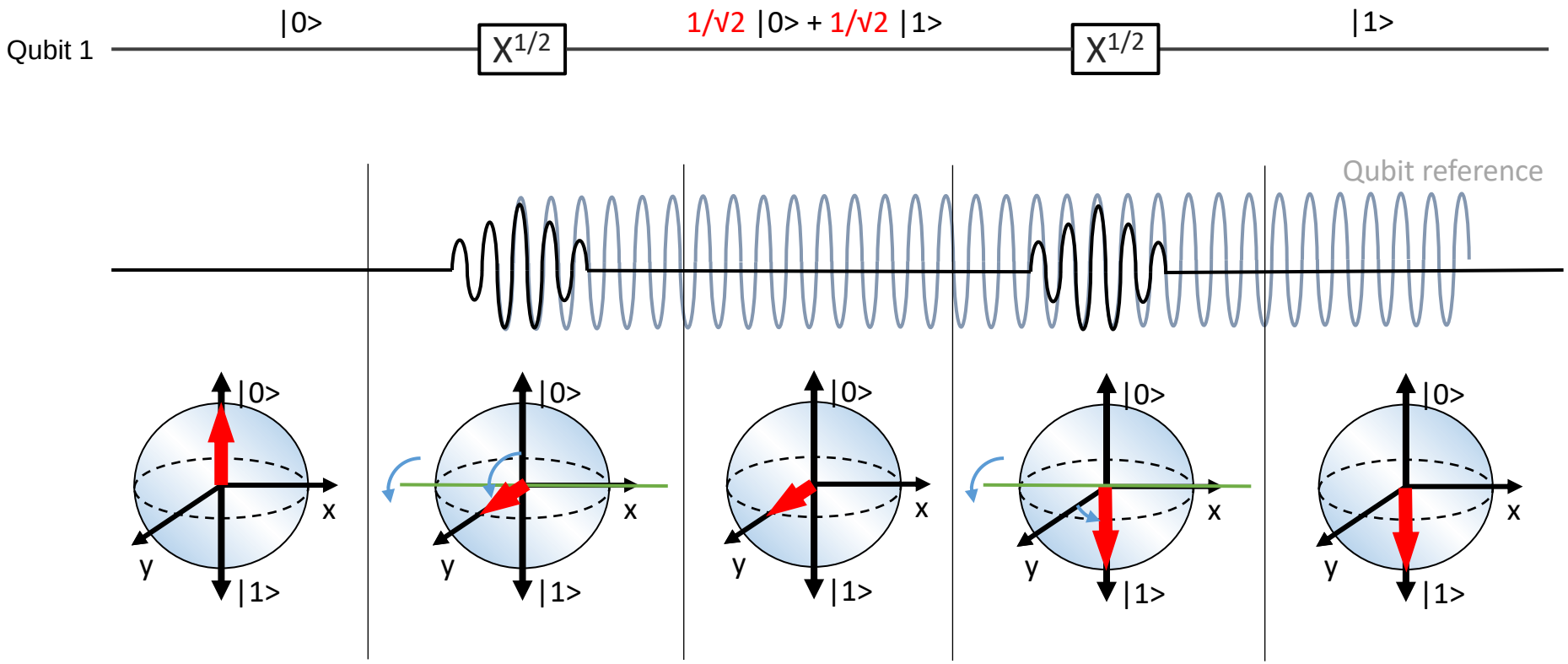
Controlling Qubits

INPUTS AND OUTPUTS



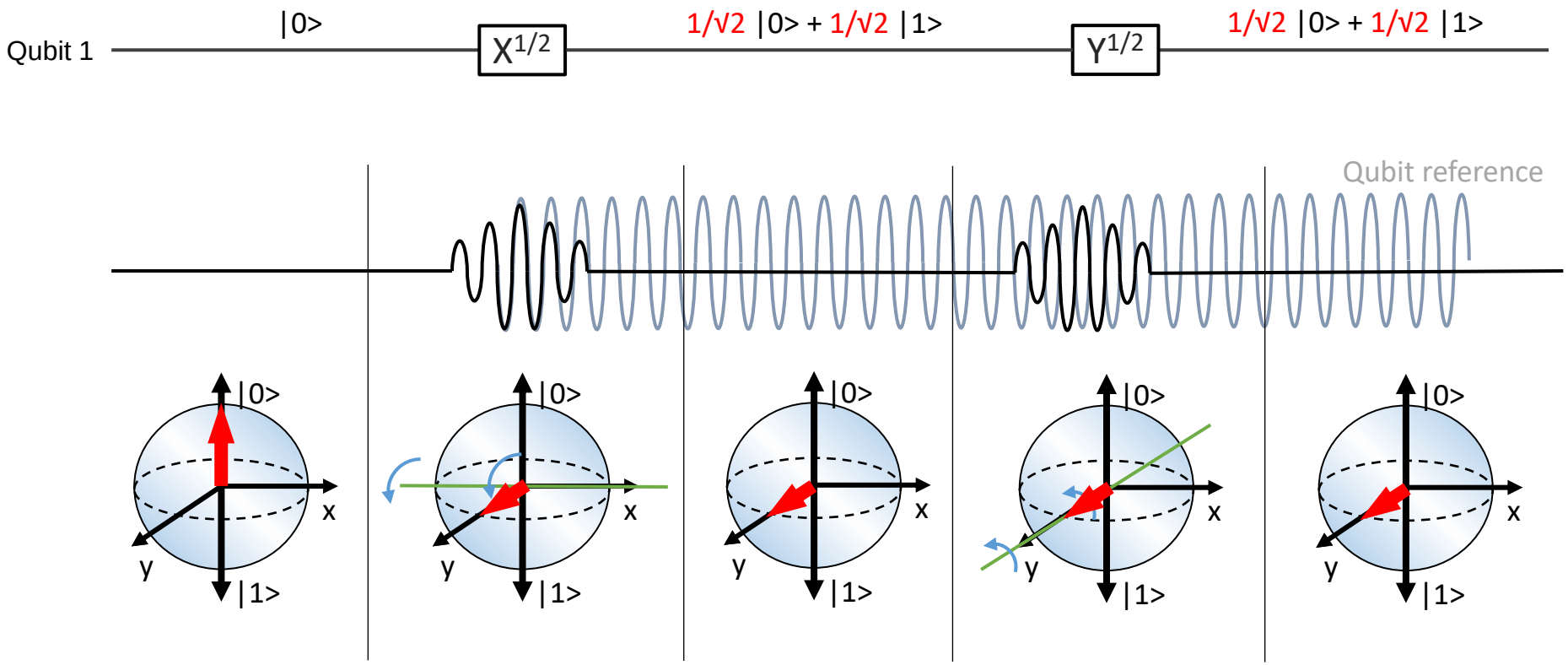
Controlling Qubits

QUBITS FRAME OF REFERENCE



Controlling Qubits

QUBITS FRAME OF REFERENCE



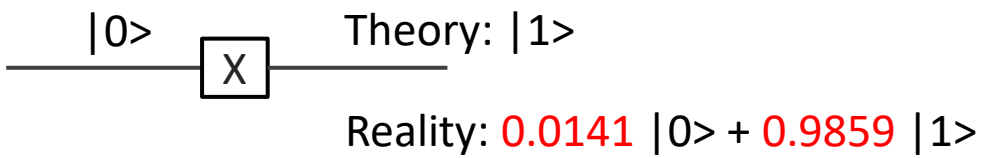
More about the importance of clock stability:
Ball, Harrison, William D. Oliver, and Michael J. Biercuk. "The role of master clock stability in quantum information processing." NPJ Quantum Information 2 (2016): 16033.

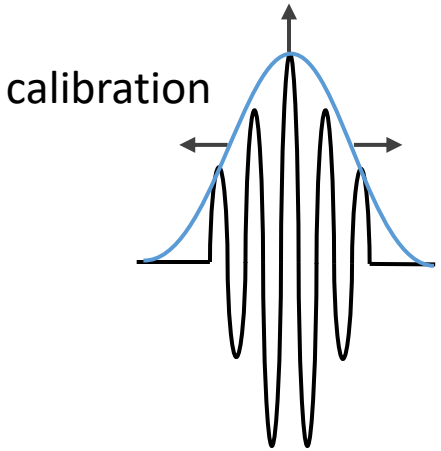
Phase noise is a critical requirement for high fidelity

Controlling Qubits

PULSE ENERGY

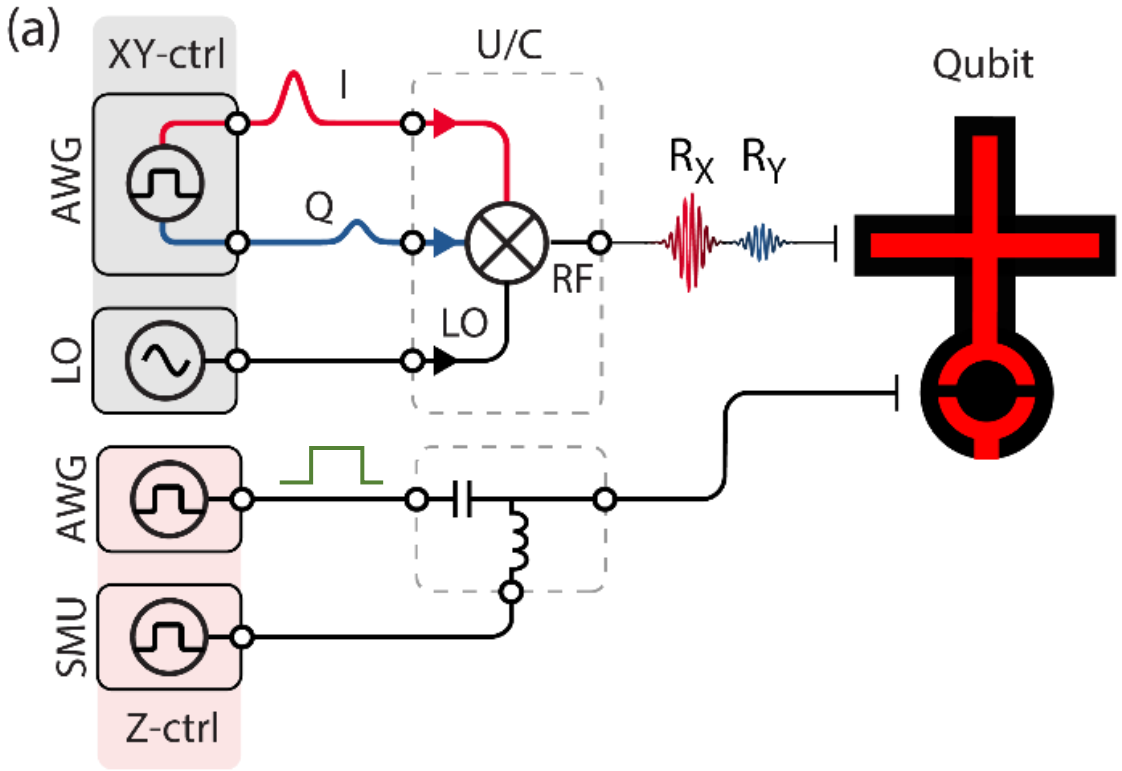
- Calibrating the envelope (area) of the pulse
  - Maximize gate fidelity
- For superconducting qubits, pulse envelope is chosen to limit the bandwidth and prevent driving unwanted transitions

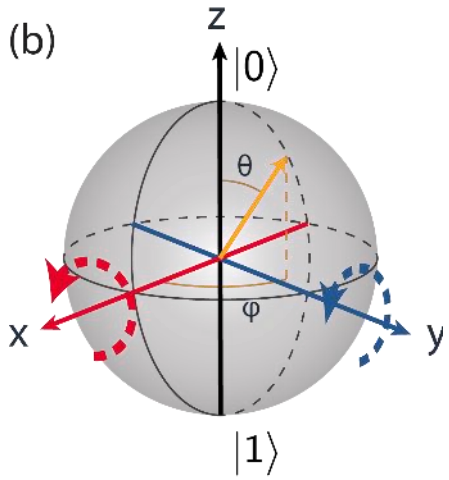




Controlling Qubits

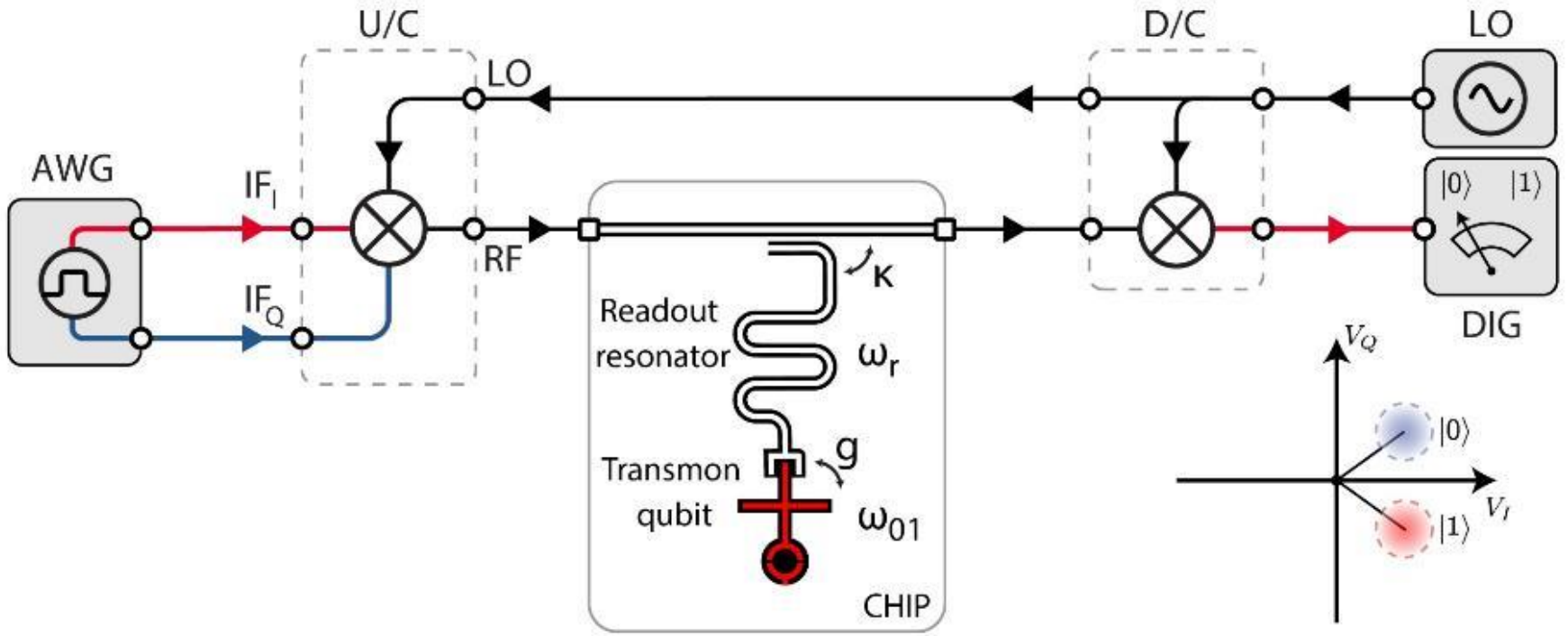
MICROWAVE AND BASEBAND CONTROL





Controlling Qubits

CIRCUIT QUANTUM ELECTRODYNAMICS

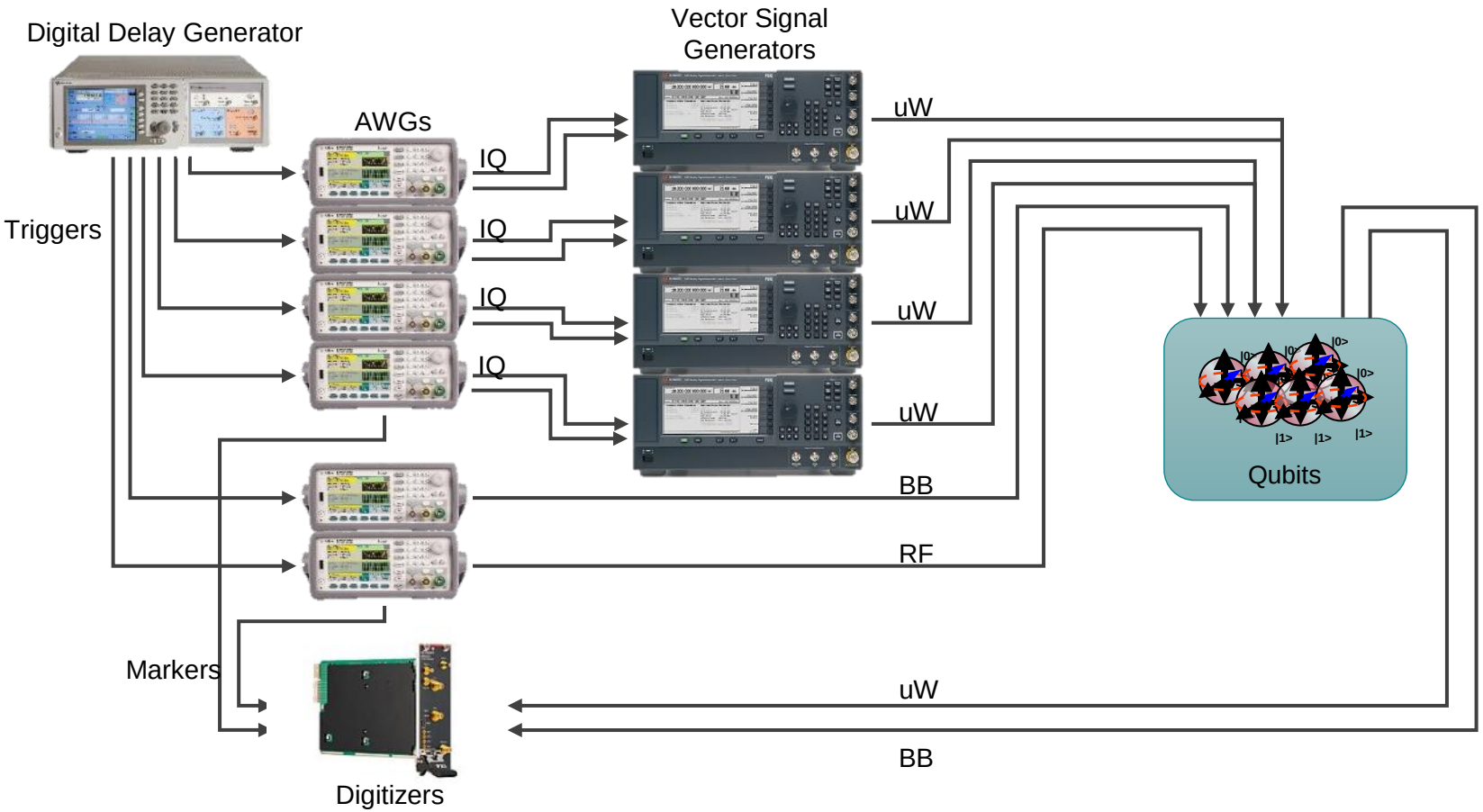


Control Challenges

Purpose	Requirements
High fidelity qubit control and readout	Tight channel-to-channel **synchronization**
Fast qubit initialization, QEC, and other feedback protocols	Dynamic-**Flow Control**
	Custom Real-Time (**RT**) **Processing** (FPGA DSP)
	Low **Feedback** latency

Synchronization

CLASSICAL CONTROL APPROACHES

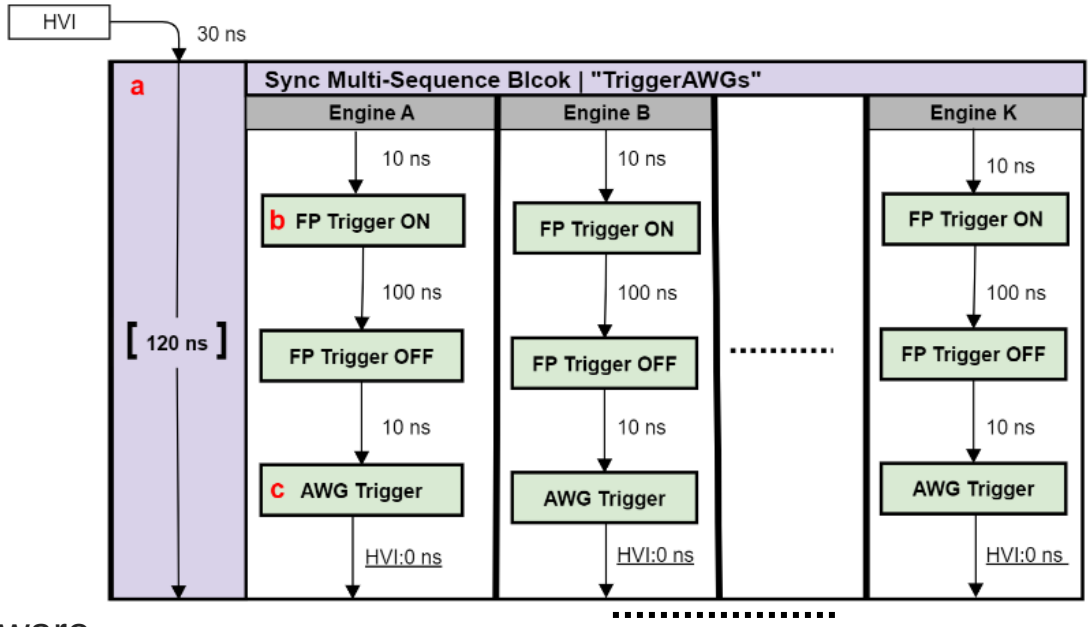


Control System Requirements
Tight channel-to-channel synchronization
Time-deterministic sequential control
Dynamic Flow Control

Dynamic flow control

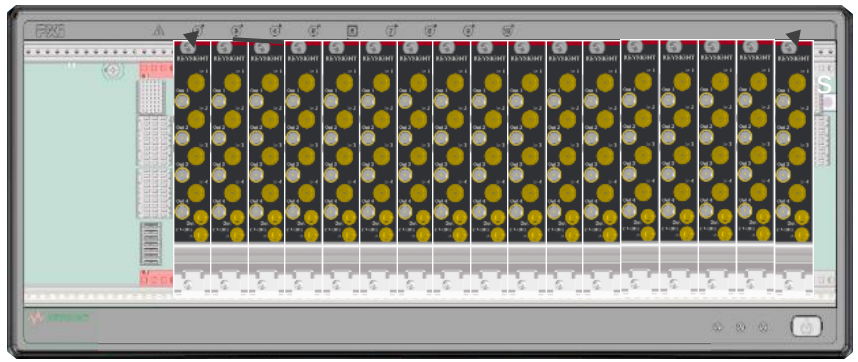
INTEGRATED RT SEQUENCING

Diagram



Hardware

Also with multiple chassis



Custom RT Processing

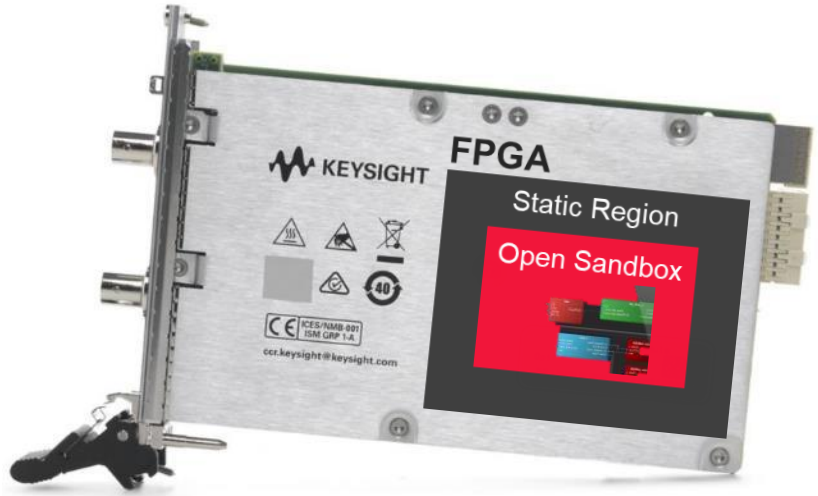
HW ACCELERATION

Custom HDL code

Ready-to-use IP Library

Quantum IP Library

PATHWAVE FPGA



- Streamlined Design Process
  - User-friendly graphical FPGA design environment
  - Remove built-in resources to free up FPGA space
  - One-click compiling and programming

AWGs and Digitizers

RF 2022 TECHNOLOGY EVENT
29 MAART 2022
QuTech/TU Delft

Feedback Operations

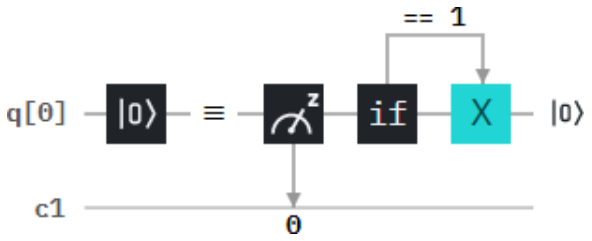
DYNAMIC SEQUENCING + RT PROCESSING

Many applications want to steer computation based on qubit measurement results

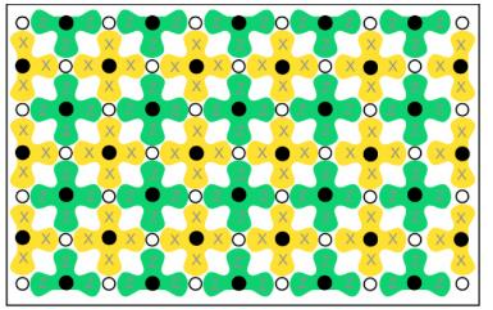
Requirements:

- ✓Accurate state preparation
- ✓High-fidelity qubit measurements
- ✓Fast processing of read-out signals
- ✓Dynamic sequencing

Fast Qubit Initialization



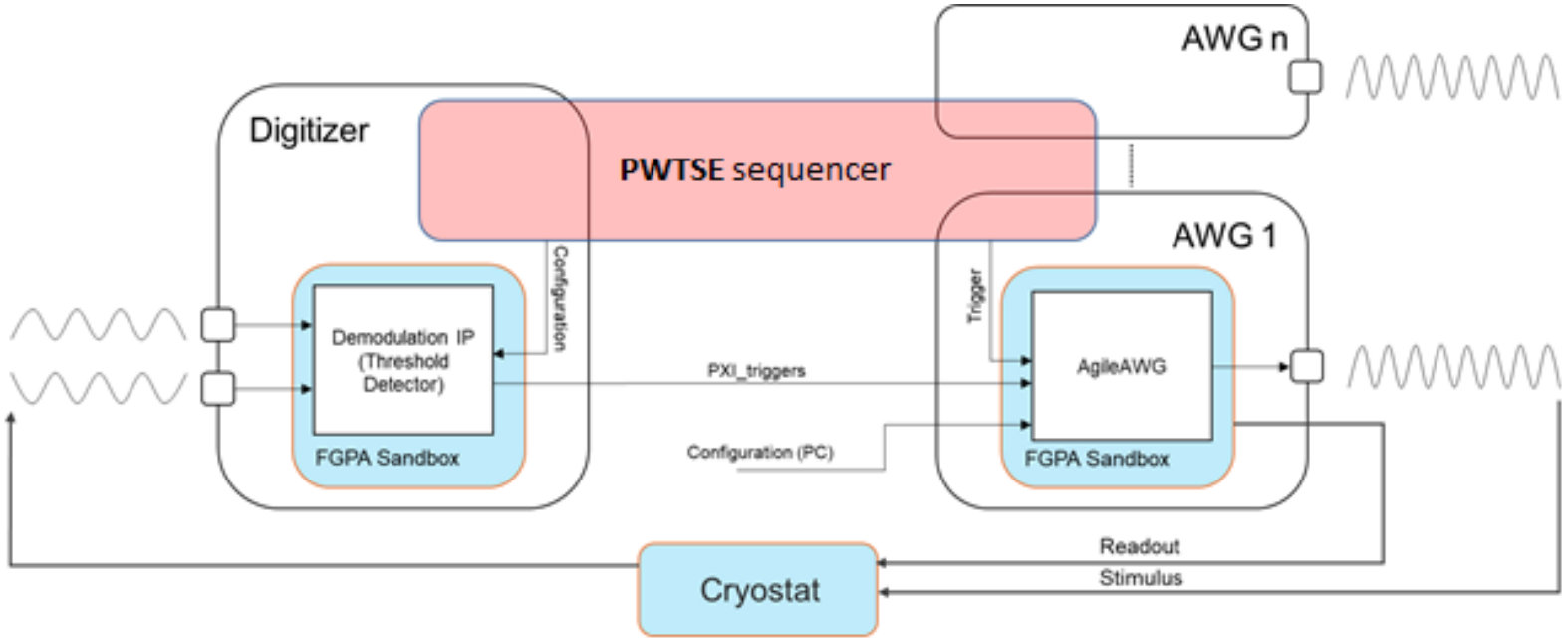
Quantum Error Correction



A. Fowler et al., "Surface codes: Towards practical large-scale quantum computation''

Low Feedback Operations

IMPLEMENTATIONS



- Feedback time << Coherence time
- Total Feedback time is <400 ns

Efficient Signal Generation

ENSURING PHASE COHERENCE

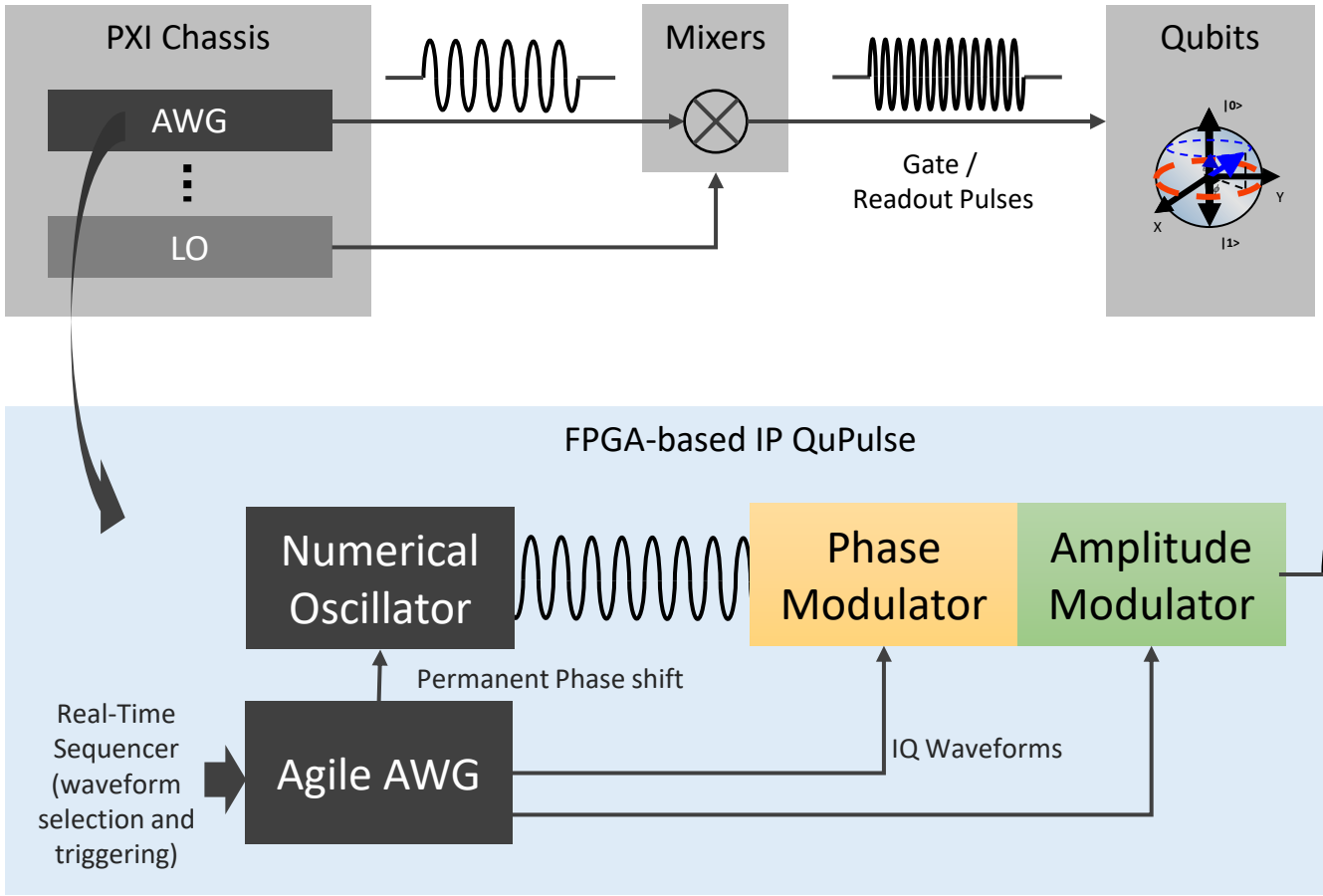
Several approaches to ensuring phase coherence:

1. Use phase of LO to keep track of qubit phase
   LO leakage becomes unwanted control signal

2. Generate at an IF
   a) Calculate the necessary waveforms ahead of time
      Requires lots of memory and data transfer
      No dynamic sequencing capabilities
   b) Use a numerical oscillator in the FPGA to track phase
      Can store complex gate primitives
      Easy parametrization of frequency, phase
      Simple Implementation of virtual Z gates

Efficient Pulses Generation

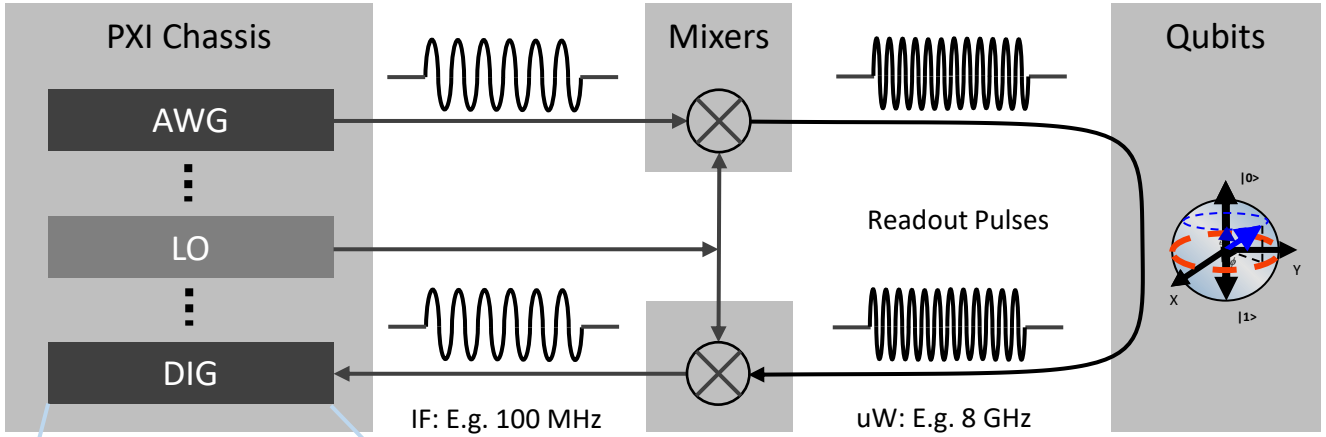
AGILE AWG



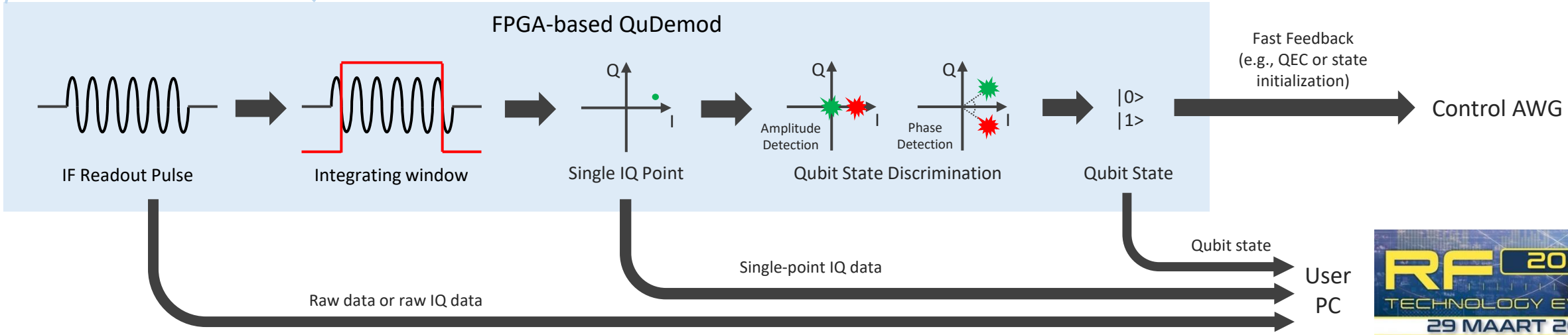
- Memory efficient by defining just gate primitives
- Triggering of individual gates performed by the RT sequencer
- Low-latency
- Phase Coherent
- Pre-scaler for "stretching" waveforms
- Ultra-light and scalable

Efficient RT Qubit Readout

CIRCUIT QED



- Phase-locked to the AWG,
- Customizable integrating window
- Streaming of raw data, raw IQ data, single-point IQ data, Qubit state
- Low-latency for feedback
- Light and scalable



Future Work

ROADMAP TO THOUSANDS OF QUBITS

- Scalable feedback architecture
  - Increasing FPGA speeds
  - Reducing data-converter processing times
  - Selective P2P data communication
- Improve scalability/density
  - Direct RF generation/acquisition
  - Increase number of modules that can be controlled
  - High resolution/ high speed AWG for flux bias and shuttling

Thank you!

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