TRENDS IN LEVENSDUURTESTEN VOOR MICRO-ELEKTRONICA

PLOT CONFERENTIE

JEROEN JALINK

8 JUNI 2016

MICROELECTRONICS RELIABILITY 54 (2014) 1988–1994

NXP

SECURE CONNECTIONS FOR A SMARTER WORLD

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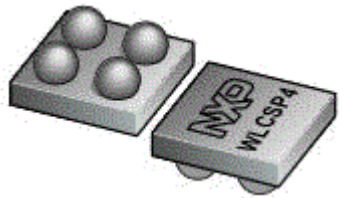
Introduction NXP



TODAY: 90% OF AUTO INNOVATION VIA ELECTRONICS
NXP IS #1

#1 INFOTAINMENT
- TUNERS
- SOFTWARE-DEFINED DIGITAL RADIO
- MULTIMEDIA PROCESSORS
- SOUND SYSTEM DSPs & AMPLIFIERS
- NFC BT PAIRING
- WIRELESS POWER CHARGING
- POWER MANAGEMENT

STANDARD PRODUCTS
- LOGIC
- POWER
- DISCRETES

#1 VEHICLE NETWORKING
- CAN/LIN/ FLEXRAY
- ETHERNET
- CENTRAL GATEWAY CONTROLLER
- SECURITY
- RF

ADAS & SECURITY

#1 BODY
- MICROCONTROLLERS
- POSITION/ ANGLE SENSORS
- SYSTEM BASIS CHIPS

POWERTRAIN & CHASSIS
- MICROCONTOLLERS
- PRESSURE/ MOTION SENSORS
- BATTERY MANAGEMENT
- DRIVERS

#1 SECURE CAR ACCESS
- IMMOBILIZER/ SECURITY
- REMOTE KEYLESS ENTRY
- PASSIVE KEYLESS ENTRY/ GO
- BI-DIRECTIONAL KEYS
- NFC
- ULTRA WIDE BAND

#1 SAFETY
- MICROCONTROLLERS AIRBAG
- ANALOG AIRBAG
- MICROCONTROLLERS BRAKING
- ANALOG BRAKING
- SENSORS BRAKING
- TIRE PRESSURE MONITORING

#1 Auto Analog/ RF | **#1 Auto MCU (ex JPN)** | **#1 Auto Merchant MEMS Sensors**

Smart Connected

Introduction NXP

>$10B IN ANNUAL REVENUE	**~45,000** EMPLOYEES	**35+** COUNTRIES
11,000+ ENGINEERS	**9,000+** PATENT FAMILIES	**4th Largest** SEMICONDUCTOR COMPANY GLOBALLY[1]

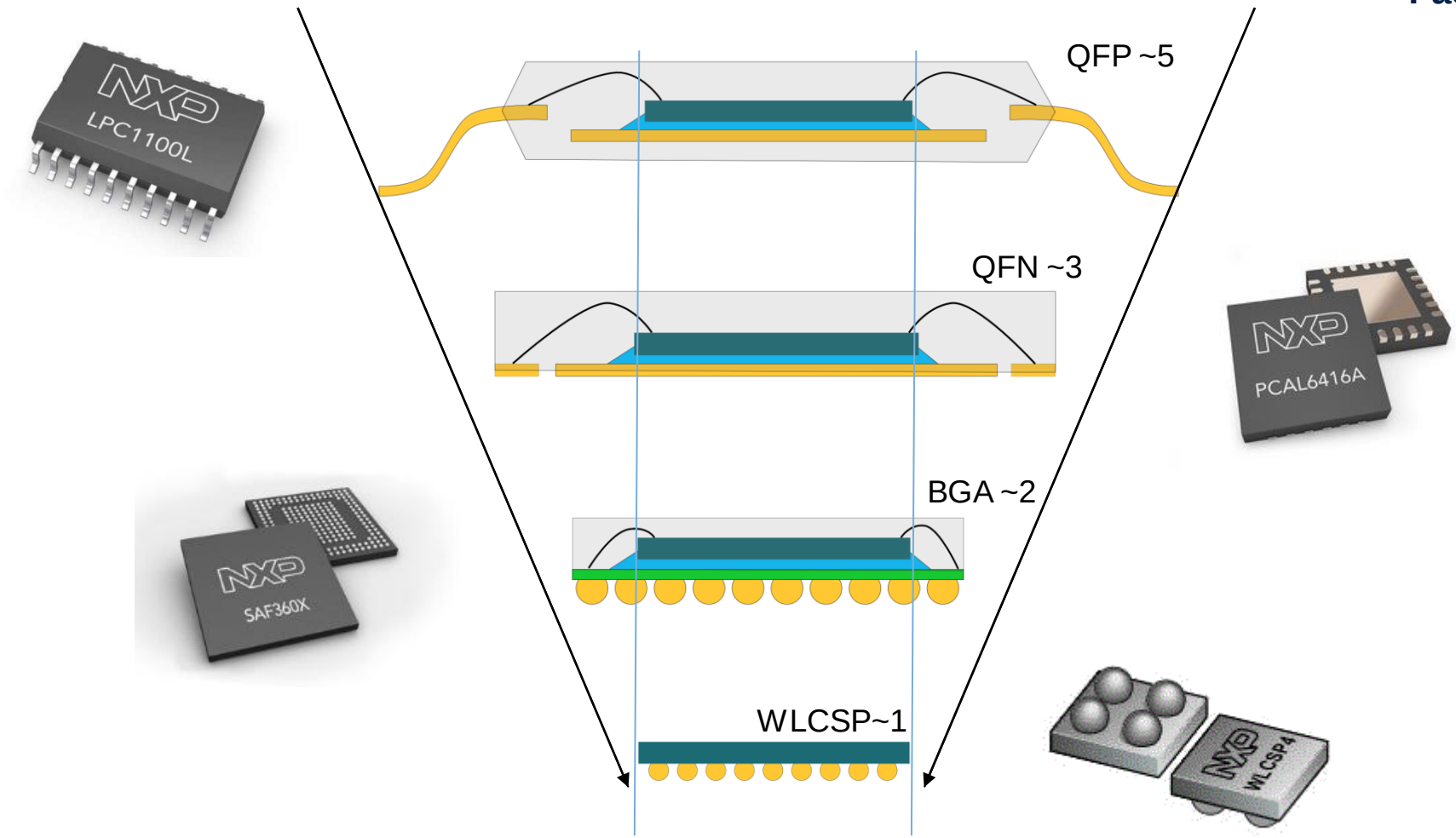
Product Diagnostics Center Nijmegen

- New Technology introduction
- New Product introduction
- Product qualification

Package Form Factor

Package form factor:

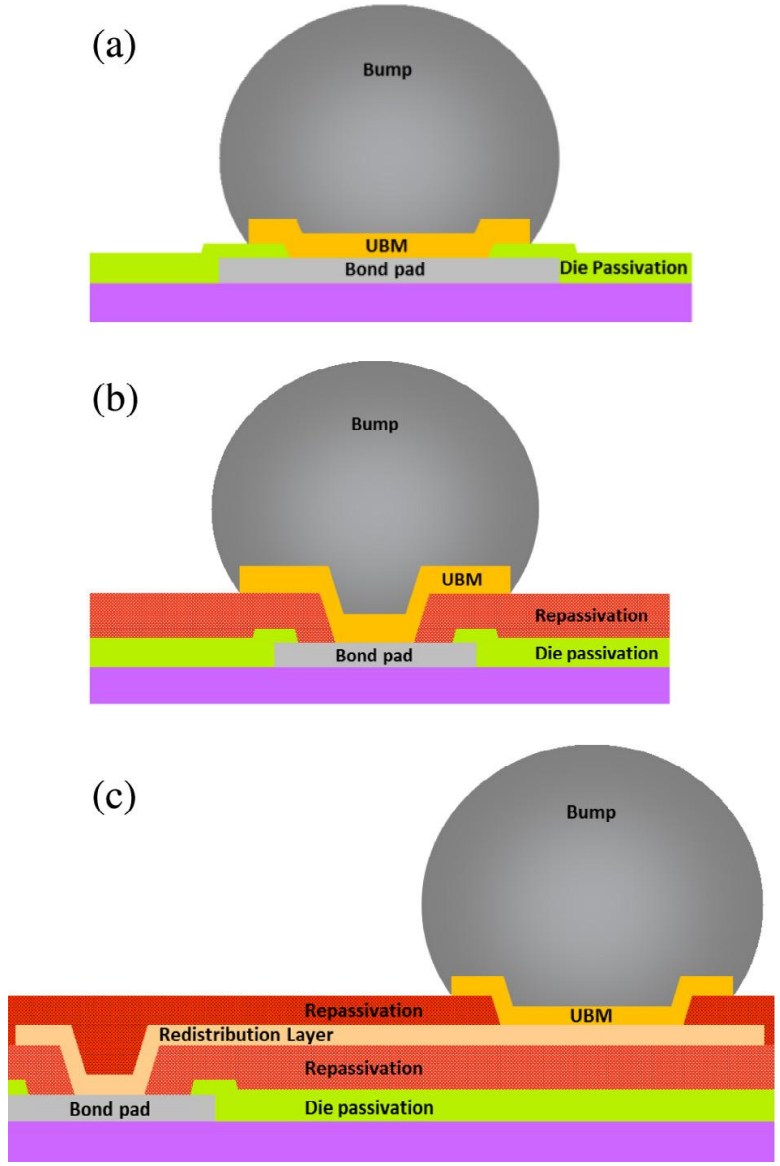
$$\frac{\text{Package area}}{\text{chip area}}$$



WLCSP bump construction

Predominant types of WLCSP bump constructions

- (A) Direct bumping
  - Under bump metallization (UBM) is directly on the chip's bond pad
- (B) Repassivation
  - A repassivation layer is applied before UBM and bump
  - Decoupling of chip and package
- (C) Redistribution
  - Allows for rerouting of electrical contact.
  - Allows to bump chips used in wire bond packages
  - Fan-in and Fan-out constructions



Failure mechanism driven qualification

- Technologies for semiconductor components are evolving rapidly:
  - Reduced dimensions (e.g., 22 nm wafer fab technology, CSP assembly)
  - More complex (e.g., 3D packages, Package on Package)
  - New devices (e.g., MEMS, CMOS sensors)
- Qualifying products by fulfilling a standard list of tests with prescribed conditions, duration and sample sizes without fails will not be appropriate anymore.
- A risk assessment on relevant failure modes (FMEA) is needed to construct a reliability risk mitigation plan.

Failure mechanism driven qualification

- The use conditions of a device in an application are typically characterized by a Mission Profile (MP)
- Typical elements in a mission profile are for example (but not limited to):
  - Expected field lifetime
  - Temperatures and duration typical for operating the device in the application
  - Environmental stress (thermo-mechanical loading, humidity)

Example of the Mission Profile (MP) for a tablet/smart phone.

Field life time: 5 years		
Operation mode	H/day	T_{device} (°C)
Power	8	85
Sleep	8	25
Idle	8	60
Cycle mode	Cls/day	ΔT (°C)
Power off ↔ on	1	75
Sleep ↔ idle	10	35
Idle ↔ power	3	25

(Thermo) Mechanical Failure Modes

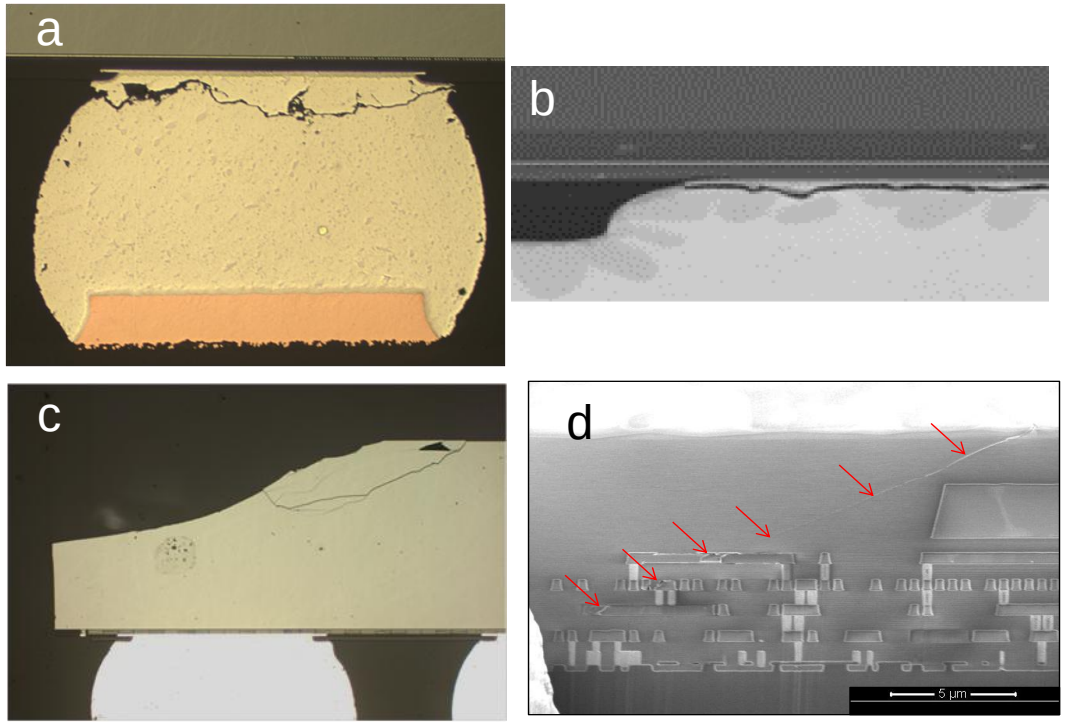
Four modes: symptom and occurrence

a) Fatigue crack, through the solder bump at the die/silicon side, observed after temperature cycling

b) Brittle fracture, through the solder bump at the die/silicon side, observed after (cyclic) drop or vibration events

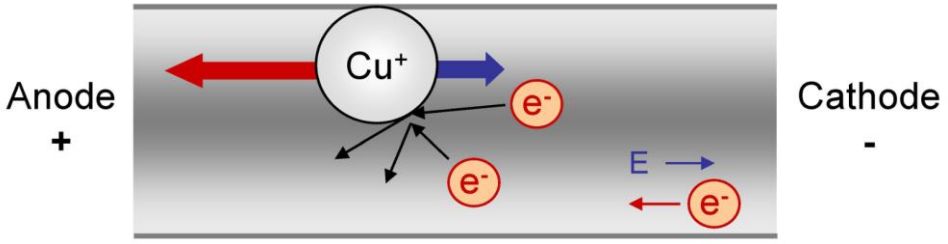
c) Chip out, observed directly, after manufacturing or as early field life fail

d) Brittle fracture in the passivation (top) layer, even extending into the BEoL, after temperature cycling



Current Driven Failure Modes

- Electromigration, in case a high current is running through the bump
- Void growing upstream the e-wind, as a result of extensive exposure to high temperature and current



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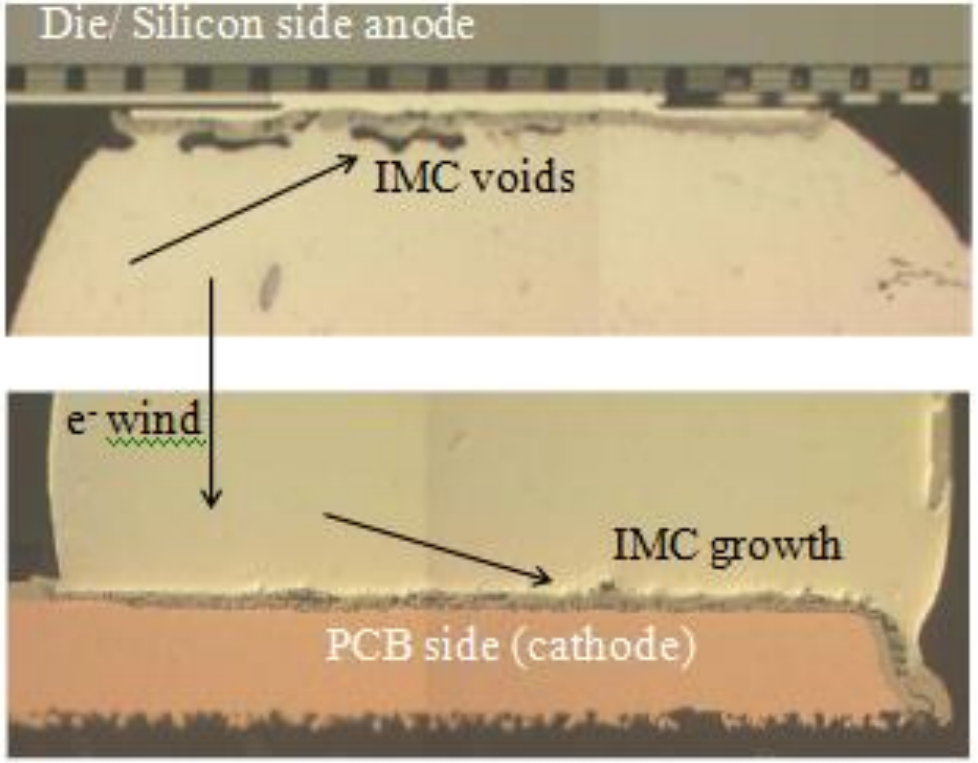
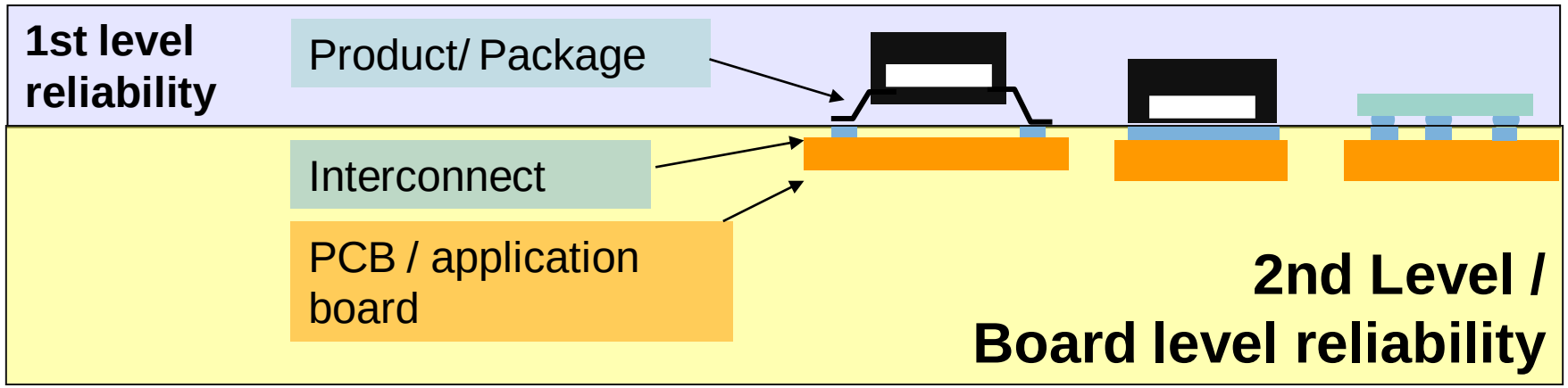


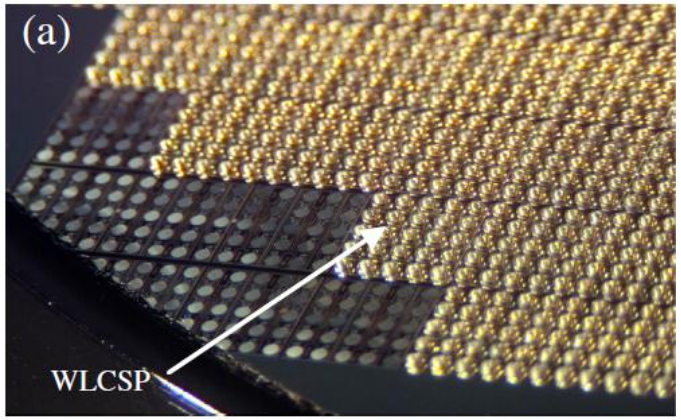
First and second level reliability

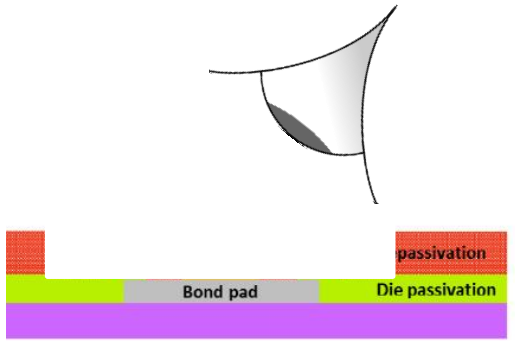
- First level reliability test are performed to cover failures mechanisms in the component itself (die, package or die-package interface),
  executed on the stand alone component
- Second level reliability focuses on the solder joint reliability, also known as board level reliability,
  executed on dedicated daisy chains mounted to PCBs



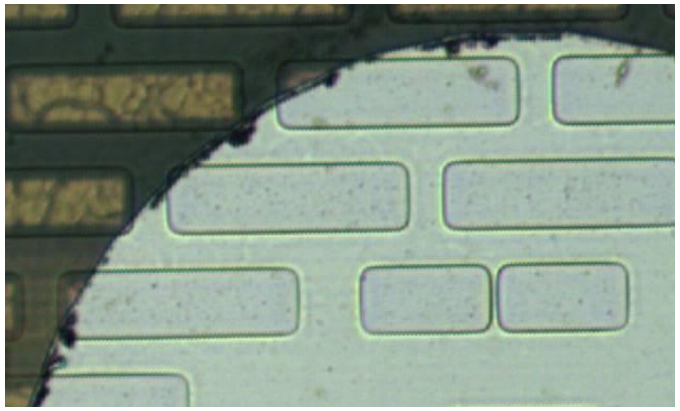
Case study: TC fails in WLCSP product

After 1st level TC on part of a wafer, Component Level (CL-TC):
No electrical failure and also no physical damage are observed

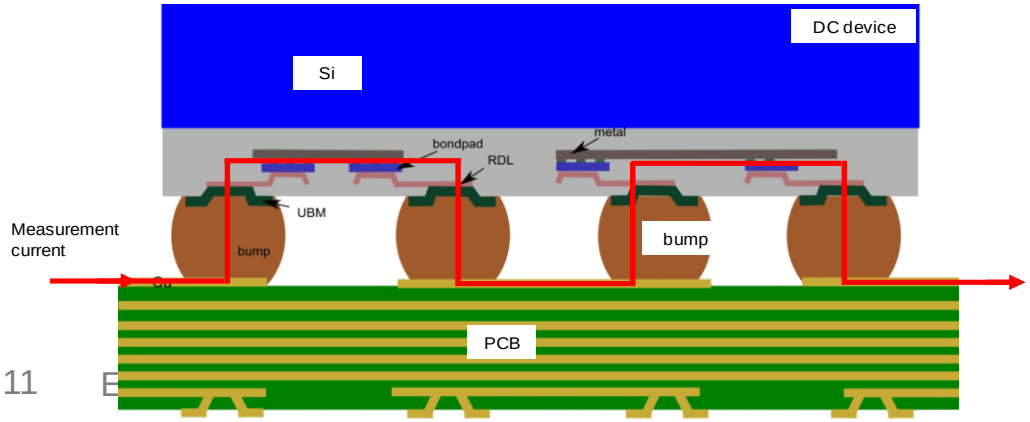


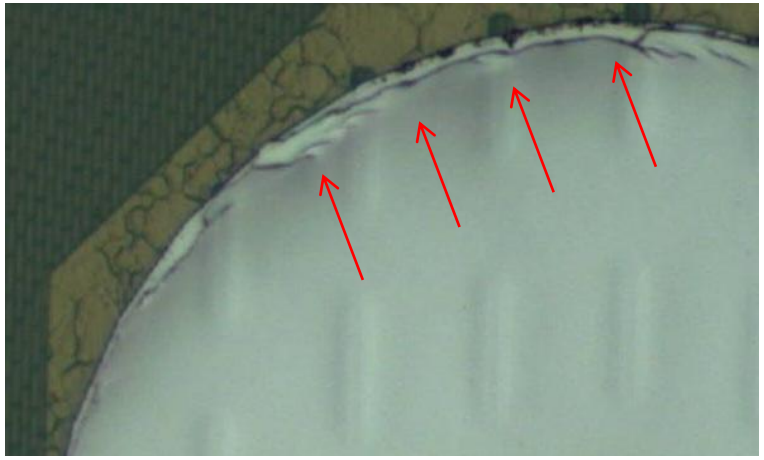


Visual inspection after bump removal:

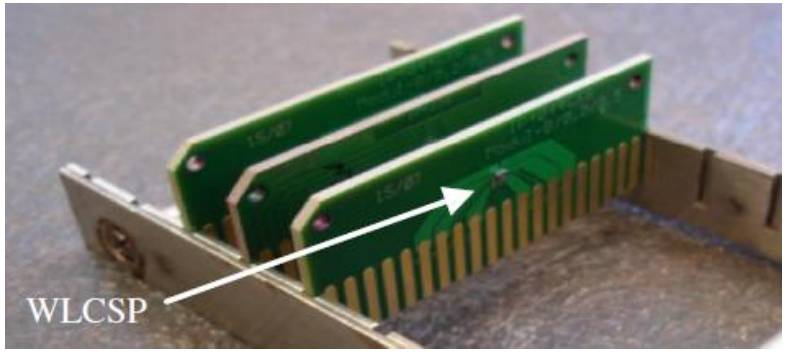


After 2nd level TC on daisy chains, Board Level (BL-TC):
No electrical failure but physical damage are observed



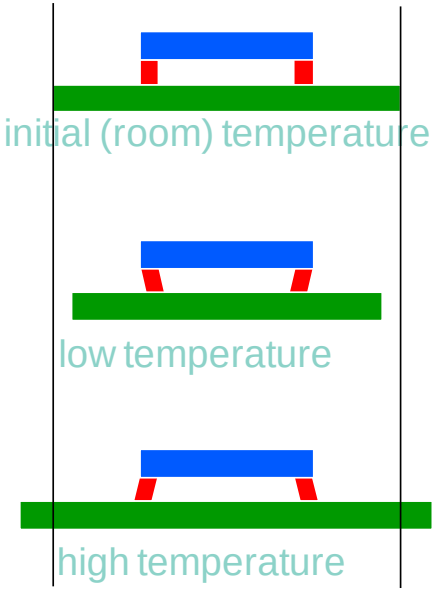


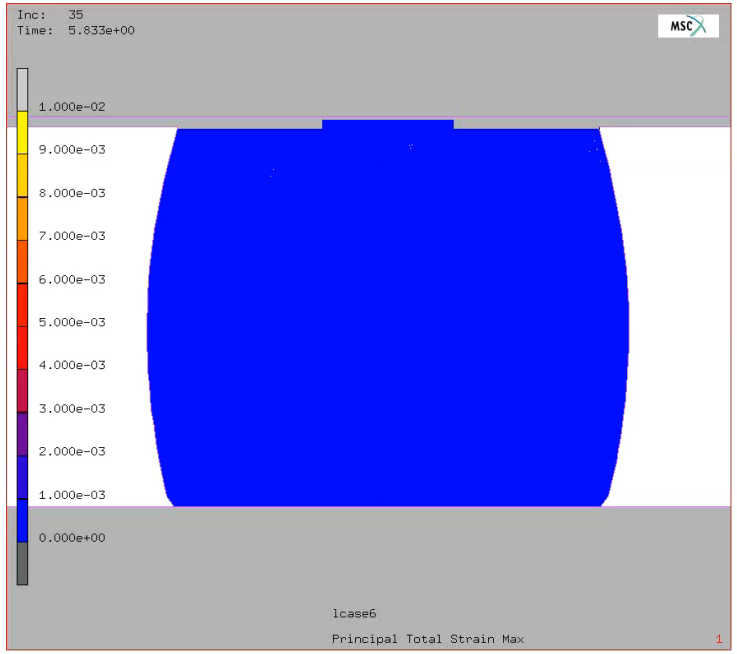
Case study: TC fails in WLCSP product

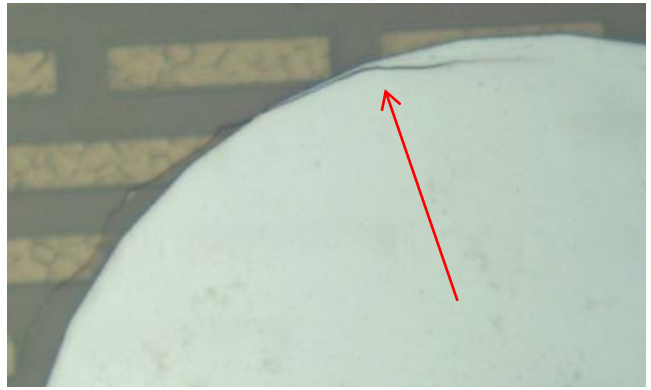


2nd level TC on actual devices, Application Level (AL-TC):

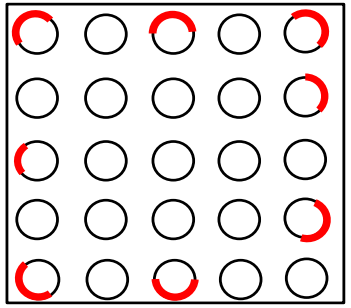
<u>Electrical rejects because of physical damage are observed</u>







Typical fail locations (confirmed by FEM):



Test to fail and life time prediction

- Model: modified Coffin Manson

$$N_f = C_0 \times (\Delta T - \Delta T_0)^{-q}$$

  - N_f: number of cycles to failure
    C_0: material dependant constant
    ΔT: entire cycle range
    ΔT_0: portion of the temperature range in the elastic region
    q: Coffin Manson exponent (failure mode dependent)

- Acceleration Factor (AF)

$$AF = \frac{N_{f,stress}}{N_{f,use}}$$

  - $N_{f,stress}$: number of cycles to failure under stress conditions
    $N_{f,use}$: number of cycles to failure under use conditions (taken from Mission Profile)

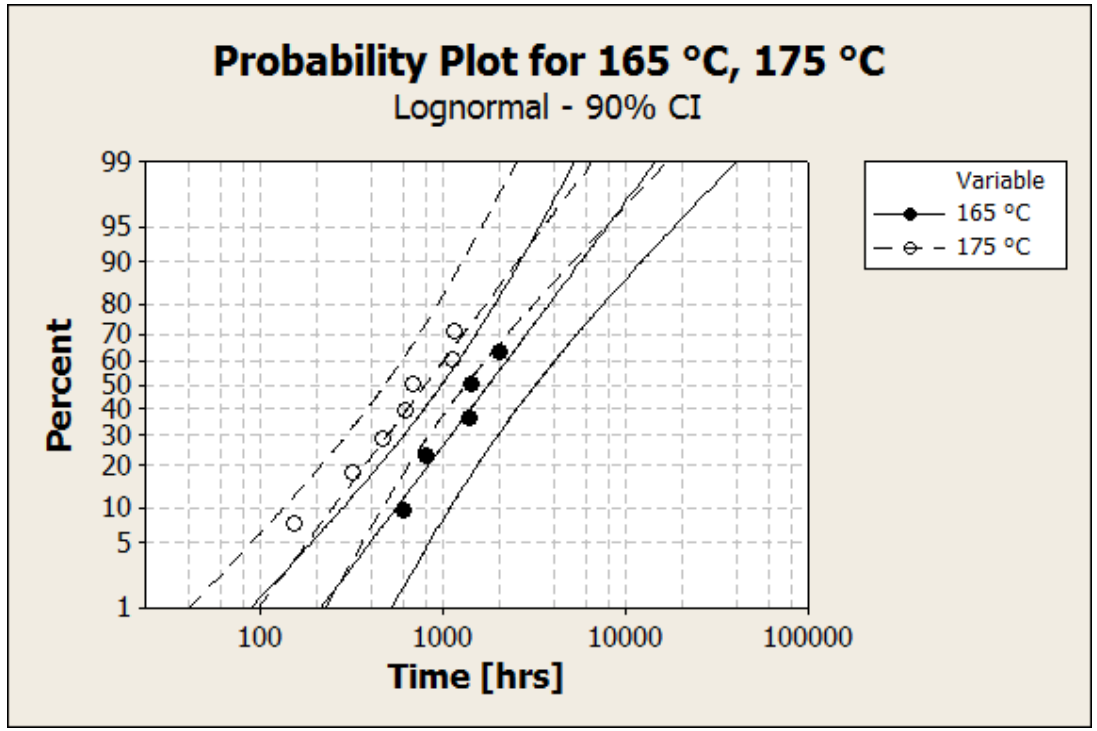
- Life time for a tablet or smart phone

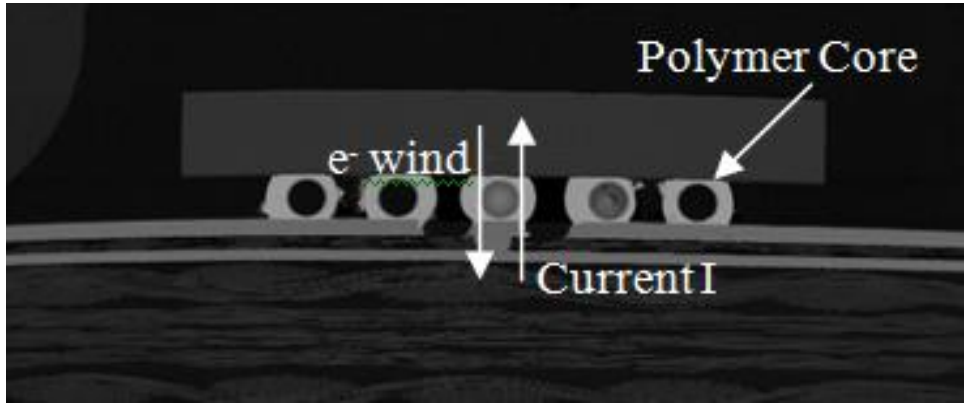
  - q = 6 (worst case value for a brittle fracture)
    $\Delta T - \Delta T_0$ = 185 (-40 to 125 °C)
    $N_{f,stress}$ = 100 cls (experimental result)

$$\text{Life time} = 28 \text{ yrs}$$

Case study: Solder Joint Electromigration

- WLCSP test-structure





$$TTF = J^{-n} \times \exp\left(\frac{E_a}{k} \cdot \frac{1}{T}\right)$$

TTF: Time To Failure
J: current density
k: Boltzmann Constant
T: temperature
"n" and "E_a": power exponent and activation energy (material specific)

Life time prediction

- Acceleration Factor (AF)
  - $t_{50,stress}$: time 50 % of the population fails under stress conditions
    $t_{50,use}$: time 50 % of the population fails under use conditions (taken from Mission Profile)

$$AF = \frac{t_{50,stress}}{t_{50,use}}$$

- Life time for a tablet or smart phone
  - E_a = 0.95 eV (from results on previous slide)
    Temperature under stress condition: 165 °C
    Temperature under use condition: 85 °C

$$AF = 290$$

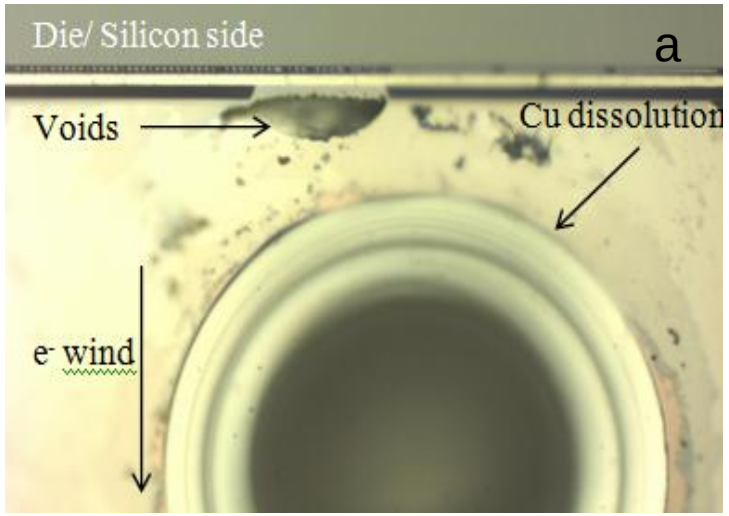
The expected lifetime for the application is **35 times** covered!

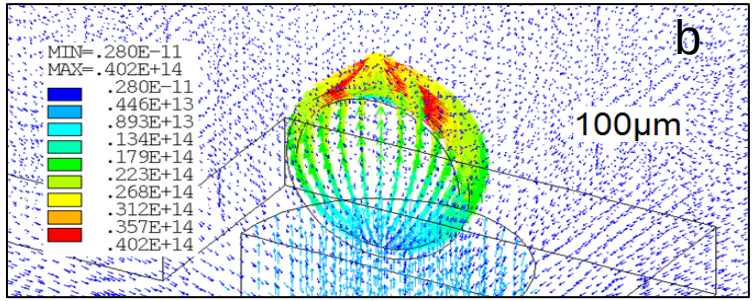
Understanding Preferred Failure Locations

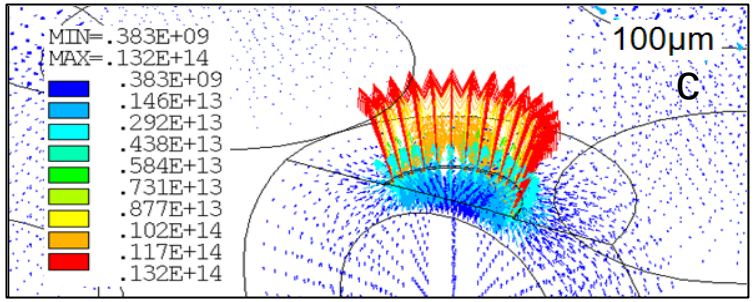
- Weakest spots from
  a) X-section after EM test

  b) FEM Mass flux distribution in the copper shell around the polymer core

  c) FEM Mass flux distribution in the SnAg solder material







Conclusions

- For WL-CSPs, direct interaction between the PCB and the silicon/die via the solder joint is much larger than for products in conventional lead frame or substrate based technologies
- New test methods, like AL-TC, and detailed assessment of failure modes and mechanisms via FEM, both help to understand the impact of stress/loading in applications
- Life time under application conditions can be predicted when acceleration models are determined together with the acceleration parameters

Acknowledgment

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- Other contributors: Jeroen Zaal for the modeling work, NXP Failure Analysis teams for the many X-sections and other sample preparations

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