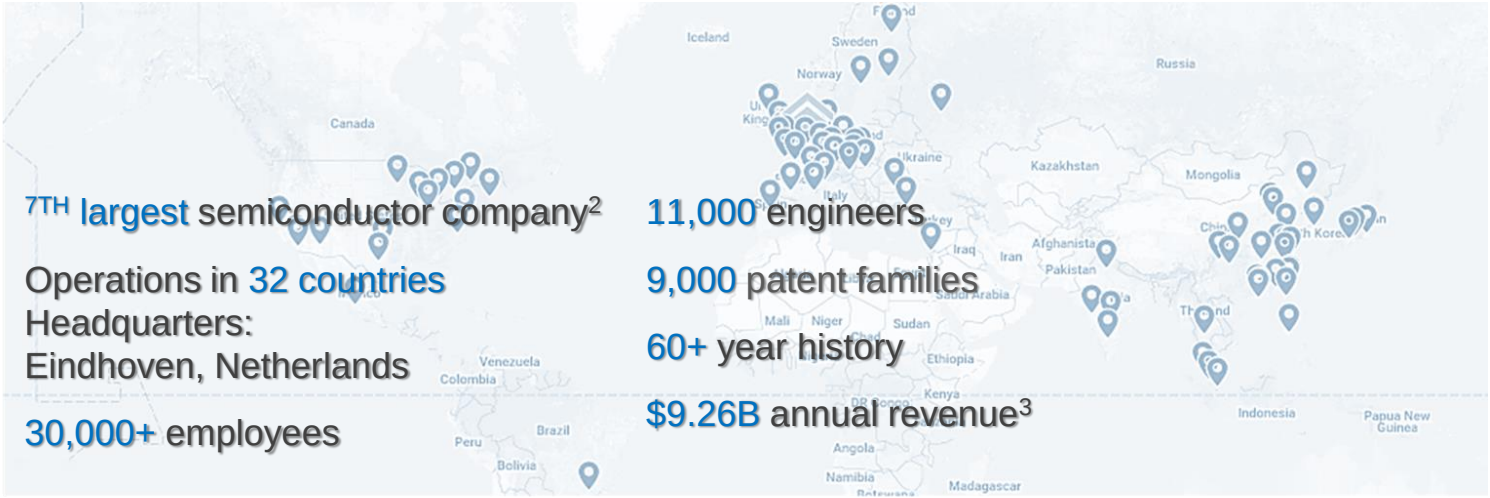
On the Evolution of Qualification Methods and Standards for Microelectronics in Automotive Applications beyond AEC-Qxx

NXP – René Rongen

29 NOVEMBER 2018
TECHNIEKHUYS
VELDHOVEN
PLOT CONFERENTIE
TOMORROW'S RELIABILITY

Company Introduction



7TH largest semiconductor company[2]

Operations in 32 countries
Headquarters:
Eindhoven, Netherlands

30,000+ employees

11,000 engineers

9,000 patent families

60+ year history

$9.26B annual revenue[3]

Corporate Office
Eindhoven, Netherlands

NXP Locations

#1 Automotive	#1 Broad-based MCUs[1]	#1 Secure Identification	#1 Communications Processors	#1 RF Power Transistors

Sources: HIS, ABI Research, Strategy Analytics, The Linley Group

1) MCU market excluding Automotive
2) Excludes memory
3) Posted revenue for 2017

Personal Introduction

- Fellow / Corporate Q&R
  - Joined NXP/ Philips as Reliability Engineer in 1997
- Internal Standardization
  - NXP Reliability Policy
  - NXP Cu-wire Way-of-Working
- External Standardization & Industry Consortia:
  Active participation in JEDEC, AEC, ZVEI
- Reliability “R&D”, Competence Building, Knowledge Sharing
  - NXP: Applied Reliability Training, Reliability Knowledge Framework
  - Conferences: IRPS, ECTC, ESREF, AEC-RW / (co)author, session chair, invited speaker
  - Dutch Accreditation Council: ISO17025 certification of reliability labs
- Problem Solving & Risk Assessments

Content

Content

Industry - Trend

- New technologies and application areas require in-depth knowledge on failure mechanisms and mission profiles
  - Sensor and Radar application, ADAS, Autonomous Driving
  - Automotive high temperature applications (beyond Q100 grade 0)
  - Applications with extended operational life time e.g., charging of electric cars

- Industry standards and consortia move towards knowledge based qualification
  - AEC Q100 and other AEC specs
  - JESD94/ JEP122
  - ZVEI Robustness Validation Handbooks

Automotive Electronics Council
Component Technical Committee

JEDEC
Global Standards for the Microelectronics Industry

ZVEI:
Die Elektroindustrie

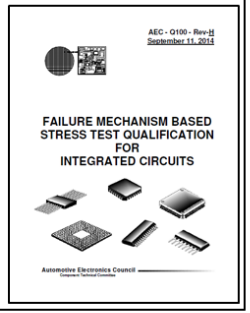
Reliability Evolution with Technology Progression

Generation 1

Stress Test Driven Qualification

- Predefined tests & conditions
- Predefined sample sizes
- Zero failures allowed

Focus on component
- Component Level Reliability



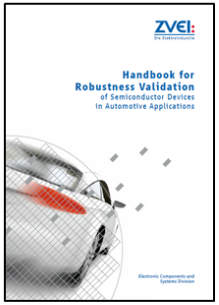
2005

Generation 2

Knowledge Driven Qualification

- Component mission profile
- Test until fail or proven margin
- Based on Physics of Fail
- Build in Reliability

New: Interaction with PCB
- Board & Application Level Reliability

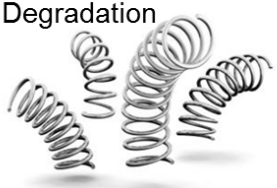


2020

Generation 3

Application Driven Qualification

- Application mission profile
- Based on Physics of Degradation
- Build in Resilience



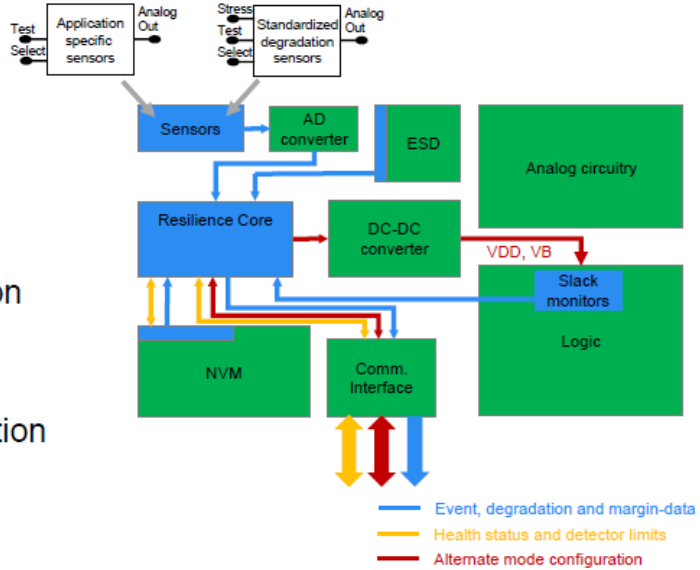
Focus on system
- Awareness of system health (sensors and detectors)
- Ability to compensate on changes (redundancy)
- Trigger user for repair or replacement before breakdown

Products and technologies for future complex applications (IoT, Autonomous Driving) will need all three methods in an optimal balance to meet all reliability requirements

Reliability engineering after RV

What is needed to implement a resilient system?

1. Sensors and detectors
   - ▶ Standardized IP
   - ▶ Application-specific sensors
   - ▶ Using an existing AD
2. Resilience core and communication interface
3. Ideally: integrated alternate operation modes



Goal is, that sensors, detectors and resilience core can re-use existing circuit blocks to minimize additional expenditure within the system!

BOSCH

Ref. “Resilience, Reliability Engineering after Robustness Validation”, F. Dietz/ Bosch, ECPE RV Workshop 2018

How to shorten qualification times

- Go extreme with test conditions :
  - Correlation with standard test condition
  - Reliability models
  - Unexpected and undesired failures

- Virtual qualification
  - Material characterization
  - Failure mechanisms models
  - Multi-discipline modelling

life.augmented

Ref. “Workshop Automotive Challenges”, C.M. Villa/ ST, ESREF 2018

Key Messages / Summary

Changes to come to the industry

- **New automotive grades / classes** will be defined in order to increase design freedom, but keep risk control
  - *T*-grades
  - *A*-grades – Application (performance vs reliability) grades
  - *L*-grades – Lifetime grades, ...
- **New automotive grades / classes** will on the other hand force designers to stay in associated design limits – which is not the case, today
- **Design for compatibility** is the answer to reliability & obsolescence management
  - This includes the usage of **standardized MPs**
- **Replacement electronics** approaches will come – security licenses will have update limitations
- **Function before car design** – cost efficient reliability assurance of electronics will achieve new ranks w.r.t. other car design aspects
- Joint **technology forecasting, monitoring & road mapping** along the supply chain is necessary and possible with proposed Platform

'Automotive' is in the phase to be defined and renewed

Ref. "New Automotive Semiconductor Categories and Classes for Standardized Mission Profile Enablement - a through the supply chain alignment activity", A. Aal/ VW, 1st European AEC-RW Workshop 2018

Reliability Evolution with Technology Progression

Generation 1 — 2005 — Generation 2 — 2020 — Generation 3

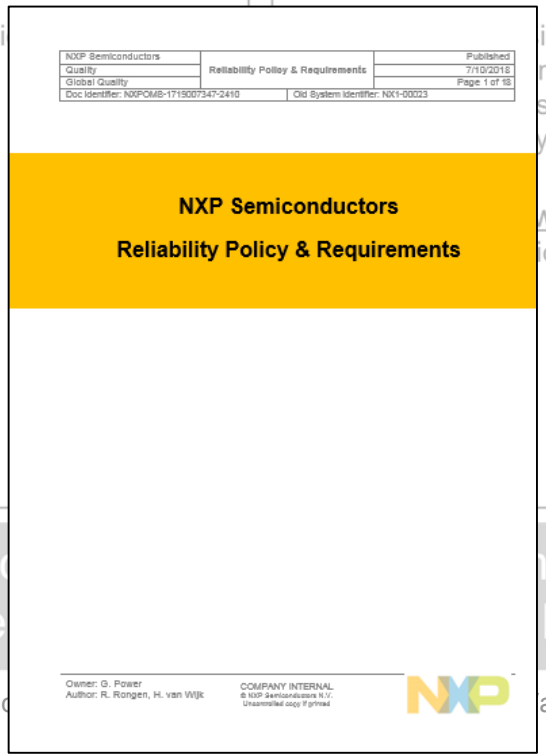
Stress Test Driven Qualification
- Predefined tests & conditi
- Predefined sample sizes
- Zero failures allowed

Focus on component
- Component Level Reliability

Knowledge Driven Qualification

Application Driven Qualification

Products and te … will need all thre … g)



The NXP Reliability Policy

1. Comply with industry standards
   "Generation 1"
2. Assess application mission vs technology capability (building in reliability, test-to-fail, extended testing)
   "Generation 2"
3. Prepare for "Generation 3"
   Reliability Engineering as integral part of Chip Design and Technology Development

Inspired by Ref. "Resilienc … alidation", F. Dietz/ Bosch, ECPE RV Workshop 2018

Content

Automotive Electronics Council - AEC

Component Technical Committee

Remembrance

Mr. Bob Vernon Knoell
February 5, 1957 - September 29, 2018

1. Founded 1993, by a.o. Bob Knoell (chair until Sept 2018)
2. Original membership of 15 companies
3. Now at
   - 18 Sustaining members
   - 46 Technical Committee member companies
   - 9 Associate member companies
4. ~ 35 spec/guidelines
5. Working Relationship with
   JEDEC, ESDA, JEITA, IEC, IPC

AEC: Standards under Revision or Preparation 2018

AEC std #	Current Rev	AEC standard title
Q100	H1	Failure Mechanism Based Stress Test Qualification of integrated Circuits (reference to Q006)
Q100-001	C	Wire Bond Shear Test
Q100-002	D	Human Body Model Electrostatic Discharge Test
~~Q100-003~~	~~E~~	~~Machine Model Electrostatic Discharge Test~~
Q100-004	C	IC Latch-Up Test
Q100-005	D	Non-Volatile Memory Program/Erase Endurance, Data Retention and Operating Life Test
~~Q100-006~~	~~D~~	~~Electrothermally-Induced Parasitic Gate leakage Test (GL)~~
Q100-007	B	Fault Simulation and Fault Grading
Q100-008	A	Early Life Failure Rate (ELFR)
Q100-009	B	Electrical Distributions Assessment
Q100-010	A	Solder Ball Shear Test
Q100-011	C	Charged Device Model (CDM) Electrostatic Discharge Test
Q100-012	0	Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems
Q101	E	Stress Test Qualification for Discrete Semiconductors
Q101-001	A	Human Body Model (HBM) Electrostatic Discharge (ESD) Test
~~Q101-002~~	~~A~~	~~Machine Model (MM) Electrostatic Discharge (ESD) Test~~
Q101-003	A	Wire Bond Shear Test
Q101-004	0	Miscellaneous Test Methods
Q101-005	0	Capacitive Discharge Model (CDM) Electrostatic Discharge (ESD) Test
Q101-006	0	Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems

AEC std #	Current Rev	AEC standard title
Q200	E	Stress Test Qualification for Passive Components
Q200-001	A	Flame Retardance
Q200-002	A	Human Body Model Electrostatic Discharge Test
Q200-003	A	Beam Load (Break Strength) Test
Q200-004	0	Measurement Methods for Resettable Fuses
Q200-005	0	Board Flex / Terminal Bond Strength Test
Q200-006	A	Terminal Strength Surface Mount / Shear Strength Test
Q200-007	0	Voltage Surge Test
Q001	D	Parts Average Testing
Q002	B	Statistical Yield Analysis
Q003	0	Guide for Characterization of Integrated Circuits
Q004	A	Zero Defects Guideline (unreleased)
Q005	B	Pb-Free Test Requirements
Q006	A	Copper Wire Qualification
Charter	A	AEC Charter
Q104	0	MCM/Module Qualification
		PC Board Qualification
Q103	0	MEMS / Sensors
Q102	0	LED
Q100 Rev. I	I	Bare Die/KGD
Q105	0	Touch Systems
		System Level ESD

Ref. “AEC 2018 Chair Report”, Bob Knoell, AEC-RW 2018 April 24-26

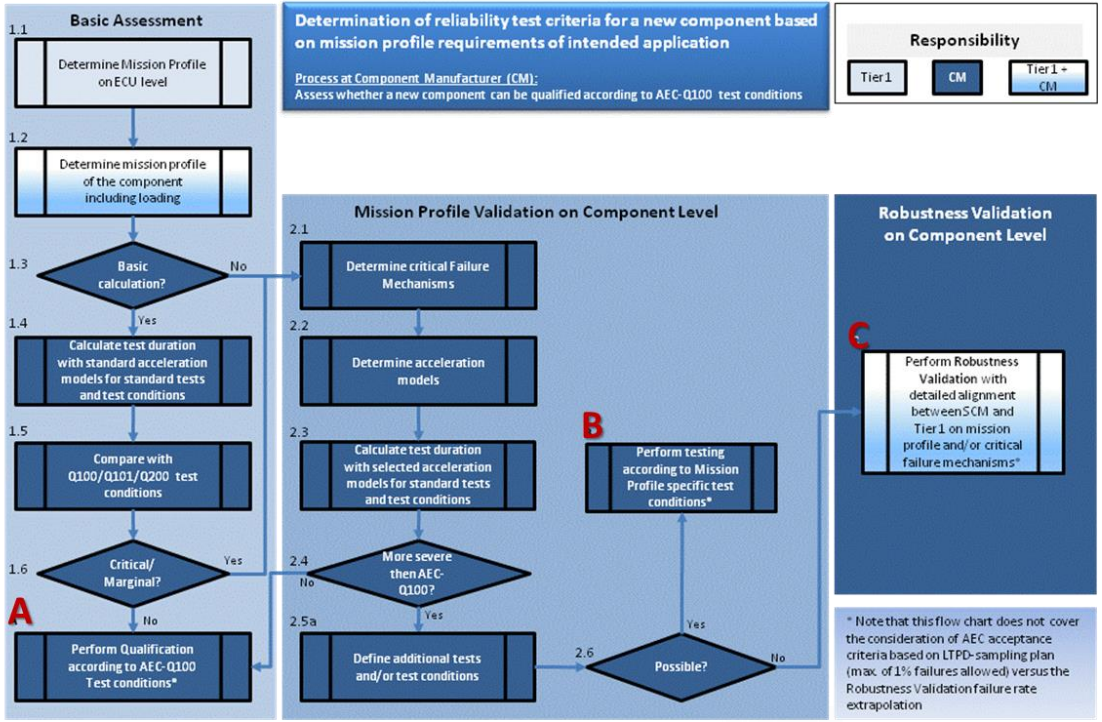
Content

Automotive Electronics Reliability: Challenge 1

- AEC-Q100 needs to provide clarity: *Extended test durations, AND Standardized Mission Profiles*

Tier1s and OEMs have to accept

“AEC-Q100/101 - Appendix 7”



Explanation to flow chart:

A AEC Q100 Standard Qualification

B Extended Qualification based on Customer Specific MP

C Modeling / test-to-fail based validation

Ref.:

1. AEC-Q100H - Appendix 7
2. “Robustness Validation – an Introductory Tutorial”. Werner Kanert/ Infineon & René Rongen, AEC-RW 2013
3. “Extended Lifetime Qualification based on Standard Mission Profiles”, Ulrich Abelein/ Infineon, AEC-RW 2018

NXP's "Generic" Mission Profiles; 4 for Automotive

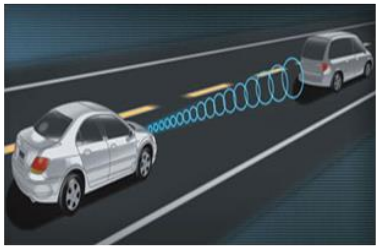
Portable:
Smart Phones

Commercial & Home & Industrial
Applications in the house and in the Industry:
Tablet, notebook & TV, DVD & Servers

Infrastructure:
Base stations

Ind RF:
RF Amplier

Automotive Grade 3
Entertainment in the cabin
Car radio / Seat DVD

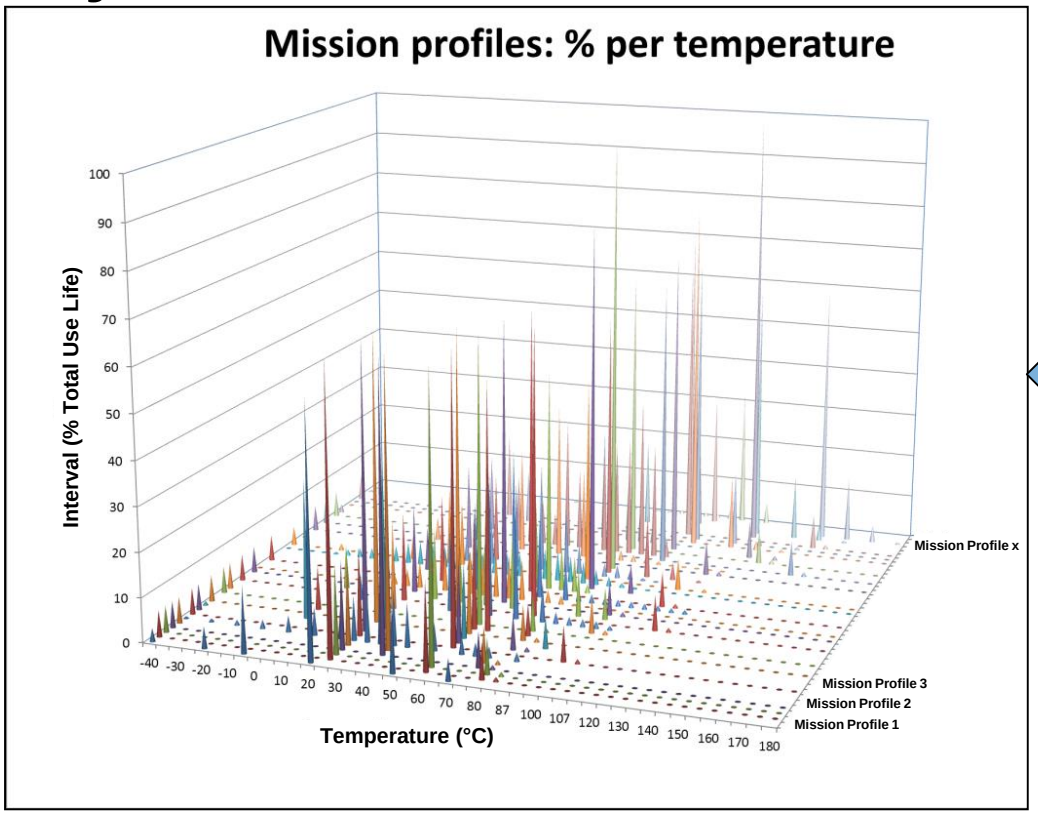


Automotive Grade 2
Car Radar

Automotive Grade 1 :
Under the hood

Automotive Grade 0 :
High Temp like sensors

Analysis of > 40 Automotive Mission Profiles …



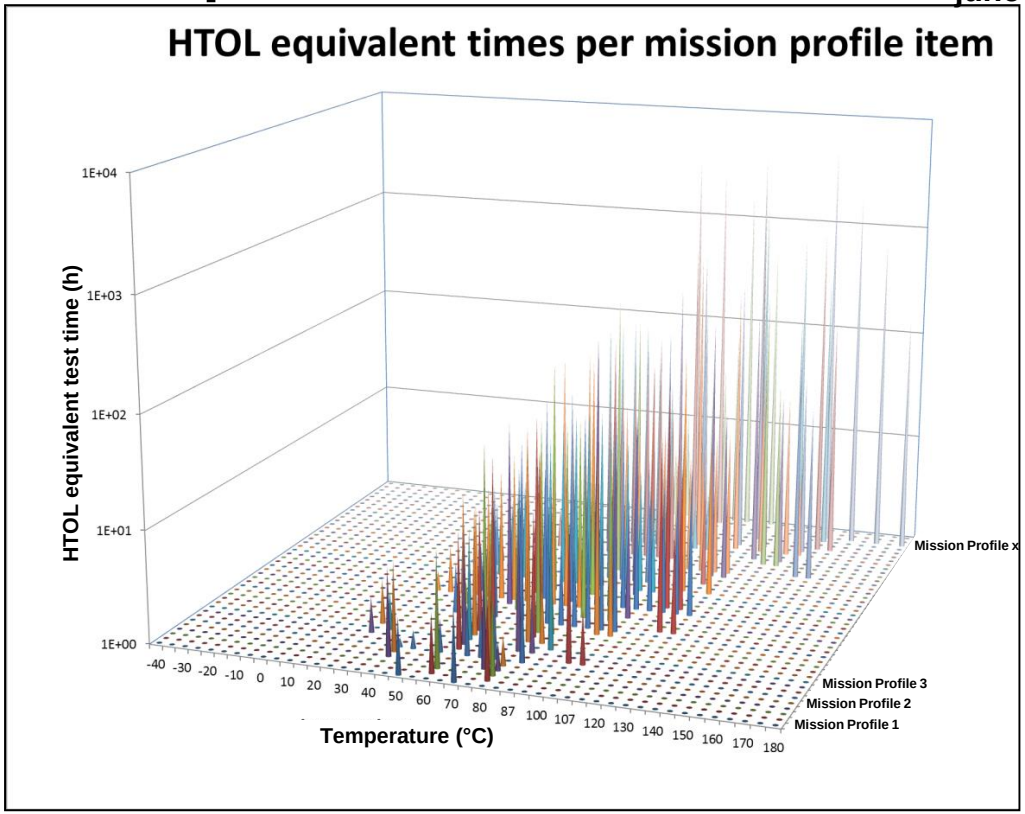
Note: Obviously there is more to cover than only 4 AEC-Q100 Grades...

Table 1: Part Operating Temperature Grades

Grade	Ambient Operating Temperature Range
0	-40°C to +150°C
1	-40°C to +125°C
2	-40°C to +105°C
3	-40°C to +85°C

Courtesy: Fred Kuper, Internal NXP Report 2014

HTOL Equivalent Test Duration (T_{junc} = 150°C / E_a = 0.7eV)



Accumulated durations span a couple of decades test durations

(Depending on the exact self dissipation in the applications)

Between 100 h and more than 10.000 h!

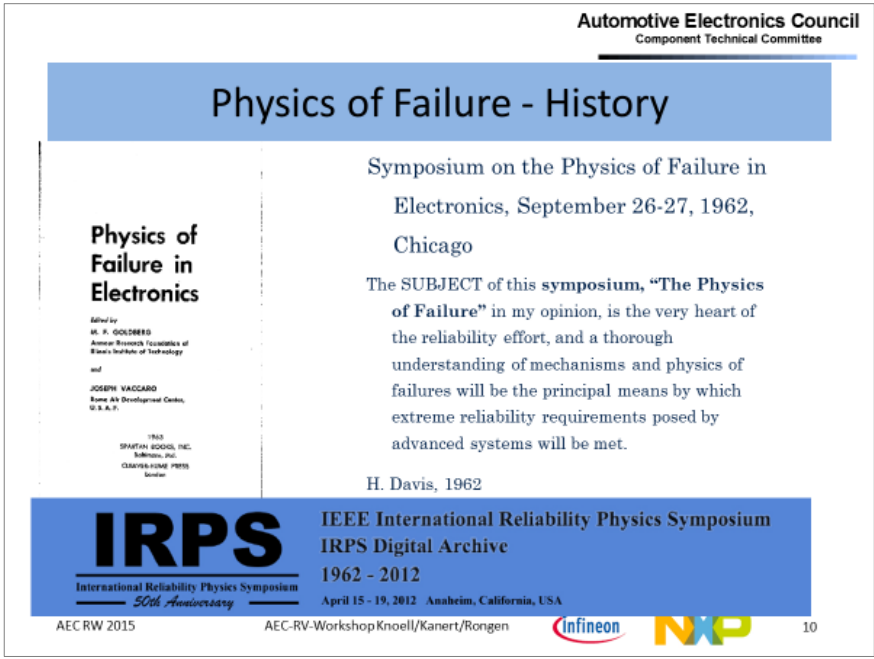
Courtesy: Fred Kuper, Internal NXP Report 2014

What is the Limit?

Or Failure vs Degradation or Change…

- Physics-of-Fail (PoF):
  - Principle is already as old as Semiconductor Industry
  - It is all about understanding processes and mechanisms causing degradation with eventual failure of materials and components

- Testing until fail can take a long time…
  - And if failures occur…
    Still the failure mechanism to be understood!



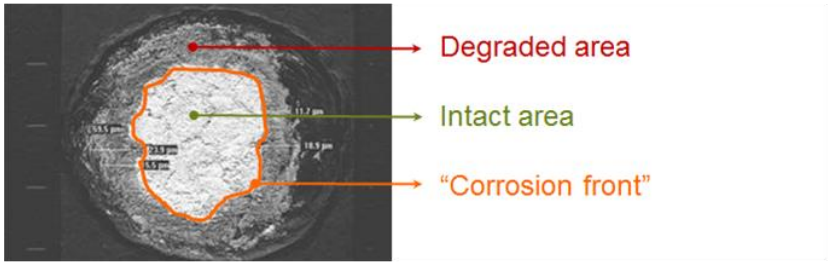
- Alternatively, the process of degradation after "time zero" can be recorded:
  - Physics-of Degradation (PoD) or even better Physics-of-Change (PoC)

Example of PoD: High T Corrosion for Cu-wire

Dynamics of Cu-Al Intermetallic Compound (IMC) Corrosion at high T:

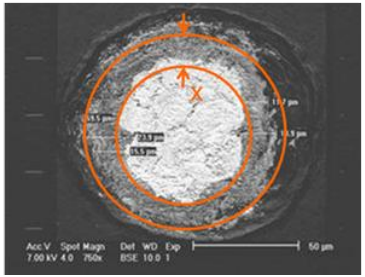
- IMC analysis method [1] : remove Cu-ball & mold compound in fuming nitric acid and analyze left intermetallic layer with back scatter SEM analysis

- Model of Degradation [2]:



$$x = \sqrt{D_0 \cdot \exp(-Ea/k_B T) \cdot t}$$

D_0 = Pre-exponential constant = 4.5 x 10^9 µm²/h
Ea = Activation Energy = 0.96 eV
k_B = Boltzmann constant = 8.617×10^{-5} (eV/K)
T = Temperature (K)



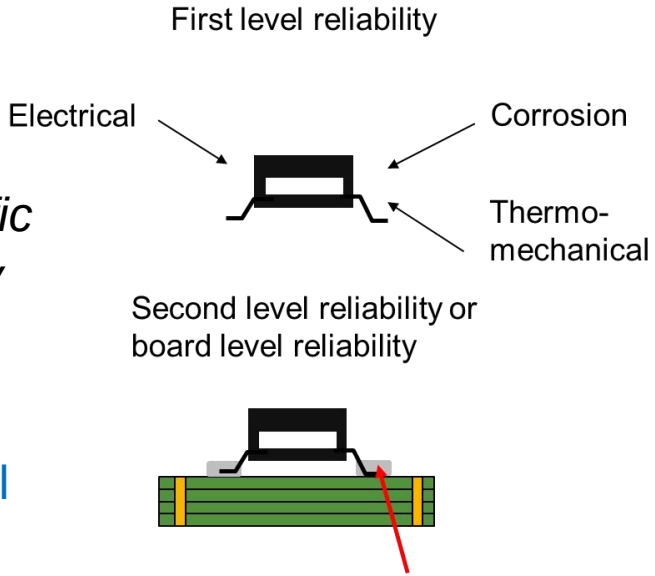
References:
1. G.M. O'Halloran, et al., "Planar Analysis of Copper-Aluminium Intermetallics", in Proc. International Symposium for testing and Failure Analysis (ISTFA), San Jose, CA, Nov 3-7 2013, pp.297-300
2. Lifetime prediction of Cu-Al wire bonded contacts for different mold compounds, R. Rongen et al., Electronic Components and Technology Conference, ECTC 64th, 2014, pp 411-418

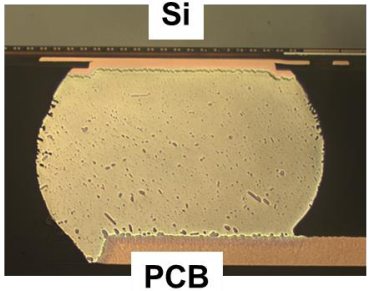
Model allows life time prediction of the contact WITHOUT reliability test

Content

Automotive Electronics Reliability: Challenge 2

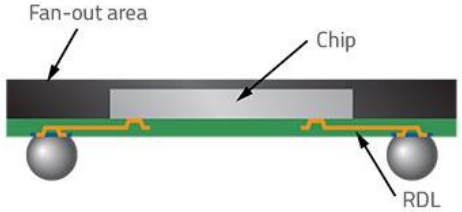
- AEC-Qxx:
  No standard test method nor requirements for Board Level/ Solder Joint Reliability
  Currently: only user (Tier1) specific methods and requirements – very inefficient…
- In addition:
  The "interaction" between 1st level (component level) and 2nd level (board level) reliability
  Currently: only guidelines in JEP150





Wafer Level Packages:
Is it 1st or 2nd level ?

Bumped Dies: New Approach
(Flip Chip, Fan-out WLP and WL CSP)

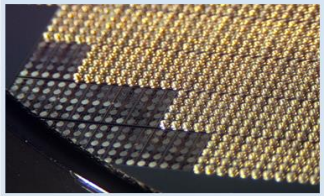
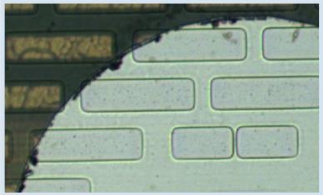
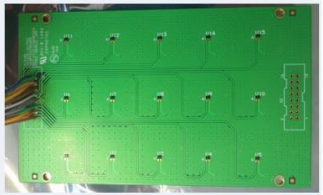
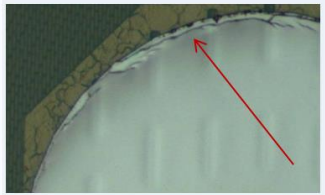
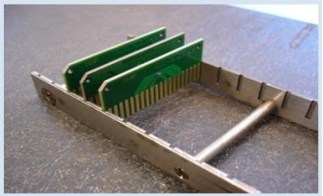
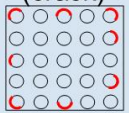
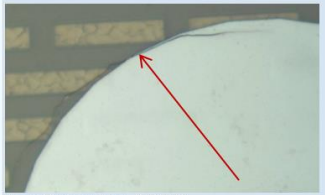


- Two key differences compared to conventional plastic packages
  - Failure modes accelerated by TC are different: dominant are cracks in the BEoL
    These can only be accelerated in the presence of a solder connection *(see next slide)*
  - Handling WLCSP may results in (many) non-stress related fails
    Mounting on a carrier is effectively preventing damage due to handling

- In principle JEP150 does apply in this case (assembled solid state devices); the problem is that JEP150 is not giving any requirements
  - NXP defined test method & requirements internally
  - Guidelines (no requirements) added to latest JESD47 revision K (IC Qualification Standard for Commercial & Industrial Application)
  - Major OEM for mobile applications adjusted its IC Qualification Standard accordingly
  - Will AEC-Qxx be next?

Flip Chip, Fan-out WLP and WL CSP

Thermomechanical Failure Modes in BEoL

TC Type	Test vehicle		Electrical signature	Physical signature	
Component Level (**CL-TC**)	Singulated functional devices or part of a wafer		No failure	No damage (crack)	
Board Level (**BL-TC**)	Daisy chains on a PCB carrier		No failure	Damage (crack)	
Application Level (**AL-TC**)	Functional devices on a PCB carrier		Failure	Damage (crack) 	

Typical fail locations (confirmed by FEM)

Ref.: Reliability of Wafer Level Chip Scale Packages, R. Rongen, R. Roucou, P.J. vd Wel, F. Voogt, F. Swartjes, K. Weide-Zaage, Microelectronics Reliability, 2014, Volume 54, pages 1988-1994

Flip Chip, Fan-out WLP and WL CSP

Example BEoL Stress Modeling for WL CSP

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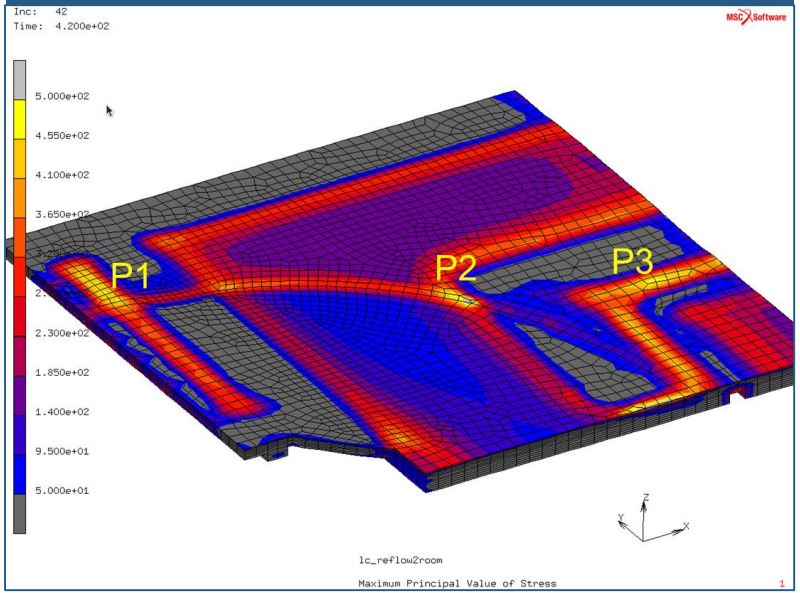
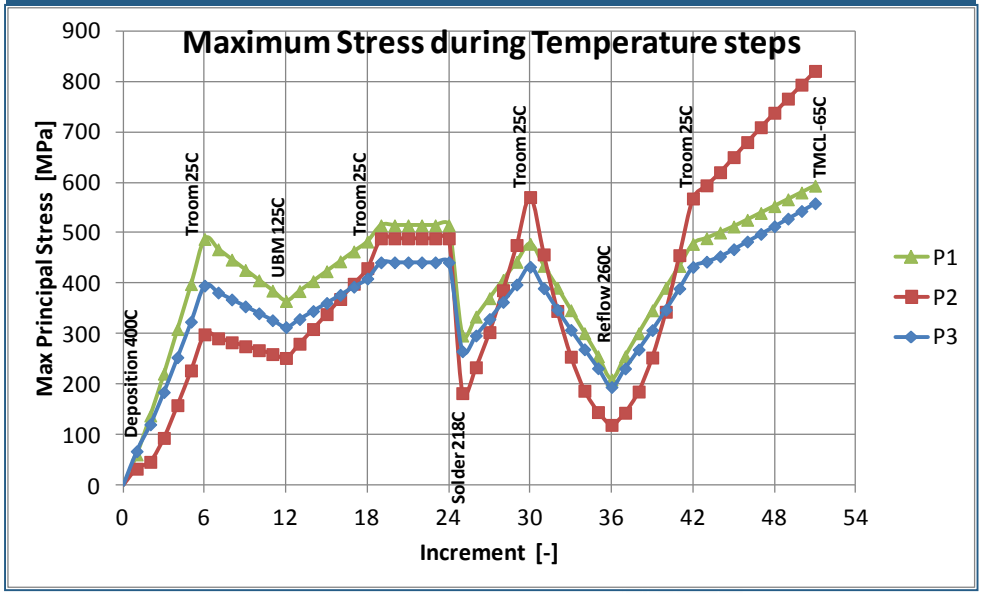
P1, P2 and P3: relevant metal structures in the corner of the die



Modeling of principal stress development over time: bumping – PCB soldering – AL-TC



Modeling allows for setting up design rules

Flip Chip, Fan-out WLP and WL CSP

Background NXP AL TC Requirements

Taking 1000 c from -40 to 85 °C as reference and using Coffin-Manson (CM) equation with exponent 6 for the other conditions:

Low T (°C)	High T (°C)	Reference (c)	Calculated (c)*
-40	85	**1000**	1000
-40	125		*189*

*Coffin-Manson equation:

$$AF = \left(\frac{\Delta T_{stress}}{\Delta T_{use}} \right)^{n}$$

AF	Acceleration Factor
ΔT_{stress}	Temperature swing during stress test
ΔT_{use}	Temperature swing during use
n = 6	CM exponent; brittle fractures (JEP122)

CM exponent 6 is selected because the failure mode to cover is not solder joint fatigue but crack in the BEoL.

To ensure robustness margin while not breaking solder joints, NXP uses 300 c from -40 to 125 °C as a requirement for AL TC, ~ 1.5 x 189 c (*blue-italic*), for non automotive .

For Automotive, AL TC requirements range from 500 to 1000 c

Content

Qualification Method Evolution beyond AEC-Qxx

1. Extended Test Durations on short term
2. Application Level Reliability (Functional Component on a PBC) on short / mid term
3. Standardized Mission Profiles on mid term
4. Health Monitoring & Prognostics on mid / long term
   - Including modeling in predictions
5. “Virtual” qualifications (using modeling) will not replace but complement “real” qualifications on mid / long term
6. Boundary Condition: industry wide exchange of Knowledge on Physics of Fail / Degradation / Change

Contact Details

- NXP Semiconductors
- Gerstweg 2, 6534 AE Nijmegen – BX0.035
- +31 (0)6 51 17 1461
- rene.rongen@nxp.com