The right choices at the right time

Steven Van Hout















































WORLD OF

ECHNOLOGY







Lifecycle status





Design for Logistics - DfL







Low risk to EOL

Medium risk to EOL. Part could be EOL in the future.

Medium Risk (48)

High Risk (3)

Low Risk (18)

Obsolete (3)

Unconfirmed (1)

Unknown (1)

Lifecycle risk

Prediction of risk on End Of Life (EOL)

WORLD OF

FECHNOLOGY

High risk to EOL. Part could be EOL in the near future.

Part is no longer available.

Part is active, but his lifecycle risk is not clear

Risk of part is unknown. This can have several causes, namely

- Incorrect Manufacturing Part Number (MPN) in BOM
- MPN is unknown in database
- No information is found from this MPN









Lifecycle risk trend Design for Logistics - DfL























Design for Logistics - DfL

















Low Risk (52)

Medium Risk (2)

High Risk (20)

Unknown (0)





Availability risk

These components have sufficient stock

These components have a risk of insufficient stock

These components have a risk of stock shortages.

Risk of part is unknown. This can have several causes, namely

- Incorrect Manufacturing Part Number (MPN) in BOM
- MPN is unknown in database
- No information is found from this MPN







03STEP

EOM KEY COMPONENTS



			LIFE CYCLE RISK		LEAD TIMES (in weeks) ■Min ■Max %No Info	vailability Risk
PART CODE	DESCRIPTION	STATUS	2022	2028	0 20 60 80 100	A
B82462A2102M000	Inductor Power Wirewound 1uH 20% 100KHz Ferrite 3A 0.024Ohm DCR Autom	Obsolete	Obsolete	Obsolete		
IRFL024NPBF	Trans MOSFET N-CH Si 55V 4A 4-Pin(3+Tab) SOT-223 Tube	Obsolete	Obsolete	Obsolete		
N25Q064A13ESE40E	NOR Flash Serial (SPI, Dual SPI, Quad SPI) 3V/3.3V 64M-bit 64M/32M/16M x	Obsolete	Obsolete	Obsolete		
BL02RN2R1M2B	Ferrite Beads Radial 7A 0.020hm DCR Bulk	LTB	High Risk	Obsolete		
9C-8.000MAAJ-T	Crystal 8MHz ±30ppm (Tol) ±30ppm (Stability) 18pF FUND 800hm 2-Pin HC-4	LTB	High Risk	Obsolete		
APDS-9301	Light to Digital Ambient Light Sensor Digital 3V Automotive 6-Pin Chip LED	NRND	High Risk	Obsolete		
KM-23ID	LED Uni-Color Hi-Eff. Red 627nm 3-Pin SOT-23 T/R	Unconfirmed	Unconfirmed	Unconfirmed		
XQERDO-H0-CORG-B00000801		Unknown	Unknown	Unknown		
7803SR-C	Module DC-DC 1-OUT 3.3V 0.5A 1.65W 3-Pin SIP	Active	Medium Risk	High Risk		
T83-A90X	Surge Arrestor 3-Electrode Surge Arrestor 90VDC 15KA Thru-Hole	Active	Medium Risk	High Risk		
STM32F427ZIT6	MCU 32-bit ARM Cortex M4 RISC 2MB Flash 2.5V/3.3V 144-Pin LQFP Tray	Active	Low Risk	Medium Risk		
C0805X225K4RAC	Cap Ceramic 2.2uF 16V X7R 10% Pad SMD 0805 Flexible Termination 125°C M	Active	Low Risk	Low Risk		



Design for Logistics - DfL









The choice of package depends on its availability, the size of the board, soldering reliability, etc.























Cost depends on:

- Lifecycle
- Availability and lead time
- Testability
- Package choice





Design for Logistics - DfL



























Design for Testing (DfT):

- List with required test points
- Test access recommendations
- Preliminary testcoverage
- Preliminary teststrategy
- Preliminary delivery quality





SCHEMATICS + BOM



Choose package of components wisely





Design for Manufacturing - DfM























05 STEP



Wrong footprints lead to bad soldering reliability















Design for Manufacturing - DfM









Wrong footprints lead to bad soldering reliability and not placeable components \rightarrow delivery delay







Design for Manufacturing - DfM





05_{STEP}



Small distance between high components lead to hardly repairable components







Design for Manufacturing – DfM





05 STEP



Bad thermal relief leads to tombstoning







Design for Manufacturing – DfM























06STEP



Design for Testing (DfT):

- Test access recommendations
- Final teststrategy
- Final testcoverage
- Final delivery quality



LAYOUT





06STEP



Design for Manufacturing (DfM):

- Manufacturability recommendations
- Footprint issues
- Component placement issues
- Netlist verification
- Final production yield





LAYOUT















Design for Testing - DfT

LAYOUT



























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